



4051

CMOS IC

8-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

DESCRIPTION

UTC **4051** is single 8-channel analog multiplexers/demultiplexers for application as digitally-controlled analog switches.

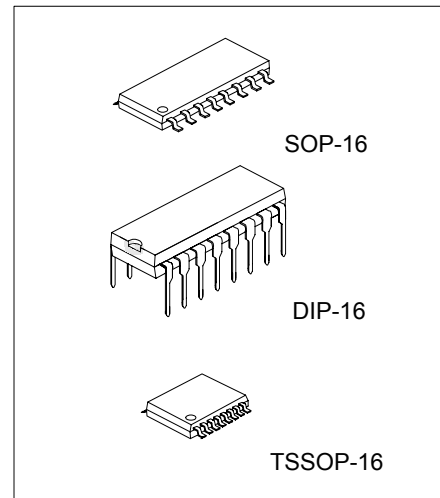
The device has three binary control inputs and an inhibit input. It feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

FEATURES

- * Wide analog voltage range: $V_{DD}-V_{EE} = 3V\sim 18V$.
(Note: V_{EE} must be V_{SS})
- * Break-Before-Make switching eliminates channel overlap.
- * Linearized transfer characteristics
- * Implement an SP8T solid state switch effectively.
- * Pin-to-Pin Replacement for CD4051

ORDERING INFORMATION

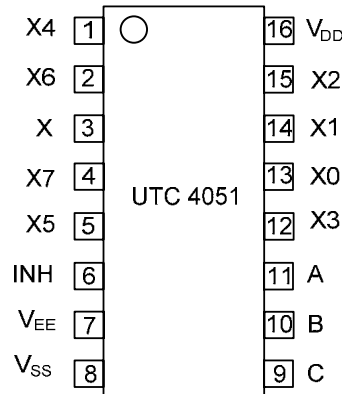
Ordering Number		Package	Packing
Normal	Lead Free Plating		
4051-D16-T	4051L-D16-T	DIP-16	Tube
4051-P16-R	4051L-P16-R	TSSOP-16	Tape Reel
4051-P16-T	4051L-P16-T	TSSOP-16	Tube
4051-S16-R	4051L-S16-R	SOP-16	Tape Reel
4051-S16-T	4051L-S16-T	SOP-16	Tube



*Pb-free plating product number: 4051L

<p>4051L-D16-T</p> <p>(1)Packing Type (2)Package Type (3)Lead Plating</p>	<p>(1) R: Tape Reel, T: Tube (2) D16: DIP-16, P16: TSSOP-16, S16: SOP-16 (3) L: Lead Free Plating, Blank: Pb/Sn</p>
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■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN No.	SYMBAL	I/O	FUNCTIONS
3	X	I/O	Common input/output
6	INH	I	Inhibit inputs
7	V _{EE}		Supply voltage
8	V _{SS}		Ground
11,10,9	A,B,C	I	Binary control inputs
13,14,15,12,1,5,2,4	X0~X7	I/O	Independent inputs/outputs
16	V _{DD}		Positive supply voltage

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage (Referenced to V_{EE} , V_{SS} V_{EE})	V_{DD}	-0.5 ~ +18	V
Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O)	V_{IN} , V_{OUT}	-0.5 ~ $V_{DD} + 0.5$	V
Input Current (DC or Transient), Per Control Pin	I_{IN}	±10	mA
Switch Through Current	I_{SW}	±25	mA
Power Dissipation	P_D	500	mW
Derating above 65		7	mW/
Junction Temperature	T_J	+125	
Operating Temperature	T_{OPR}	-40 ~ +125	
Storage Temperature	T_{STG}	-40 ~ +150	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS ($T_a=25$, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})						
Power Supply Voltage Range	V_{DD}	$V_{DD} - 3.0$ V_{SS} V_{EE}	3		18	V
Quiescent Current Per Package	I_Q	Control Inputs: $V_{IN} = V_{SS}$ or V_{DD} Switch I/O: V_{EE} V_{IO} V_{DD} , and ΔV_{sw} 500mV (Note 2)		0.005 0.010 0.015	5 10 20	μ A
Total Supply Current (Dynamic Plus Quiescent, Per Package)	$I_{D(AV)}$	$T_a=25$ only (The channel component, $(V_{IN}-V_{OUT})/R_{ON}$, is not included.)		(0.07 μ A/kHz) f + I_Q (0.20 μ A/kHz) f + I_Q (0.36 μ A/kHz) f + I_Q		μ A
SWITCHES IN/OUT AND COMMONS OUT/IN -- X, Y, Z (Voltages Referenced to V_{EE})						
Recommended Peak-to-Peak Voltage Into or Out of the Switch	V_{IO}	Channel On or Off	0		V_{DD}	V_{PP}
Recommended Static or Dynamic Voltage Across the Switch	ΔV_{sw}	Channel On	0		600	mV
Output Offset Voltage	$V_{O(OFF)}$	$V_{IN} = 0V$, No Load		10		μ V
ON Resistance	R_{ON}	ΔV_{sw} 500mV $V_{IN} = V_{IL}$ or V_{IH} (Control), and $V_{IN} = 0$ to V_{DD} (Switch)		250 120 80	1050 500 280	Ω
ON Resistance Between Any Two Channels in the Same Package	ΔR_{ON}			25 10 10	70 50 45	Ω
Off-Channel Leakage Current	I_{OFF}	$V_{IN} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel, $V_{DD}=15V$		±0.05	±100	nA
Capacitance, Switch I/O	$C_{I/O}$	Inhibit = V_{DD}		10		pF
Capacitance, Common O/I	$C_{O/I}$	Inhibit = V_{DD}		17		pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	Pins Not Adjacent Pins Adjacent		0.15 0.47		pF

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
CONTROL INPUTS – INHIBIT A, B, C (Voltages Referenced to V_{SS})							
Low Level Input Voltage	V _{DD} =5V	V _{IL}	R _{ON} = per spec, I _{OFF} = per spec		2.25	1.5	V
	V _{DD} =10V				4.50	3.0	
	V _{DD} =15V			6.75	4.0		
High Level Input Voltage	V _{DD} =5V	V _{IH}	R _{ON} = per spec, I _{OFF} = per spec		3.5	2.75	V
	V _{DD} =10V				7	5.5	
	V _{DD} =15V				11	8.25	
Input Leakage Current	I _{LEAK}	V _{IN} = 0 or V _{DD} , V _{DD} =15V		±0.00001	±0.1	μA	
Input Capacitance	C _{IN}			5.0	7.5	pF	

■ DYNAMIC ELECTRICAL CHARACTERISTICS

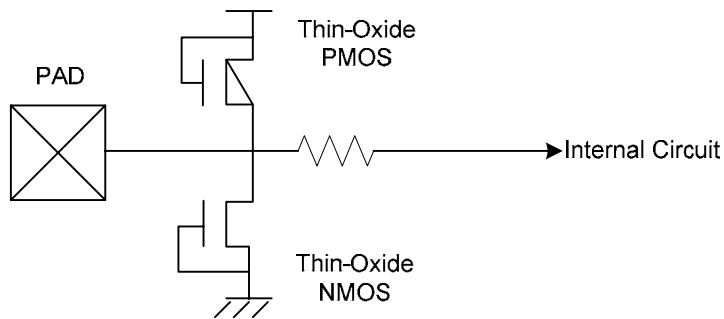
(C_L = 50pF, T_a=25 °C, V_{EE} = V_{SS}, unless otherwise specified)

PARAMETER	SYMBOL	V _{DD} -V _{EE} V _{dC}	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Times Switch Input to Switch Output (R _L = 10 kΩ)	t _{PLH} , t _{PHL}	5	t _{PLH} , t _{PHL} = (0.17 ns/pF)C _L + 26.5ns		35	90	ns
		10	t _{PLH} , t _{PHL} = (0.08 ns/pF)C _L + 11ns		15	40	
		15	t _{PLH} , t _{PHL} = (0.06 ns/pF)C _L + 9ns		12	30	
Inhibit to Output	t _{PHZ} , t _{PLZ} t _{PZH} , t _{PZL}	5	(R _L =10kΩ, V _{EE} =V _{SS})		350	700	ns
		10	Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level		170	340	
		15			140	280	
Control Input to Output	t _{PLH} , t _{PHL}	5	R _L = 10 kΩ, V _{EE} = V _{SS}		360	720	ns
		10			160	320	
		15			120	240	
Total Harmonic Distortion	THD	10	R _L = 10KΩ, f = 1 kHz, V _{in} = 5 V _{PP}		0.07		%
Bandwidth	BW	10	R _L = 1kΩ, V _{IN} = 1/2 (V _{DD} -V _{EE}) p-p, C _L = 50pF, 20 Log (V _{OUT} /V _{IN}) = -3dB		17		MHz
Off Channel Feedthrough Attenuation		10	R _L =1KΩ, V _{IN} = 1/2 (V _{DD} -V _{EE}) p-p f _{IN} = 4.5 MHz		-50		dB
Channel Separation		10	R _L = 1kΩ, V _{IN} = 1/2 (V _{DD} -V _{EE}) p-p f _{IN} = 3MHz		-50		dB
Crosstalk, Control Input to Common O/I		10	R ₁ = 1kΩ, R _L = 10kΩ Control t _{TLH} = t _{THL} = 20ns, Inhibit = V _{SS}		75		mV

Note 1. Data of "TYP" is intended as an indication of the IC's potential performance.

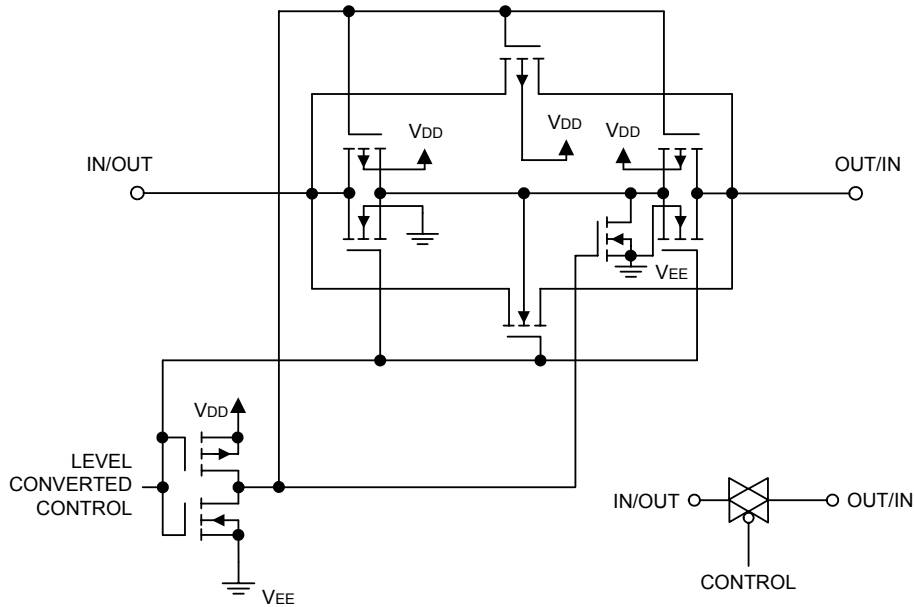
2. For voltage drops across the switch(ΔV_{sw})>600mV (>300mV at high temperature), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

■ ESD PROTECTION CIRCUIT



Standard ESD protection circuit at all input pads.

SWITCH CIRCUIT SCHEMATIC

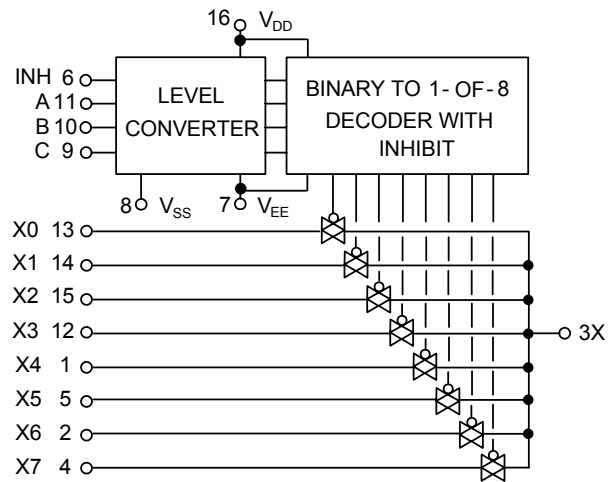


TRUTH TABLE

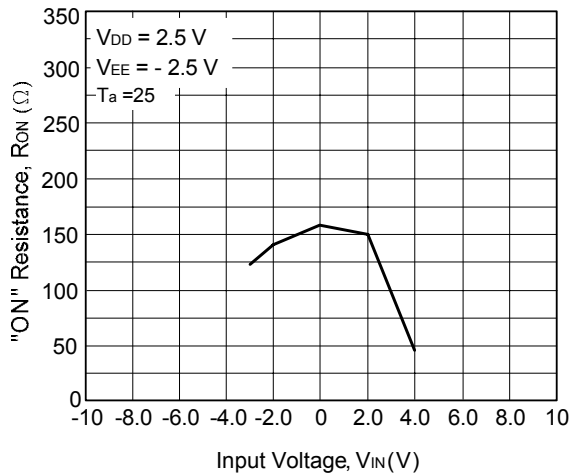
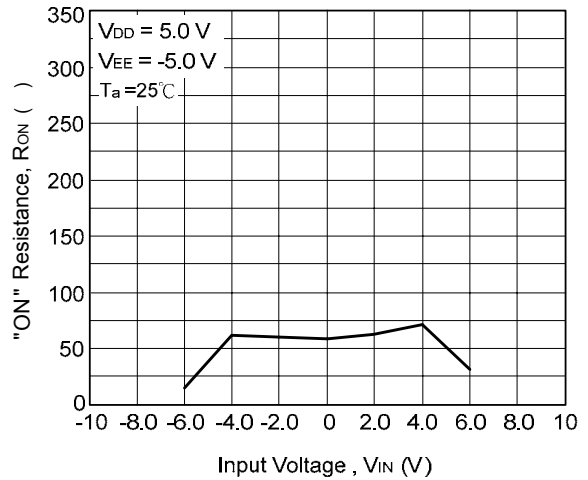
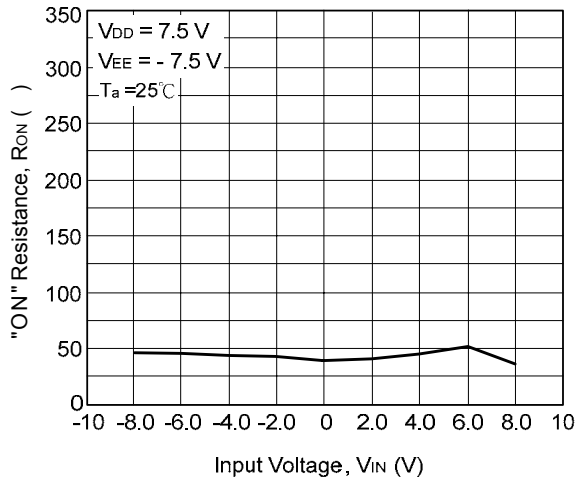
Control Inputs				ON Switches
INHIBIT	C	B	A	
0	0	0	0	X0
0	0	0	1	X1
0	0	1	0	X2
0	0	1	1	X3
0	1	0	0	X4
0	1	0	1	X5
0	1	1	0	X6
0	1	1	1	X7
1	x	x	x	None

x = Don't Care

FUNCTIONAL DIAGRAM



■ TYPICAL CHARACTERISTICS



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