



PA3427

Preliminary

CMOS IC

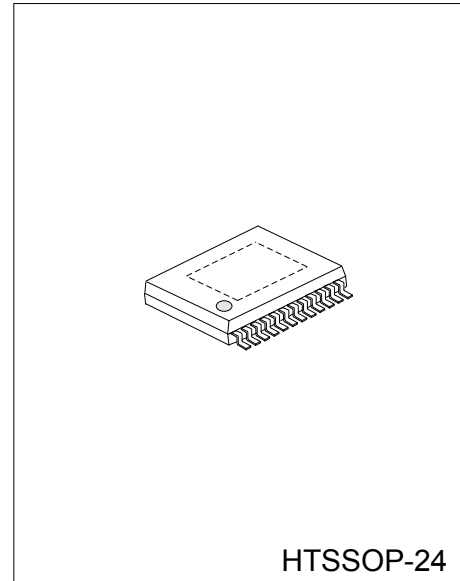
2W STEREO AUDIO AMPLIFIER

DESCRIPTION

The UTC **PA3427** is a stereo audio speaker operated on a single 5V supply. It is capable of delivering 2W of output power per channel in Bridge-Tied Load mode into 4Ω load with less than 1% THD+N.

Two terminals (GAIN0 and GAIN1) can configure and control the amplifier gain. In order to simplify the design of audio system in the notebook application, the two modes of Bridge-Tied Load (BTL) and Single-End (SE) mode drive the speakers and headphone respectively. The UTC **PA3427** supports two input paths to choose two different amplitude AC signals through setting HP/LINE pin.

The UTC **PA3427** is suitable for applications, such as stereo power amplifiers of notebooks or desktop computers, and multimedia monitors.



FEATURES

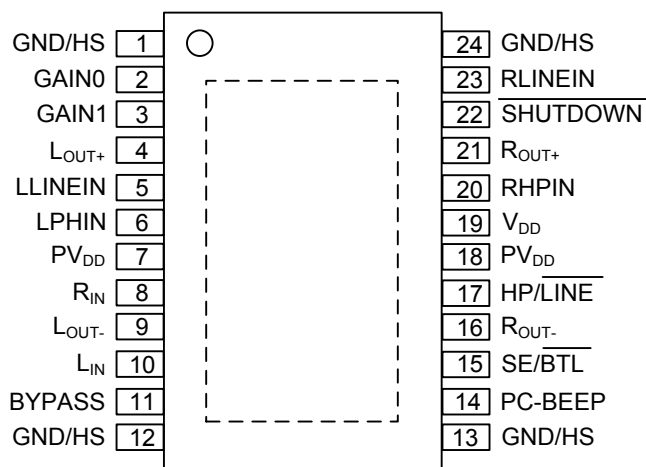
- * Depop circuitry integrated
- * BTL gain: 6dB, 10dB, 15.6dB, 21.6dB
SE gain: 4.1dB
- * Output power (THD+N:1%, supply voltage:5V)
 - 2.0W into a 4Ω load
 - 1.2W into a 8Ω load
- * With two mode :BTL and SE
- * Stereo input multiplexer
- * Fully differential input
- * Build-in gain control
- * PC-Beep input function
- * Thermal shutdown protection
- * Halogen Free

ORDERING INFORMATION

Ordering Number	Package	Packing
PA3427G -N24-R	HTSSOP-24	Tape Reel
PA3427G -N24-T	HTSSOP-24	Tube

<p>PA3427G-N24-R</p> <p>(1)Packing Type (2)Package Type (3)Halogen Free</p>	<p>(1) R: Tape Reel T: Tube (2) N24: HTSSOP-24 (3) G: Halogen Free</p>
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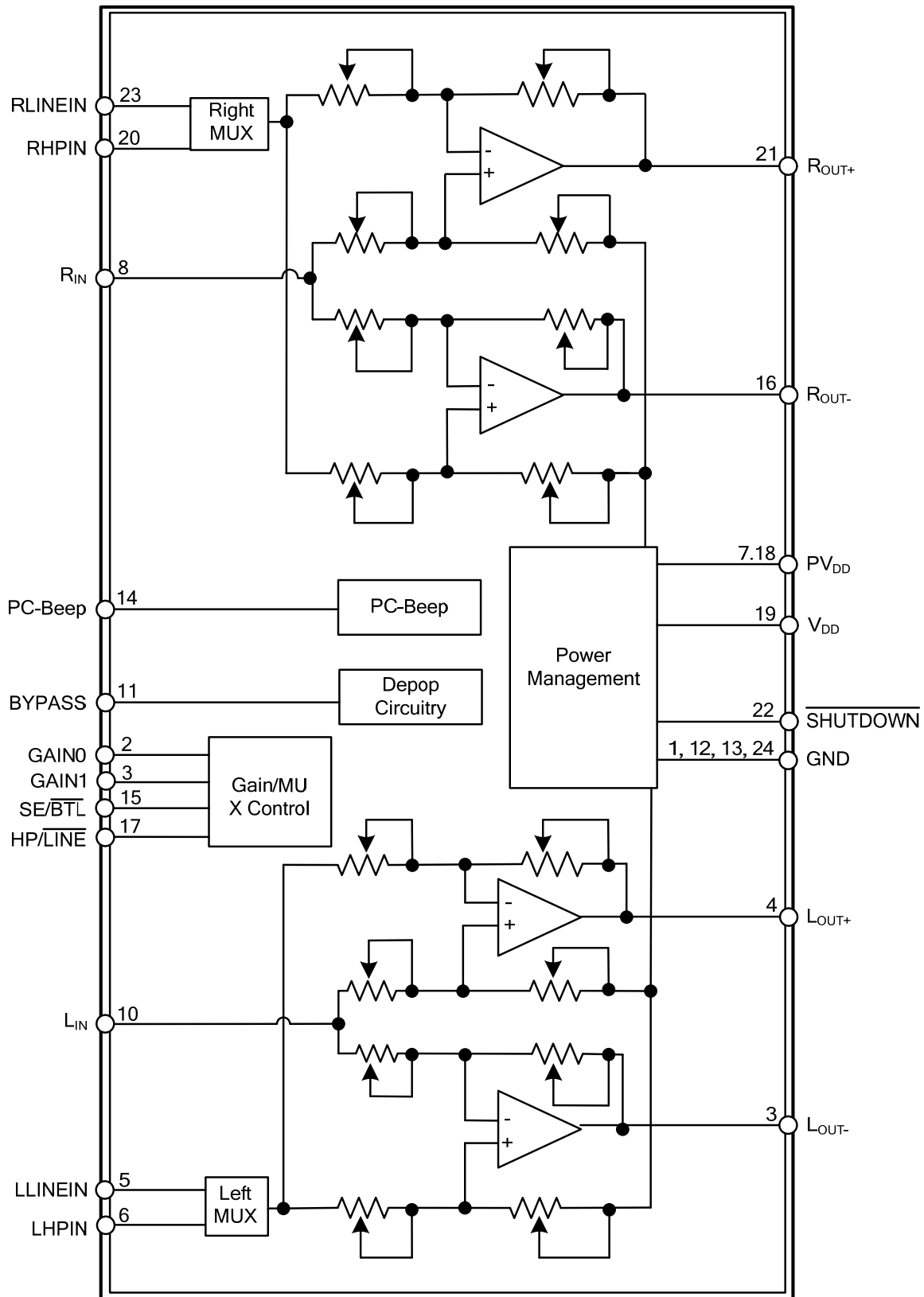
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO	PIN NAME	I/O	DESCRIPTION
1,12,13,24	GND/HS		Ground, directly connected to thermal pad.
2	GAIN0	I	Bit 0 of gain control
3	GAIN1	I	Bit 1 of gain control
4	L _{OUT+}	O	Positive output for Left channel in BTL mode, + output in SE mode.
5	LLINEIN	I	Line input for left channel, selected when HP/LINE pin is held low.
6	LHPIN	I	Left channel headphone input, selected when HP/LINE pin is held high.
7,18	PV _{DD}	I	Supply voltage
8	R _{IN}	I	Differential input for Right channel. AC ground for single-ended inputs.
9	L _{OUT-}	O	Negative output for Left channel, and high impedance in SE mode.
10	L _{IN}	I	Differential input for Left channel. AC ground for single-ended inputs.
11	BYPASS		Tap to voltage divider for internal mid-supply bias generator
14	PC-BEEP	I	The input for PC-BEEP mode. PC-BEEP is enabled when at least eight continuous > 1-V _{PP} (peak to peak) square waves is input to PC-BEEP pin.
15	SE/ BTL	I	Hold low for BTL mode, hold high for SE mode.
16	R _{OUT-}	O	negative output for Right channel
17	HP/LINE	I	MUX control input, hold high to select headphone inputs (6, 20), hold low to select line inputs (5, 23).
19	V _{DD}		Analog V _{DD} supply voltage
20	RHPIN	I	Right channel headphone input, selected when HP/LINE pin is held high.
21	R _{OUT+}	O	Positive output for right channel in BTL mode, positive output in SE mode.
22	SHUTDOWN	I	In shutdown mode when held low, expect PC-BEEP remains active.
23	RLINEIN	I	Line input for Right channel, selected when HP/LINE pin is held low.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	6	V
Power Dissipation ($T_a=25^\circ\text{C}$)	P_D	2.7	W
Junction Temperature	T_J	150	$^\circ\text{C}$
Operating Temperature	T_{OPR}	-40 ~ +85	$^\circ\text{C}$
Storage Temperature	T_{STG}	-65 ~ +150	$^\circ\text{C}$

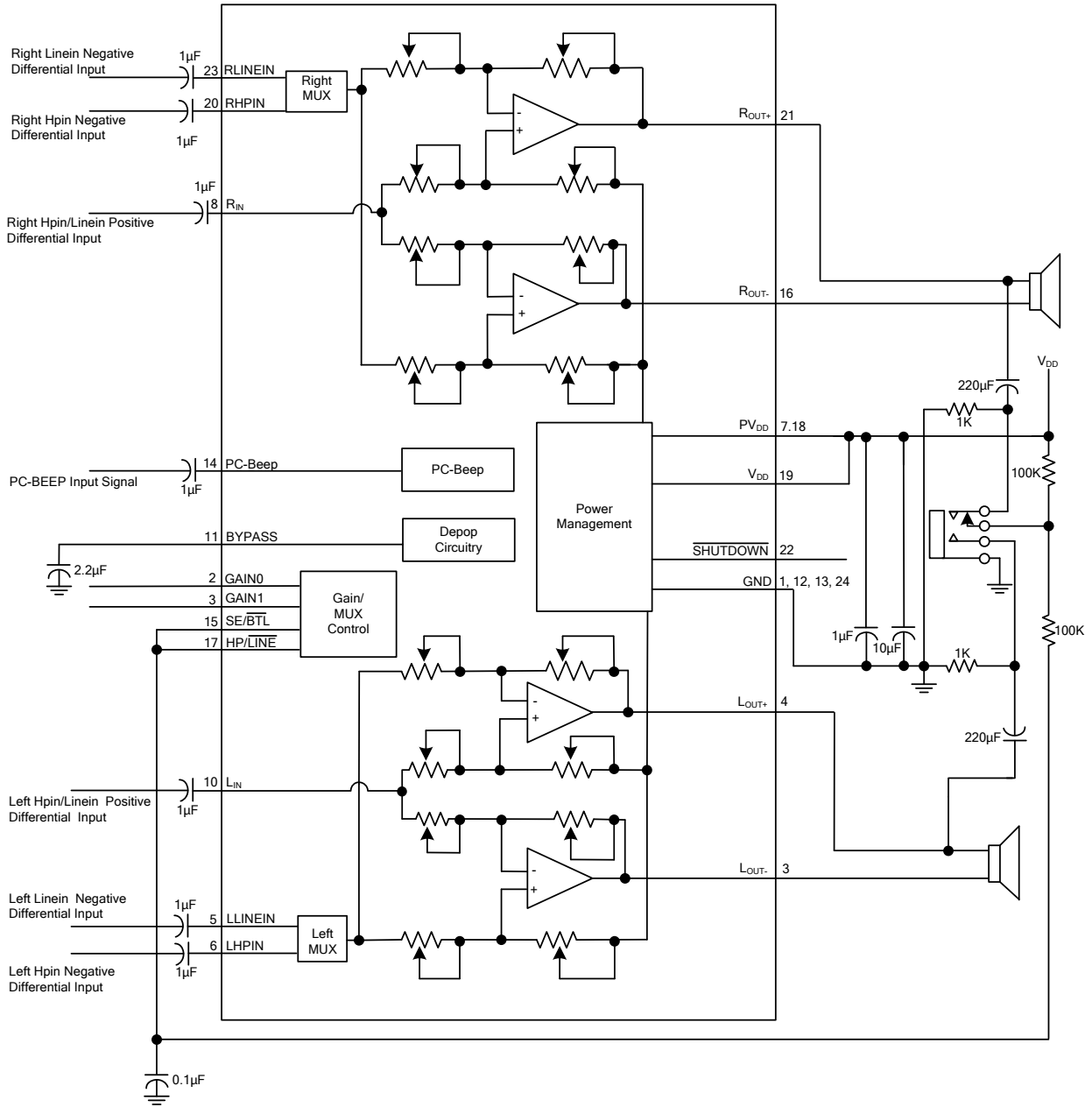
Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS ($T_a=25^\circ\text{C}$)						
Supply voltage	V_{DD}		4.5	5	5.5	V
High-Level Input Voltage	V_{IH}	SE/ $\overline{\text{BTL}}$, HP/ $\overline{\text{LINE}}$, SHUTDOWN GAIN0, GAIN1	2			V
Low-Level Input Voltage	V_{IL}	SE/ $\overline{\text{BTL}}$, HP/ $\overline{\text{LINE}}$, SHUTDOWN GAIN0, GAIN1			0.8	V
DC Differential Output Voltage	$V_{O(DIFF)}$	$V_{DD}=5\text{V}$, Gain = 2V/V		5	50	mV
Supply Current in Mute Mode	I_{DD}	$V_{DD}=5\text{V}$, Stereo BTL		7.5	13	mA
		$V_{DD}=5\text{V}$, Stereo SE		4	7	mA
I_{DD} in Shutdown Mode	I_{SD}	$V_{DD}=5\text{V}$		160	300	μA
AC ELECTRICAL CHARACTERISTICS ($T_a=25^\circ\text{C}$, $V_{DD}=5.0\text{V}$, $R_L=4\Omega$)						
Output Power (Note)	P_{OUT}	THD =1%, BTL, $R_L=4\Omega$, G=-2V/V		2		W
		THD =1%, BTL, $R_L=8\Omega$, G=-2V/V		1.25		W
		THD =10%, BTL, $R_L=4\Omega$, G=-2V/V		2.5		W
		THD =10%, BTL, $R_L=8\Omega$, G=-2V/V		1.6		W
		THD = 0.1%, SE, $R_L=32\Omega$		85		mW
Total Harmonic Distortion Plus Noise	THD+N	$P_{OUT}=1.6\text{W}$, BTL, $R_L=4\Omega$, G=-2V/V		100		m%
		$P_{OUT}=1\text{W}$, BTL, $R_L=8\Omega$, G=-2V/V		60		m%
		$P_{OUT}=75\text{mW}$, SE, $R_L=32\Omega$		80		m%
		$V_{IN}=1\text{V}$, $R_L=10\text{k}\Omega$, SE		30		m%
Max Output Power Bandwidth	B_W	THD = 5%		> 15		kHz
Power Supply Rejection	PSRR	F=1kHz, BTL, G=-2V/V, $C_{BYP}=1\mu\text{F}$		68		dB
Channel-to-Channel Output Separation		f = 1kHz		80		dB
Line/HP Input Separation				80		dB
BTL Attenuation (SE mode)				85		dB
Signal-to-Noise Ratio	SNR	$P_{OUT}=500\text{mW}$, BTL, G=2V/V		90		dB
Output Noise Voltage	E_N	BTL, G=2V/V, A Weighted filter		45		μVrms

Note: Output power is measured at the output terminals of the IC at 1kHz.

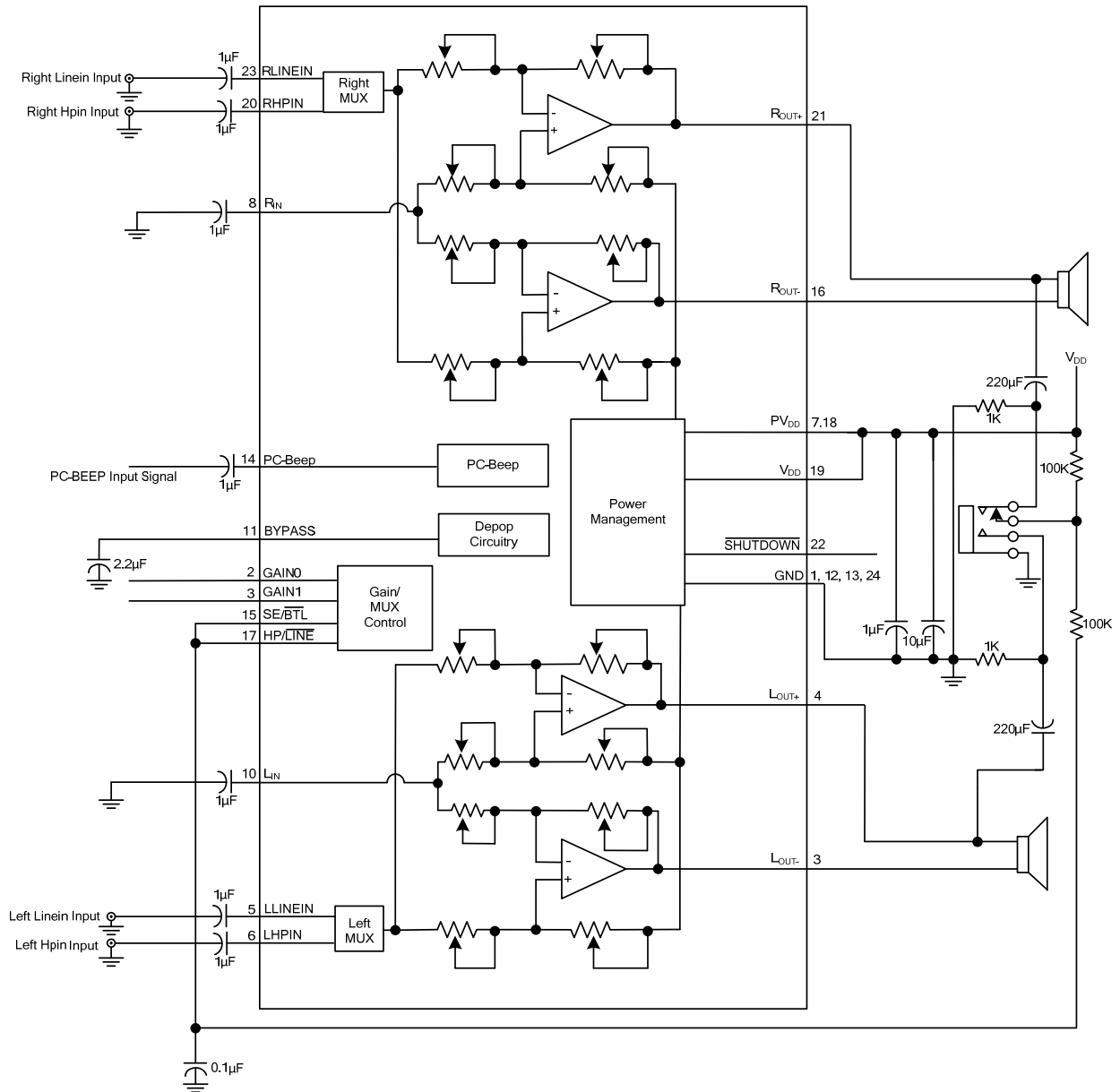
■ TYPICAL APPLICATION CIRCUIT



Application Circuit Using Differential Inputs

Note: 1µF ceramic capacitor must be placed much closely to the IC. For filtering lower frequency noise signals, a larger electrolytic capacitor of 10µF or greater should be placed as close as possible to the audio power amplifier.

■ TYPICAL APPLICATION CIRCUIT(Cont.)



Application Circuit Using Single-Ended Inputs

Note: 1μF ceramic capacitor should be placed as close as possible to the IC to filter the higher-frequency noise.

■ APPLICATION INFORMATION

1. Shutdown Mode Operating

INPUT			AMPLIFIER	
HP/ $\overline{\text{LINE}}$	SE/ $\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
X	X	L	X	MUTE
L	L	H	LINE	BTL
L	H	H	LINE	SE
H	L	H	HEADPHONE	BTL
H	H	H	HEADPHONE	SE

X: Don't care

L: Low

H: High

2. Gain setting (VS Gain0, Gain1 and Ri, SE/BTL)

Gain setting is determined by GAIN0 and GAIN1. The gains listed in the next table are realized by changing the taps on the input resistors inside the amplifier which will cause the internal input impedance(R_i) to be dependent on the gain setting as we can see listed in the next table.

A_v (dB)	GAIN0	GAIN1	SE/ $\overline{\text{BTL}}$	R_i (k Ω)
6	0	0	0	90
10	0	1	0	70
15.6	1	0	0	45
21.6	1	1	0	30
4.1	X	X	1	-

X: Don't care

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