



UT6302

Power MOSFET

P-CHANNEL ENHANCEMENT MOSFET

DESCRIPTION

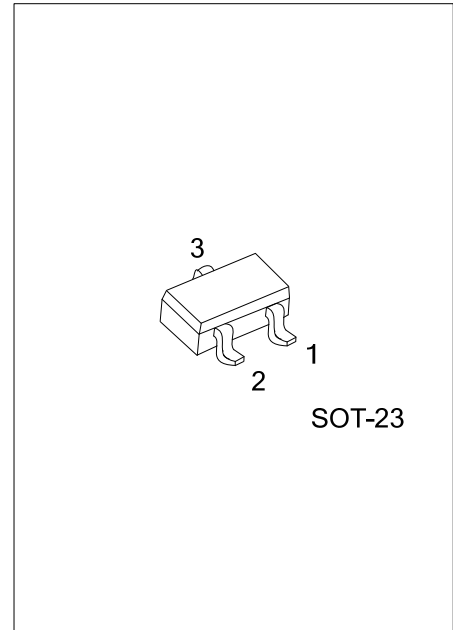
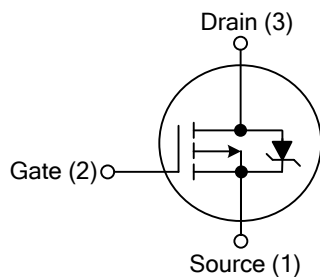
The UTC **UT6302** is a power MOSFET offering the customers efficient and reliable performance.

The UTC **UT6302** is ideal for thin application environments, such as portable electronics and PCMCIA cards.

FEATURES

- * Extremely-Low On-Resistance
- * Fast Switching Speed

SYMBOL

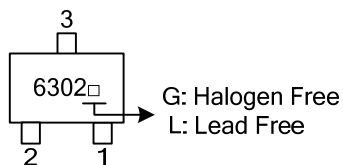


ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT6302L-AE3-R	UT6302G-AE3-R	SOT-23	S	G	D	Tape Reel

<p>UT6302L-AE3-R</p> <p>(1) Packing Type (2) Package Type (3) Lead Free</p>	<p>(1) R: Tape Reel (2) AE3: SOT-23 (3) G: Halogen Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	-20	V
Gate-Source Voltage	V_{GSS}	± 12	V
Continuous Drain Current ($V_{GS} = -4.5\text{V}$, $T_a = 25^\circ\text{C}$)	I_D	-0.78	A
Pulsed Drain Current (Note 2)	I_{DM}	-4.9	A
Peak Diode Recovery dv/dt (Note 3)	dv/dt	-5.0	V/nS
Power Dissipation ($T_a = 25^\circ\text{C}$)	P_D	540	mW
Linear Derating Factor above 25°C		4.3	mW/ $^\circ\text{C}$
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Pulse width limited by $T_{J(MAX)}$

3. $I_{SD} \leq -0.61\text{A}$, $di/dt \leq 76\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J = 150^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	230	$^\circ\text{C}/\text{W}$

Note: Surface Mounted on FR-4 Board, $t \leq 5\text{sec}$.

■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{V}$, $I_D = -250\ \mu\text{A}$	-20			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS} = -16\text{V}$, $V_{GS} = 0\text{V}$			-1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 12\text{V}$, $V_{DS} = 0\text{V}$			± 100	nA
Drain-Source Breakdown Voltage	$\Delta BV_{DSS}/\Delta T_J$	$I_D = -1\text{mA}$, Reference to 25°C		-4.9		mV/ $^\circ\text{C}$
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu\text{A}$	-0.70		-1.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS} = -4.5\text{V}$, $I_D = -0.61\text{A}$ (Note 2)			0.60	Ω
		$V_{GS} = -2.7\text{V}$, $I_D = -0.31\text{A}$ (Note 2)			0.90	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{DS} = -15\text{V}$, $V_{GS} = 0\text{V}$, $f = 1.0\text{MHz}$		97		pF
Output Capacitance	C_{OSS}			53		pF
Reverse Transfer Capacitance	C_{RSS}			28		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{GS} = -4.5\text{V}$, $V_{DS} = -16\text{V}$ $I_D = -0.61\text{A}$ (Note 1, 2)		2.4	3.6	nC
Gate Source Charge	Q_{GS}			0.56	0.84	nC
Gate Drain Charge	Q_{GD}			1.0	1.5	nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD} = -10\text{V}$, $I_D = -0.61\text{A}$, $R_G = 6.2\ \Omega$, $R_D = 16\ \Omega$ (Note 1, 2)		13		nS
Turn-ON Rise Time	t_R			18		nS
Turn-OFF Delay Time	$t_{D(OFF)}$			22		nS
Turn-OFF Fall-Time	t_F			22		nS

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage	V_{SD}	$I_S = -0.61A, V_{GS} = 0V$			-1.2	V
Maximum Continuous Drain-Source Diode Forward Current	I_S				-0.54	A
Maximum Pulsed Drain-Source Diode Forward Current (Note 1)	I_{SM}				-4.9	A
Reverse Recovery Time	t_{RR}	$T_J = 25^\circ C, I_F = -0.61A,$		35	53	nS
Reverse Recovery Charge	Q_{RR}	$di/dt = 100A/\mu s$ (Note 2)		26	39	nC

Notes: 1. Repetitive Rating; Pulse width limited by $T_{J(MAX)}$
 2. Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

■ TEST CIRCUITS AND WAVEFORMS

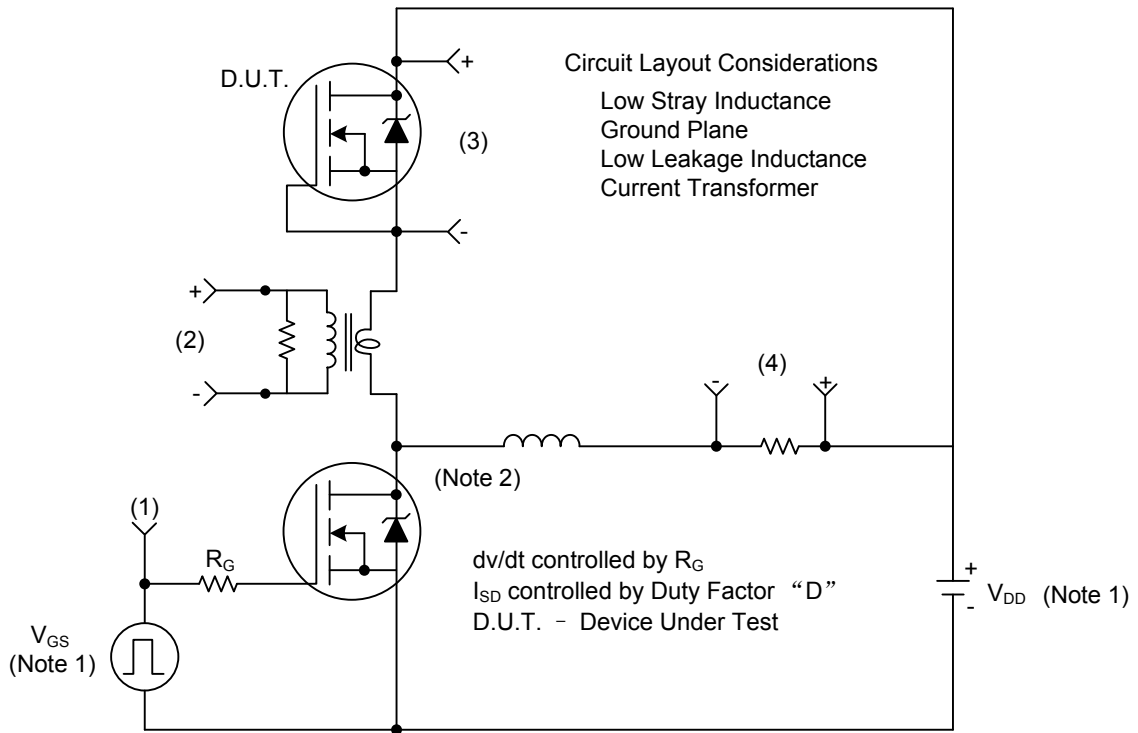


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

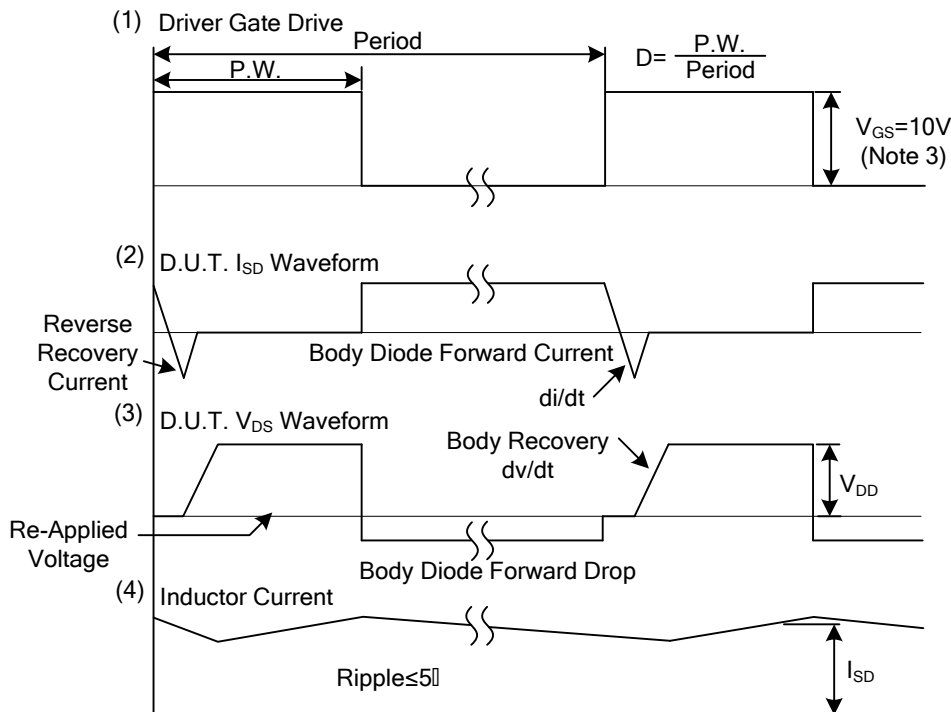
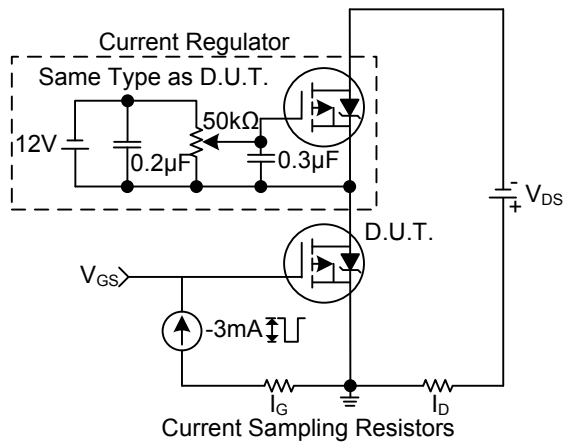


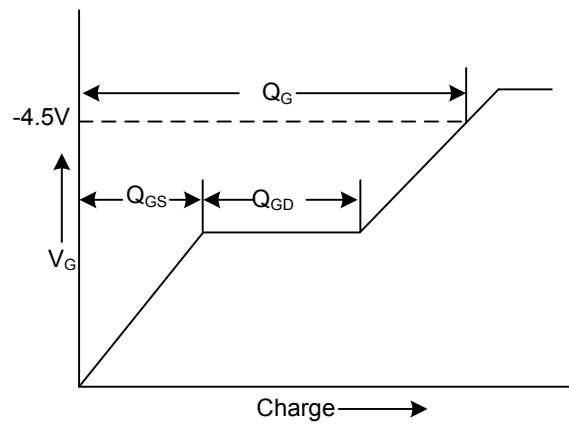
Fig. 1B Peak Diode Recovery dv/dt Waveforms

- Note:
1. Reverse Polarity for P-Channel
 2. Use P-Channel Driver for P-Channel Measurements
 3. $V_{GS}=5.0V$ for Logic Level and 3V Drive Devices

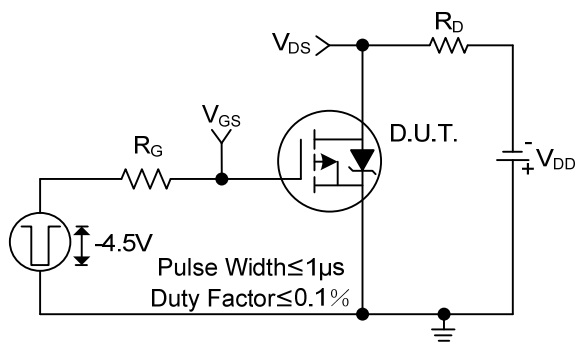
■ TEST CIRCUITS AND WAVEFORMS(Cont.)



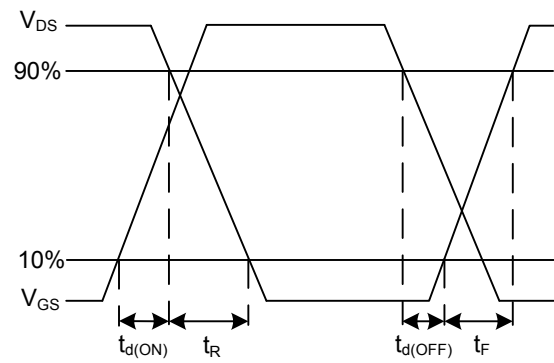
Gate Charge Test Circuit



Gate Charge Waveforms

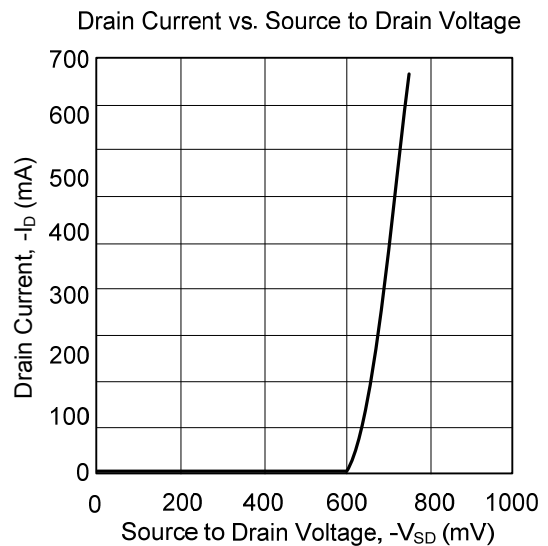
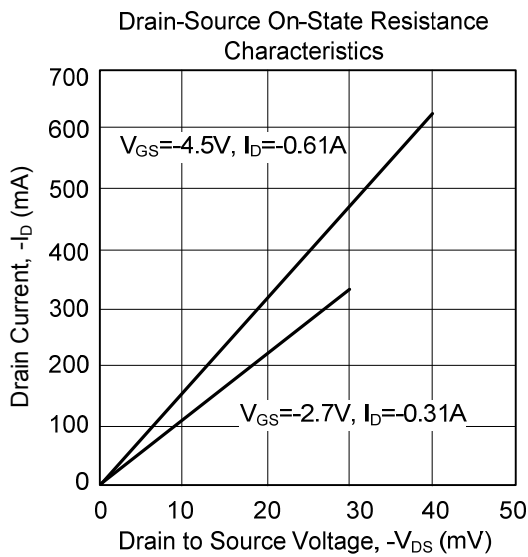
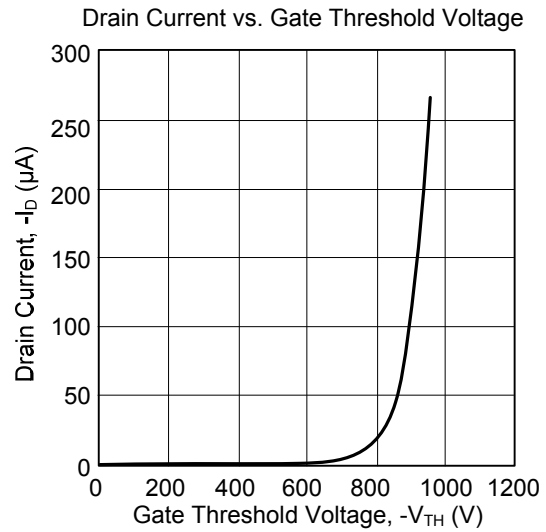
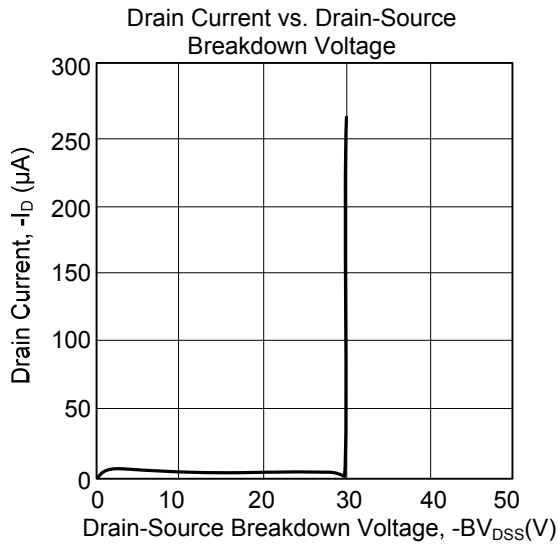


Switching Time Test Circuit



Switching Time Waveforms

TYPICAL CHARACTERISTICS



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