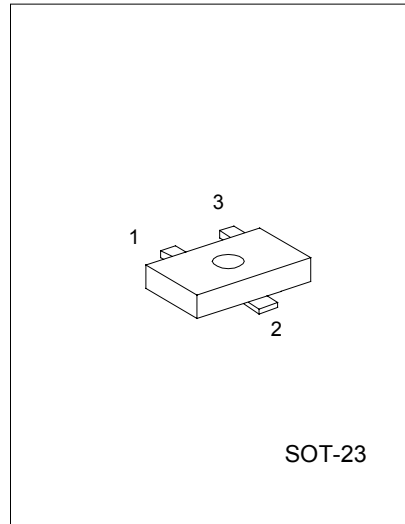


SCRs

DESCRIPTION

The XL1225/ML1225 silicon controlled rectifiers are high performance planar diffused PNP devices. These parts are intended for low cost high volume applications.



1: GATE 2: ANODE 3: CATHODE

ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise specified)

PARAMETERS	PART NO.	SYMBOL	TEST CONDITION	MIN.	MAX.	UNITS
Repetitive Peak Off-State Voltage	XL1225	V _{DRM}	T _j =40 to 125°C (RGK =1kΩ)	400		V
	ML1225	V _{DRM}		300		
On-State Current		I _{T(RMS)}	T _c =40°C	0.8		A
Average On-State Current		I _{T(AV)}	Half Cycle=180°, T _c =40°C	0.5		A
Peak Reverse Gate Voltage		V _{GRM}	I _{GR} =10uA	1		V
Peak Gate Current		I _{GM}	10us Max.	0.1		A
Gate Dissipation		P _{G(AV)}	20ms Max.	100		mW
Operating Temperature		T _j		-40	125	°C
Storage Temperature		T _{STG}		-40	125	°C
Soldering Temperature		T _{SLD}	1.6mm from case 10s Max.		250	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Off state leakage current	I _{DRM}	V _{DRM} (RGK=1KΩ), T _j =125°C		0.1	mA
Off state leakage current	I _{DRM}	V _{DRM} (RGK=1KΩ), T _j =25°C		1.0	μA
On state voltage	V _T	AT I _T =0.4A		1.4	V
		AT I _T =0.8A		2.2	
On state threshold voltage	V _{T(TH)}	T _j =125°C		0.95	V
On state slope resistance	R _t	T _j =125°C		600	m
Gate trigger current	I _{GT}	V _D =7V		200	μA
Gate trigger voltage	V _{GT}	V _D =7V		0.8	V
Holding current	I _H	RGK=1KΩ		5	mA
Latching current	I _L	RGK=1KΩ		6	mA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Critical rate of voltage rise	DV/DT	VD=0.67*VDRM(RGK=1KΩ), Tj=125°C			V/μs
Critical rate of current rise	DV/DT	IG=10mA, dIG/dt=0.1A/μs, Tj=125°C			A/μs
Gate controlled delay time	TGD	IG=10mA, dIG/dt=0.1A/μs,		2.2	μs
Commutated turn-off time	TG	Tj=85°C, VD=0.67*VDRM, VR=35V, IT=IT(AV)		200	μs
Thermal resistance junc. to case	Rθ JC				K/W
Thermal resistance junc. to case	Rθ JA				K/W

CLASSIFICATION OF I_{GT}

RANK	B	C	AA	AB	AC	AD
RANGE	50-100μA	100-200μA	8-15μA	15-20μA	20-25μA	25-50μA

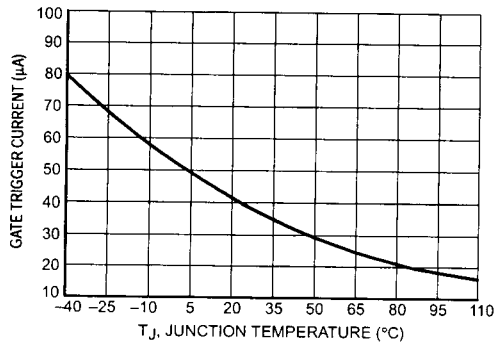


Figure 1. Typical Gate Trigger Current versus Junction Temperature

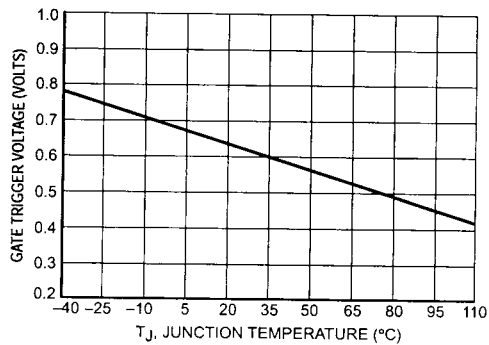


Figure 2. Typical Gate Trigger Voltage versus Junction Temperature

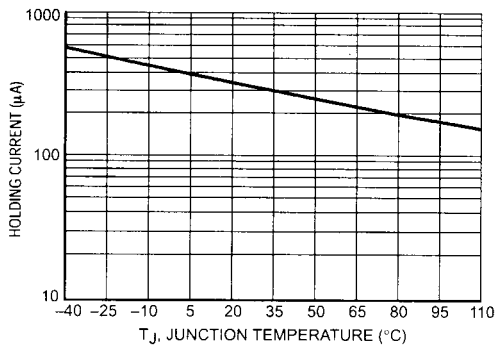


Figure 3. Typical Holding Current versus Junction Temperature

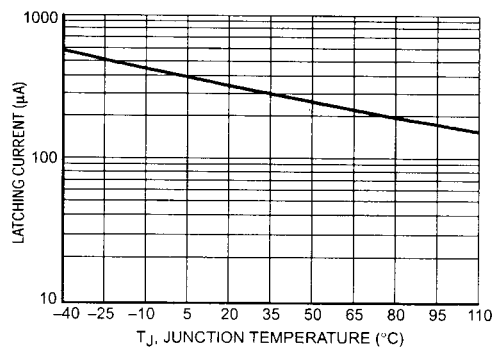


Figure 4. Typical Latching Current versus Junction Temperature

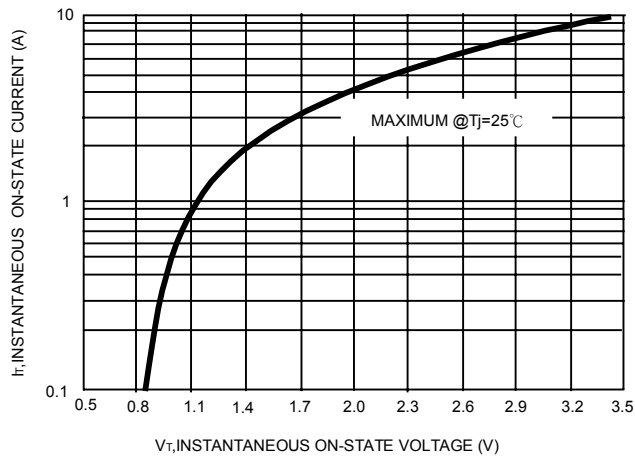


Figure 5. Typical On-State Characteristics

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