



## 3511

CMOS IC

### PC POWER SUPPLY SUPERVISORS

#### DESCRIPTION

The UTC 3511 is designed to provide the voltage, and current supervisor function, power good output (PGO), fault protection latch (FPL\_N), and protection detector function (PDON\_N) control for switching power systems.

For supervisor function, it provides the over voltage detector (OVD) monitoring for 3.3V, 5V, 12V; the under voltage detector (UVD) monitoring for 3.3V, 5V. When 3.3V or 5V voltage is decreasing to 2.69V, 4.3V respectively, the under voltage detector (UVD) function will be enabled to reset the PGO signal from high to low, and the FPL\_N is latched HIGH. When 3.3V, 5V or 12V voltage is increasing to 3.9V, 6.1V or 13.4V respectively, the over voltage detector (OVD) function will be enabled to reset the PGO signal from high to low, and the FPL\_N is latched HIGH.

To achieve better immunity for lightning surge glitch and to prevent accidental power shut down during dynamic loading condition, the de-bounce time for UVD and OVD is 73us. The power supply is turned on after 38mS de-bounce time when FPL\_N signal is set from high to low.

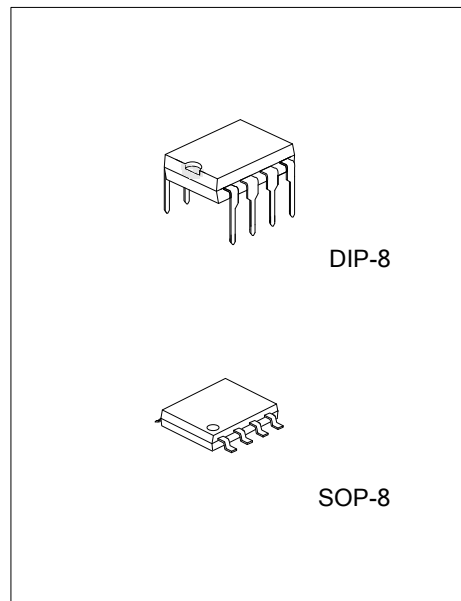
#### FEATURES

- \* Over Voltage Detector (OVD) for 3.3V, 5V, 12V.
- \* Under Voltage Detector (UVD) for 3.3V, 5V.
- \* Open Drain Output for PGO and FPL\_N.
- \* 300 ms power good delay.
- \* 75 ms delay for 3.3V and 5V turn on.
- \* 38 ms PDON\_N control De-bounce.
- \* 2.4 ms PDON\_N control to FPL\_N turn-off delay.
- \* De-bounce time 73 μs for UVD/OVD.
- \* Wide supply voltage range from 4V ~ 15V.

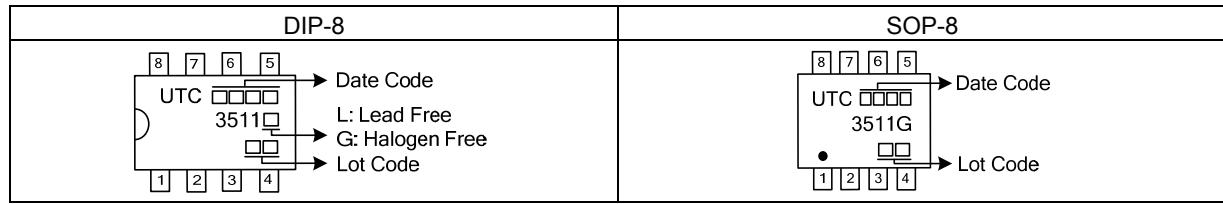
#### ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
3511L-D08-T	3511G-D08-T	DIP-8	Tube
-	3511G-S08-R	SOP-8	Tape Reel

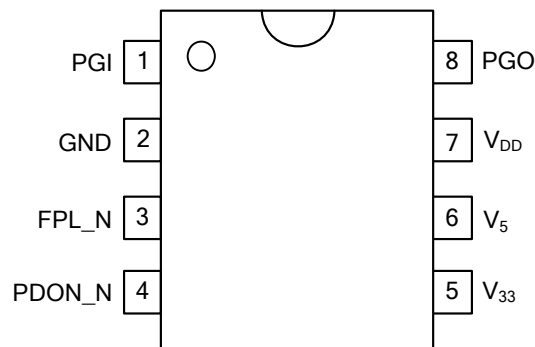
<p>3511L-D08-T</p> <ul style="list-style-type: none"> <li>(1)Packing Type</li> <li>(2)Package Type</li> <li>(3)Green Package</li> </ul>	<ul style="list-style-type: none"> <li>(1) T: Tube, R: Tape Reel</li> <li>(2) D08: DIP-8, S08: SOP-8</li> <li>(3) L: Lead Free, G: Halogen Free and Lead Free</li> </ul>
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## MARKING



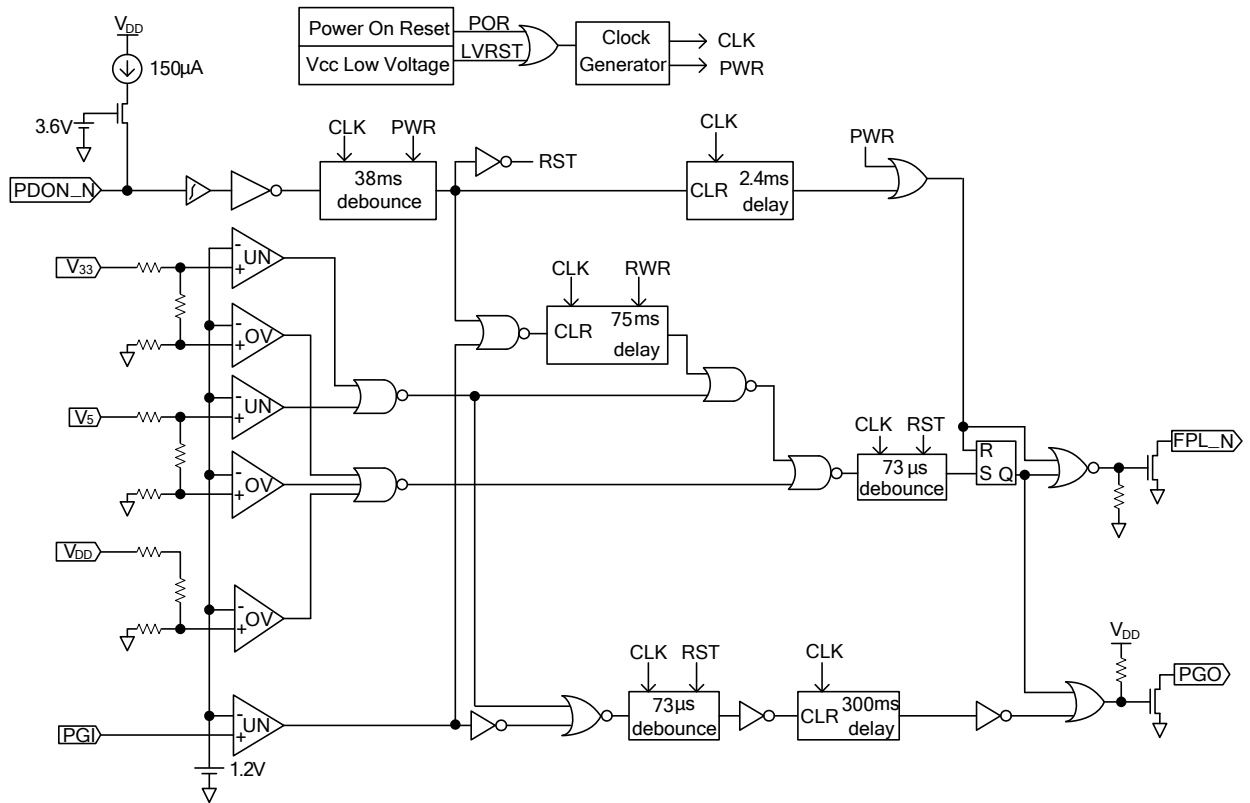
## PIN CONFIGURATION



## PIN DESCRIPTION

PIN No.	PIN NAME	TYPE	DESCRIPTION
1	PGI	I	Power good input pin
2	GND	P	Ground
3	FPL-N	O	Fault protection latch output pin (open drain output)
4	PDON-N	I	Protection detector function ON/OFF control input pin
5	V <sub>33</sub>	I	3.3V input pin
6	V <sub>5</sub>	I	5V input pin
7	V <sub>DD</sub>	I	Supply voltage/12V input pin
8	PGO	O	Power good output pin(open drain output)

■ BLOCK DIAGRAM



### ■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		$V_{DD}$	-0.3 ~ 16	V
Input Voltage	PDON_N, V <sub>5</sub> , V <sub>33</sub> , PGI	$V_{IN}$	-0.3 ~ 7	V
Output Voltage	FPL_N	$V_{OUT}$	-0.3 ~ 16	V
	PGO		-0.3 ~ 7	
Operating Temperature		$T_{OPR}$	-40 ~ 125	°C
Storage Temperature		$T_{STG}$	-55 ~ 150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.  
2. Stresses above those listed may cause permanent damage to the devices

### ■ RECOMMENDED OPERATING CONDITIONS

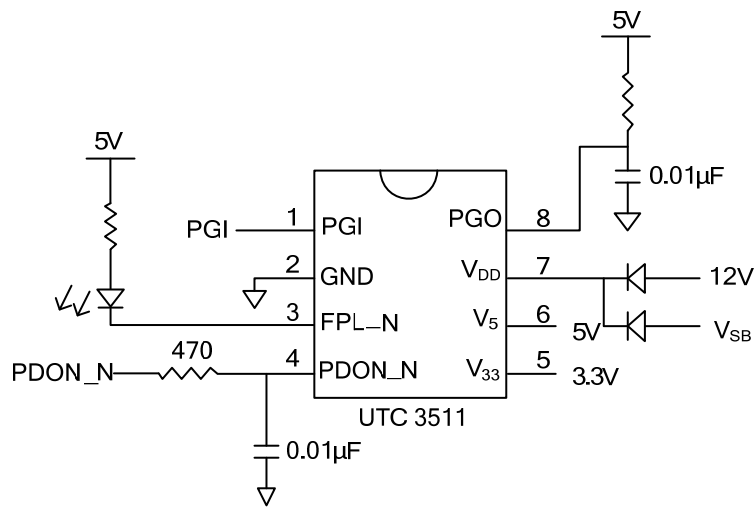
PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		$V_{DD}$	3.8	12	15	V
Input Voltage	PDON_N, V <sub>5</sub> , V <sub>33</sub> , PGI	$V_{IN}$			7	V
Output Voltage	FPL_N	$V_{OUT}$			15	V
	PGO				7	V
Output Sink Current	FPL_N	$I_{OSINK}$			30	mA
	PGO				10	mA
Supply Voltage Rising Time		$T_{RS}$	1			ms

### ■ ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C, V<sub>DD</sub>=5V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
<b>OVER VOLTAGE DETECTION</b>						
Over Voltage Threshold	V <sub>33</sub>		3.7	3.9	4.1	V
	V <sub>5</sub>		5.7	6.1	6.5	
	V <sub>DD</sub> /V <sub>12</sub>		12.8	13.4	13.9	
Low Level Output Voltage (FPL_N)	V <sub>OL</sub>	I <sub>SINK</sub> =10mA I <sub>SINK</sub> =30mA		0.3 0.7		V
Leakage Current (FPL_N)	I <sub>LEAKAGE</sub>	FPL_N=5V		5		μA
<b>PGI AND PGO</b>						
Under Voltage Threshold	V <sub>33</sub>		2.55	2.69	2.83	V
	V <sub>5</sub>		4.1	4.3	4.47	
Input Threshold Voltage (PGI)	V <sub>PGI</sub>		1.16	1.20	1.24	
Low Level Output Voltage (PGO)	V <sub>OL</sub>	I <sub>SINK</sub> =10mA		0.4		V
Leakage Current (PGO)	I <sub>LEAKAGE</sub>	PGO=5V		5		μA
<b>PDON_N</b>						
High-Level Input Voltage	V <sub>IH</sub>		2.4			V
Low-Level Input Voltage	V <sub>IL</sub>				1.2	V
Input Pull-Up Current	I <sub>I</sub>	PDON_N=0V		150		μA
<b>TOTAL DEVICE</b>						
Low Voltage	V <sub>DD</sub>			3		V
Supply Current	I <sub>CC</sub>	PDON_N=5V			1	mA
De-Bounce Time (PDON_N)	t <sub>DB1</sub>		32	38	61	ms
Delay Time (PGI to PGO)	t <sub>DELAY</sub>	T <sub>A</sub> = -40°C ~ 125°C	200	300	490	ms
De-Bounce Time (PDON_N)	t <sub>DB2</sub>		32	38	61	ms
PDON_N to FPL_N delay Time	t <sub>DELAY2</sub>		T <sub>DB2</sub> +2.0	T <sub>DB2</sub> +2.4	T <sub>DB2</sub> +3.8	ms
Internal UVD Delay Time	t <sub>DELAY3</sub>	FPL_N go low & every Time PGI>1.2V	65	75	122	ms
De-Glitch Time	t <sub>G</sub>		63	73	120	us

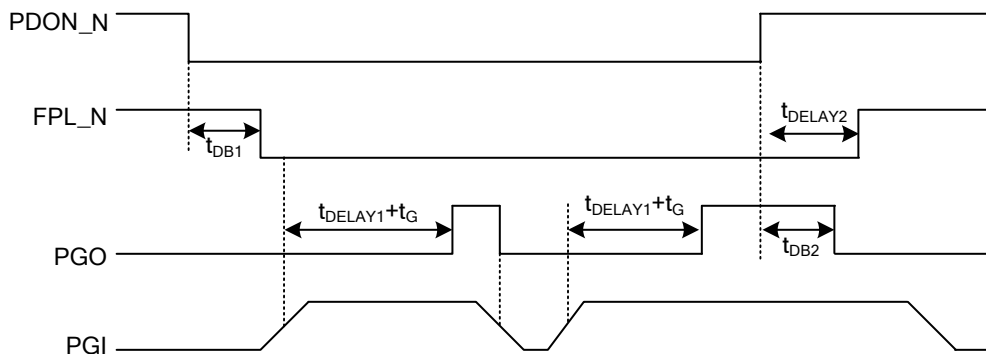
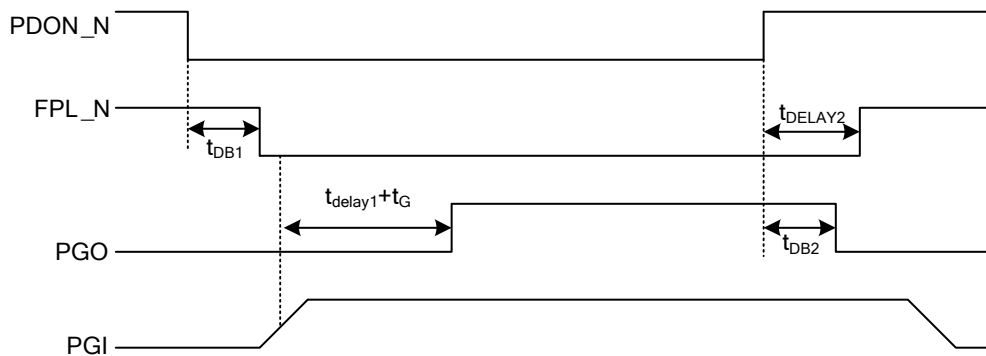


■ APPLICATION CIRCUIT



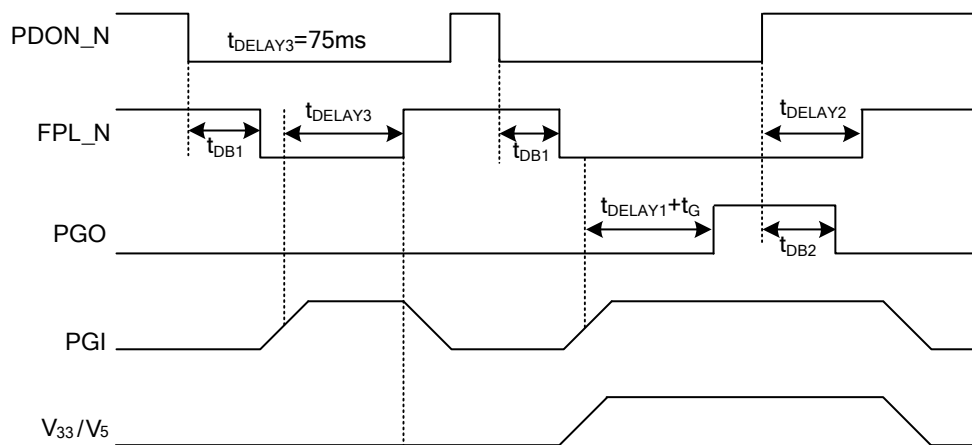
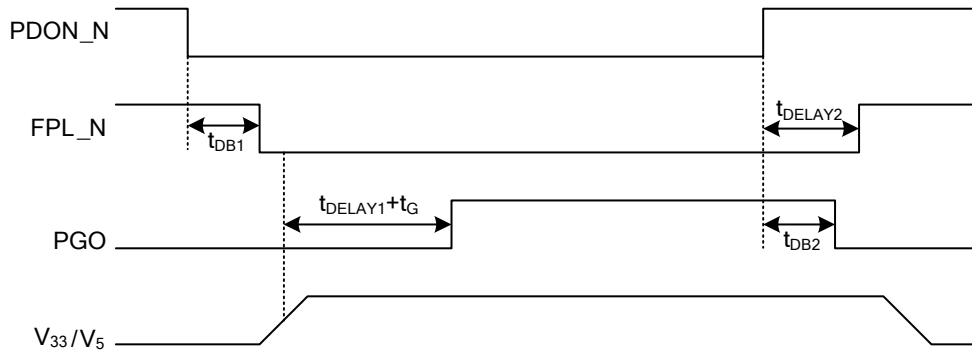
■ APPLICATION TIMMING

1. PGI (UNDER\_VOLTAGE):



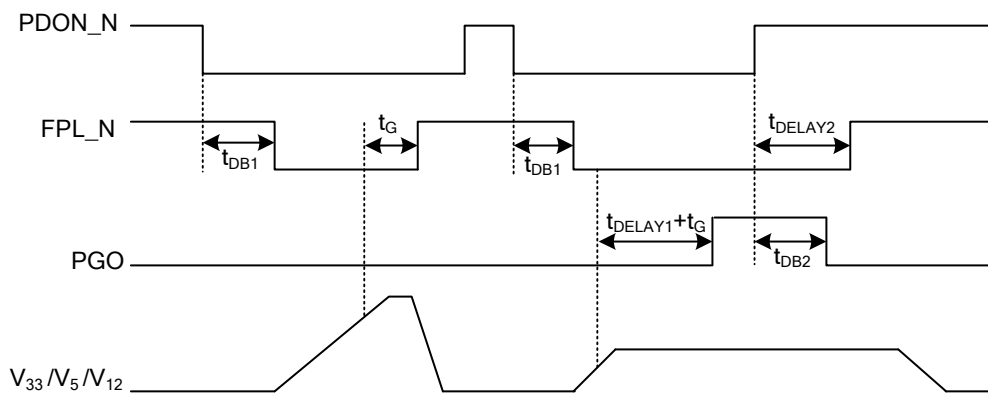
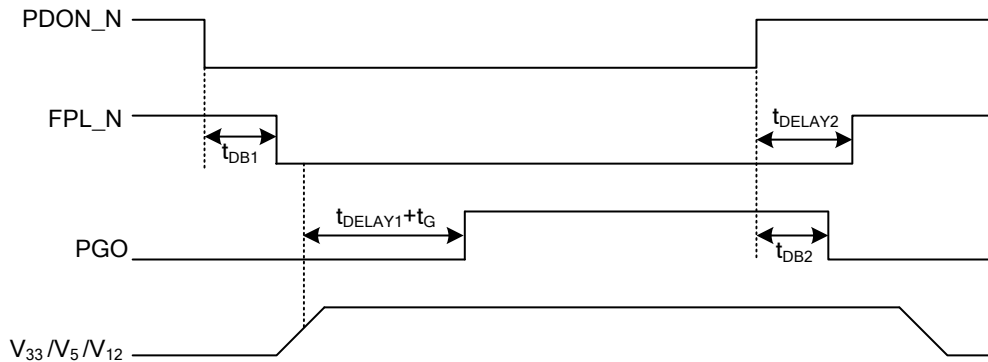
■ APPLICATION TIMMING(Cont.)

2.  $V_{33}$ ,  $V_5$  (UNDER\_VOLTAGE):



■ APPLICATION TIMMING(Cont.)

3.  $V_{33}$ ,  $V_5$ ,  $V_{12}$  (OVER\_VOLTAGE):



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