

UNISONIC TECHNOLOGIES CO., LTD

82XX

Preliminary

# **MONOLITHIC IC 82XX SERIES**

### DESCRIPTION

The normal operation of the UTC **82XX** is that while the power is turned on or interrupted, detect power supply voltage and then reset the system accurately.

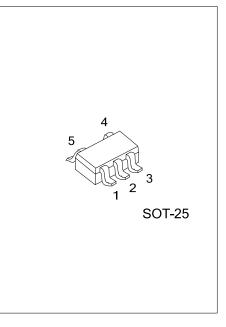
The internal circuits of the UTC **82XX** include a built-in fixed delay time generating circuit. With a counter timer using an analog/digital hybrid circuit, the UTC **82XX** as new low reset type system reset ICs expands the delay time series.

These ICs can be used in a variety of CPU systems and other logic systems.

### FEATURES

- \* Internal Fixed Delay Time Setting by Counter Timer
- \* Grate Delay Time Temperature Characteristics:±800ppm/°C
- \* Operating Limit Voltage as 0.65V(Typ.)
- \* Hysteresis Voltage Provided: 50mV(Typ.)
- \* Circuit Current While On I<sub>CCL</sub>=300µA(Typ.)
- \* Circuit Current While Off I<sub>CCH</sub>=200µA(Typ.)
- \* Open-Drain RESET Active Low Output

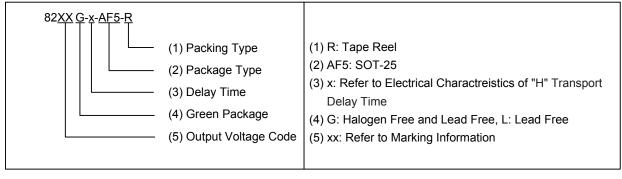
#### ORDERING INFORMATION



Ordering Number		Deskare	Decking	
Lead Free	Halogen Free	Package	Packing	
82XXL-x-AF5-R	82XXG-x-AF5-R	SOT-25	Tape Reel	

Notes: 1. xx: Output Voltage, refer to Marking Information.

2.x: Delay Time, refer to Electrical Characteristics of "H" Transport Delay Time.



# 82XX

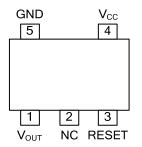
# Preliminary

# LINEAR INTEGRATED CIRCUIT

## MARKING INFORMATION

PACKAGE	VOLTAGE CODE	MARKING			
SOT-25	25: 2.5V 27: 2.7V 2K: 2.93V	Voltage Code			

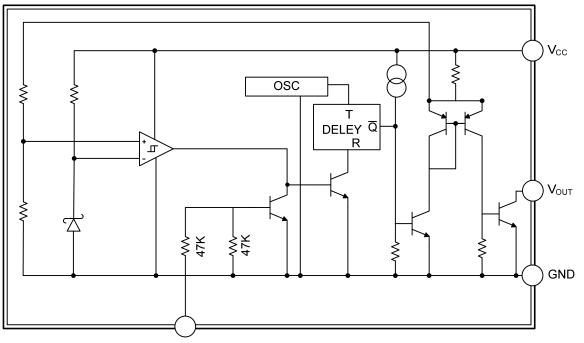
#### ■ PIN CONFIGURATION



#### ■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION				
1	V <sub>OUT</sub>	Dutput pin				
2	NC	Connected nothing				
3	RESET	Reset control pin				
4	V <sub>cc</sub>	Supply voltage				
5	GND	Ground				

#### BLOCK DIAGRAM



MANUAL RESET



#### ■ ABSOLUTE MAXIMUM RATING (T<sub>A</sub>=25°C, Unless otherwise specified)

PARAMETER	SYMBOL	SYMBOL RATINGS	
Power Supply Voltage	V <sub>CC</sub>	-0.3~+10	V
Manual Reset Input Voltage	V <sub>RESET</sub>	-0.3~+10	V
Power Dissipation	PD	400	mW
Operating Temperature	T <sub>OPR</sub>	-20~+75	°C
Storage Temperature	T <sub>STG</sub>	-40~+125	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

#### ■ ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C, Unless otherwise specified)

V<sub>S</sub>=2.5V~2.93V

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
Detection Voltage		Vs	V <sub>OL</sub> ≤0.4V, V <sub>CC</sub> =H→L, R <sub>L</sub> =470Ω (See Test Circuit 1)		V <sub>S</sub> -0.15V	Vs	V <sub>S</sub> +0.15V	V	
Low-Level Output Voltage		V <sub>OL</sub>	$V_{CC}=V_{S(min)}$ -0.05V, R <sub>L</sub> =470Ω (See Test Circuit 1)			0.1	0.4	V	
Operating Power Supply Voltage		V <sub>OPL</sub>	R <sub>L</sub> =4.7kΩ, V <sub>OL</sub> ≤0.4V			0.65	0.85	V	
Hysteresis Voltage		$\Delta V_{S}$	V <sub>CC</sub> =L→H→L , R <sub>L</sub> =470Ω (See Test Circuit 1)		30	50	100	mV	
Detection Voltage Temperature Coefficient		$\frac{V_{S}}{\Delta T}$	$R_L=470\Omega$ , $T_A=-20^{\circ}C \rightarrow +75^{\circ}C$ (See Test Circuit 1)			±0.01		%/°C	
Output Leakag	e Current		I <sub>OH</sub>	V <sub>cc</sub> =10V (See Test Circuit 1)				±0.1	μA
Circuit Current		On	I <sub>CCL</sub>	V <sub>CC</sub> = V <sub>S(MIN)</sub> -0.05V, R <sub>L</sub> =∞			300	600	μA
(See Test Circu	uit 1)	Off	I <sub>CCH</sub>	V <sub>CC</sub> =V <sub>S(TYP)</sub> /0.85V, R <sub>L</sub> =∞			200	350	μA
				Ρ	30	50	75	mS	
				Q	60	100	150	mS	
"H" Transport D	Delay Time		t <sub>PLH</sub>	R <sub>L</sub> =4.7KΩ, C <sub>L</sub> =100PF (Note 1) (See Test Circuit 2)	R	120	200	300	mS
			(See Test Circuit 2)	S	240	400	600	mS	
				-	Т	480	800	1200	mS
"L" Transport Delay Time		t <sub>PHL</sub>	R <sub>L</sub> =4.7kΩ, C <sub>L</sub> =100PF (Note 1) (See Test Circuit 2)			10		μS	
Output Current While on 1		I <sub>OL1</sub>	$V_{CC}$ =VS min0.05V, R <sub>L</sub> =0Ω (See Test Circuit 1)		8			mA	
Output Current While on 2		I <sub>OL2</sub>	$T_A$ =-20°C ~+75°C, R <sub>L</sub> =0Ω(Note 2) (See Test Circuit 1)		6			mA	
Manual Reset	Input High \	/oltage	V <sub>RESH</sub>			2.0			V
	Input High C	Current	I <sub>RESH</sub>	V <sub>RESET</sub> =2V				80	μA
Pin	Input Low V	oltage	V <sub>RESL</sub>					0.8	V

Notes: 1. t<sub>PLH</sub>: V<sub>CC</sub>= (V<sub>S(TYP)</sub>-0.4V) $\rightarrow$ (V<sub>S(TYP)</sub>+0.4V)

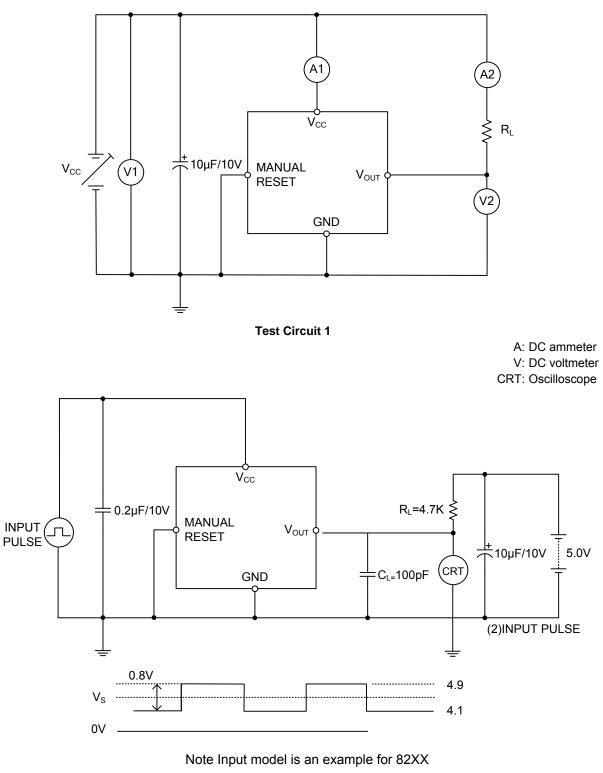
t<sub>PHL</sub>: V<sub>CC</sub>= (V<sub>S(TYP)</sub>+0.4V)→(V<sub>S(TYP)</sub>-0.4V)

2.  $V_{CC}=V_{S(MIN)}-0.15V$ 

3.  $V_{OUT}$  pin is low when manual reset pin is high.  $V_{OUT}$  pin is high when manual reset pin is low.



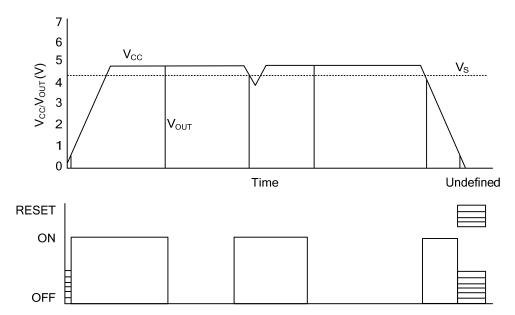
TEST CIRCUITS



Test Circuit 2



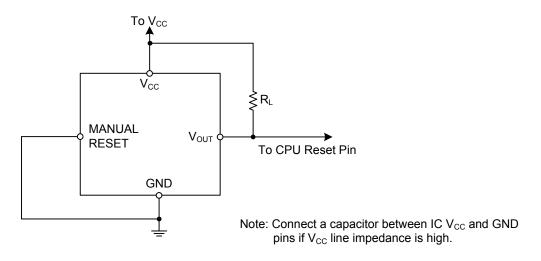
## TIMING CHART



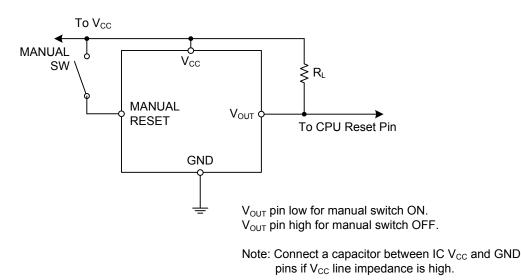


#### **TYPICAL APPLICATION CIRCUITS**

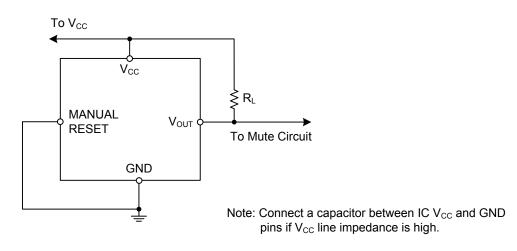
1. Normal hard reset



2. Manual reset



3. Mute circuit





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