



MC4558

LINEAR INTEGRATED CIRCUIT

DUAL OPERATIONAL AMPLIFIER

■ DESCRIPTION

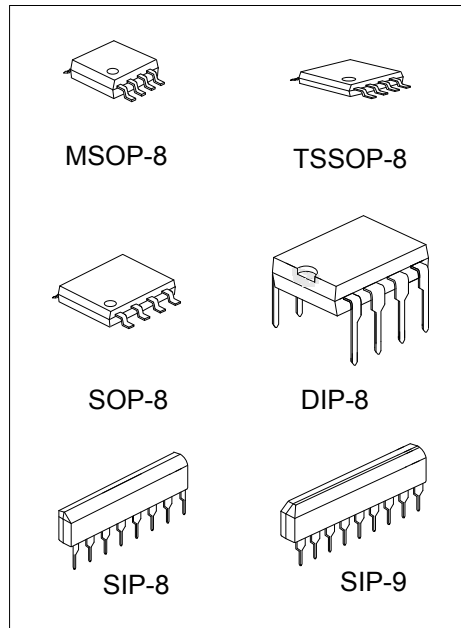
The UTC **MC4558** is a monolithic integrated circuit designed for dual operational amplifier.

■ FEATURES

- * No frequency compensation required
- * No latch-up
- * Large common mode and differential voltage range
- * Parameter tracking over temperature range
- * Gain and phase match between amplifiers
- * Internally frequency compensated
- * Low noise input transistors

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
MC4558L-D08-T	MC4558G-D08-T	DIP-8	Tube
MC4558L-G08-T	MC4558G-G08-T	SIP-8	Tube
MC4558L-L09-T	MC4558G-G09-T	SIP-9	Tube
MC4558L-P08-R	MC4558G-P08-R	TSSOP-8	Tape Reel
MC4558L-S08-R	MC4558G-S08-R	SOP-8	Tape Reel
MC4558L-SM1-R	MC4558G-SM1-R	MSOP-8	Tape Reel



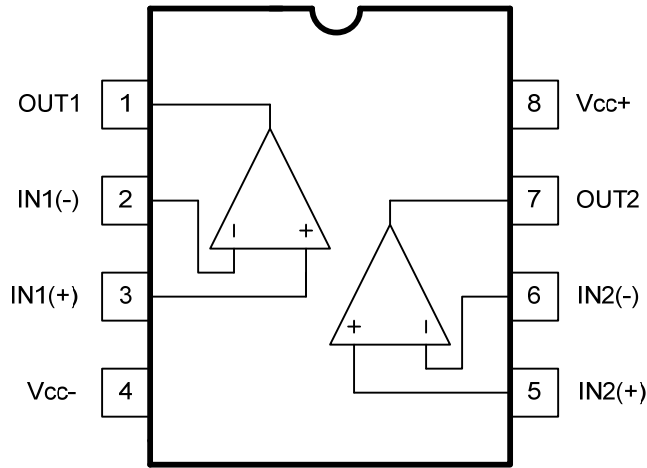
<p>MC4558G-D08-T</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) T: Tube, R: Tape Reel (2) D08: DIP-8, G08: SIP-8, G09: SIP-9, P08: TSSOP-8, S08: SOP-8, SM1: MSOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING

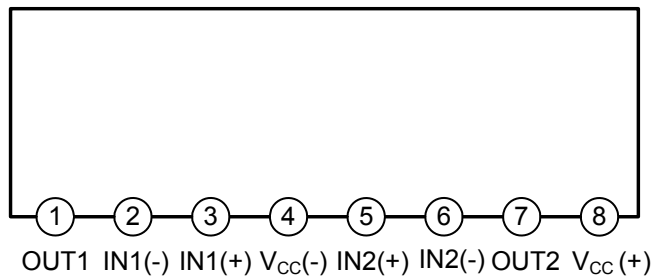
<p>DIP-8</p> <p>Date Code UTC □□□□ MC4558 □ L: Lead Free G: Halogen Free Lot Code</p>	<p>SOP-8/MSOP-8</p> <p>Date Code UTC □□□□ MC4558 □ L: Lead Free G: Halogen Free Lot Code</p>
<p>TSSOP-8</p> <p>Date Code UTC □□□□ MC4558 □ L: Lead Free G: Halogen Free Lot Code</p>	<p>SIP-8 / SIP-9</p> <p>Date Code UTC □□□□ MC4558 □ L: Lead Free G: Halogen Free Lot Code</p>

■ PIN CONFIGURATIONS

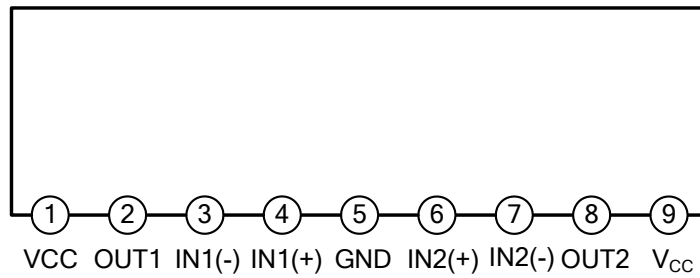
SOP-8/DIP-8/MSOP-8/TSSOP-8



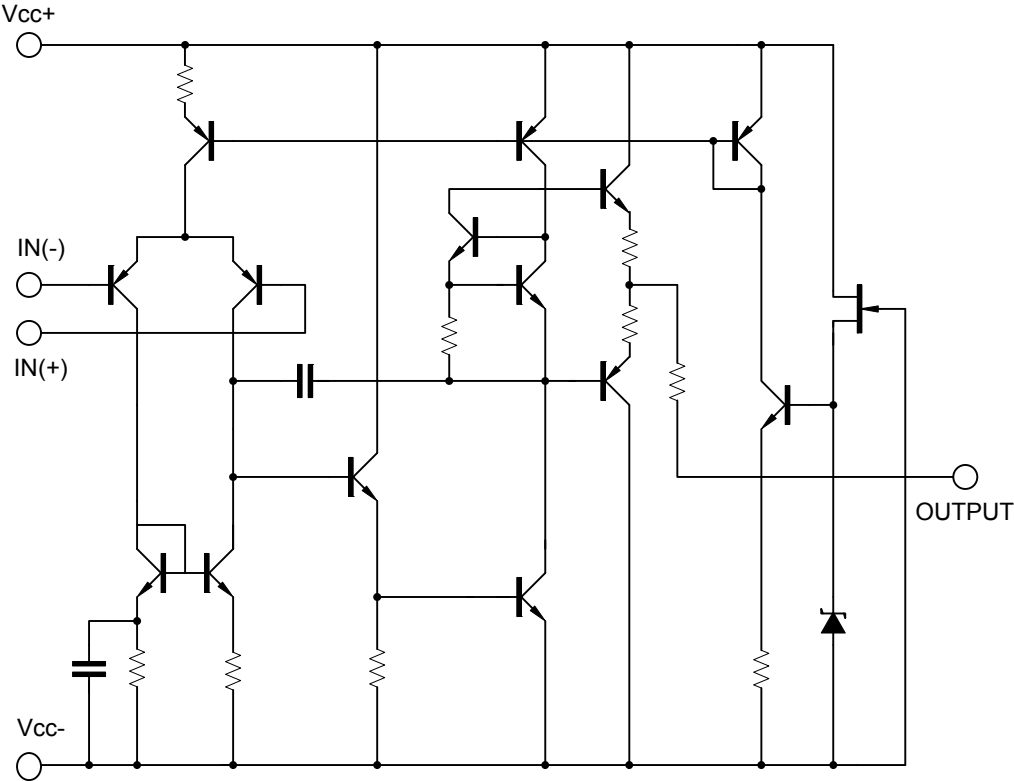
SIP-8



SIP-9



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}	± 22	V
Differential input voltage		$V_{I(DIFF)}$	± 18	V
Power Dissipation	DIP-8	P_D	600	mW
	SOP-8		400	mW
	TSSOP-8		300	mW
	SIP-8/SIP-9		750	mW
	MSOP-8		250	mW
Input Voltage		V_{IN}	± 15	V
Junction Temperature		T_J	+125	°C
Operating Temperature (Note 2)		T_{OPR}	-40 ~ +125	°C
Storage Temperature		T_{STG}	-40 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

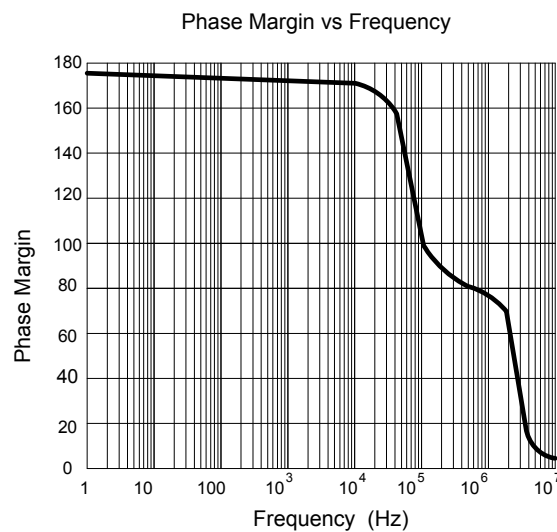
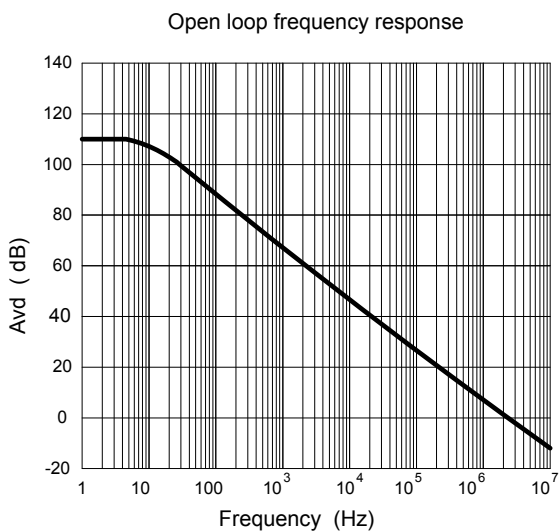
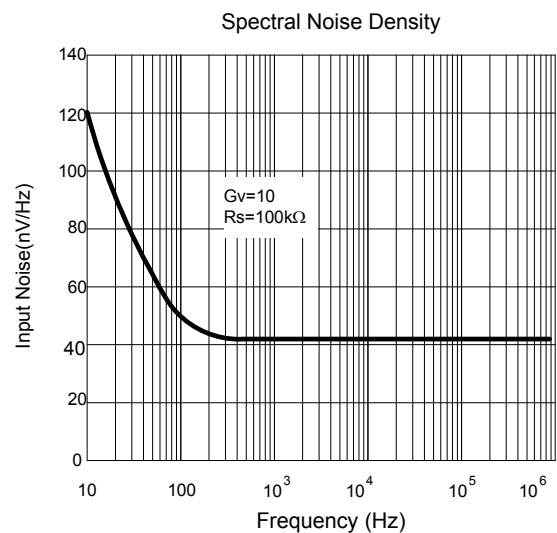
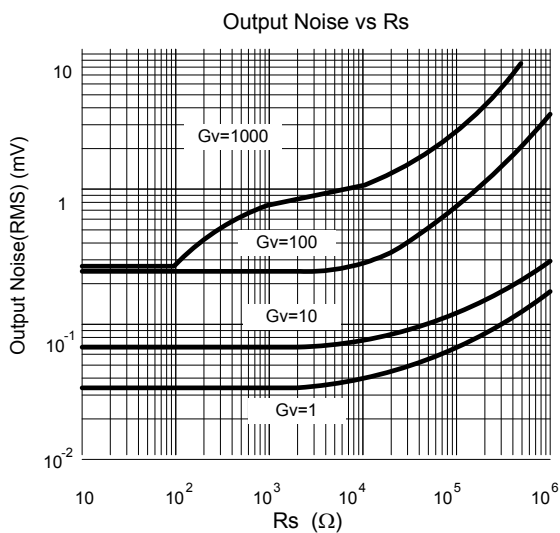
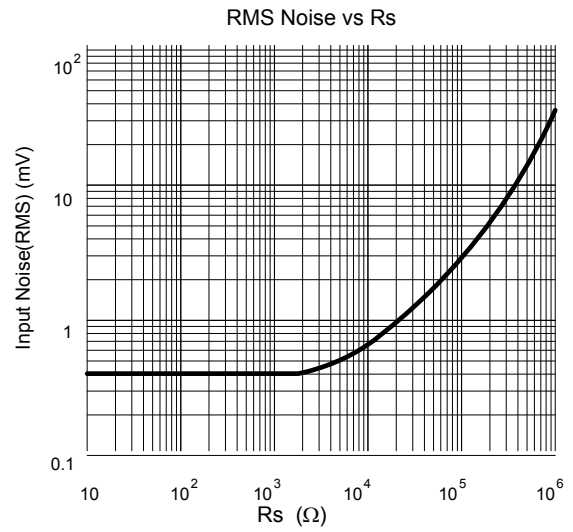
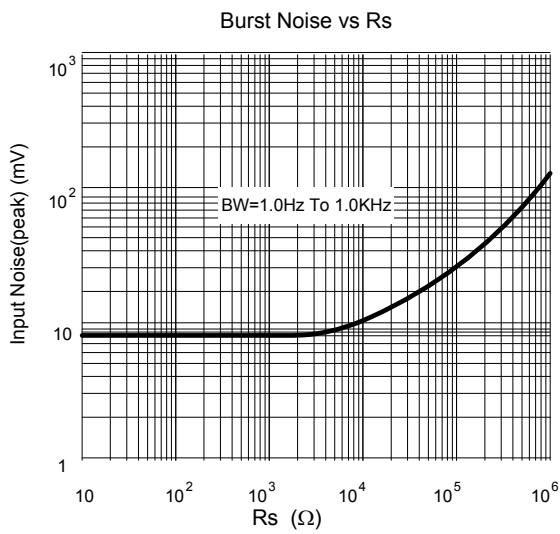
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. It is guarantee by design, not 100% be tested.

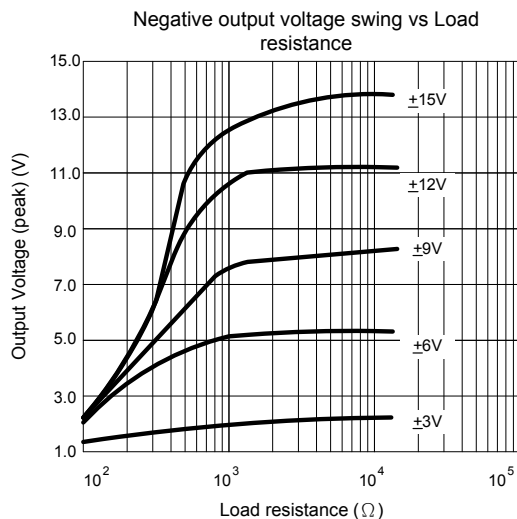
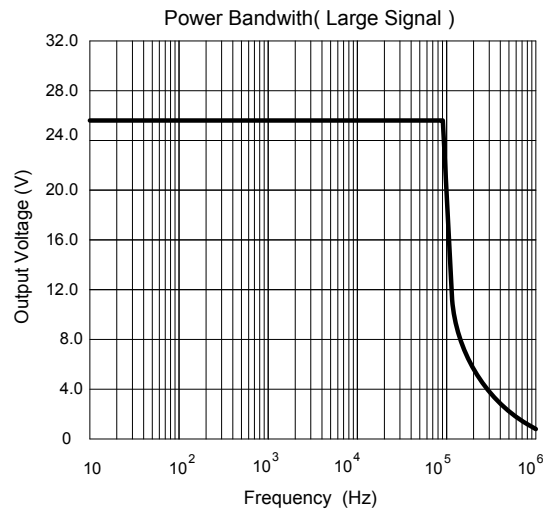
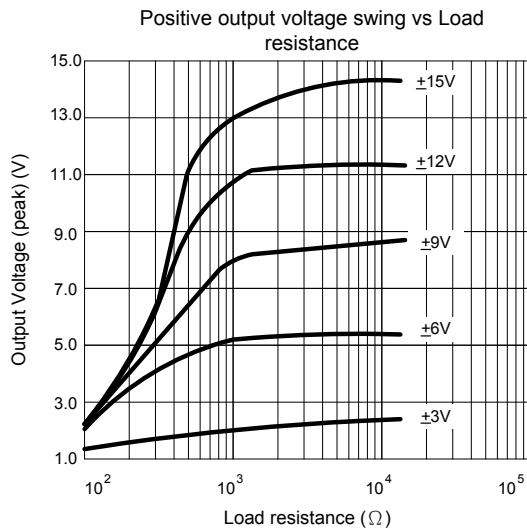
■ ELECTRICAL CHARACTERISTICS ($V_{CC}=15V$, $V_{EE}=-15V$, $T_A=25^\circ C$.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current, all Amp, no load	I_{CC}			2.3	4.5	mA
Input offset voltage	$V_{I(OFF)}$	$R_S < 10k\Omega$		2	6	mV
Input offset current	$I_{I(OFF)}$			5	200	nA
Input bias current	$I_{I(BIAS)}$			30	500	nA
Large signal voltage gain	G_V	$V_o(p-p) = \pm 10V$, $R_L \cong 2k\Omega$	20	200		V/mV
Common Mode Input Voltage Range	$V_{I(COM)}$		± 12	± 13		V
Common Mode Rejection Ratio	$RR_{(COM)}$	$R_S \cong 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$RR_{(VCC)}$	$R_S \cong 10k\Omega$	76	90		dB
Output Voltage swing	$V_{O(p-p)}$	$R_L \geq 10k\Omega$	± 12	± 14		V
Power Consumption	P_C			70	170	mW
Slew Rate	SR	$V_{IN} = \pm 10V$, $R_L \cong 2k\Omega$, $C_L \cong 100pF$	1.2	2.2		V/ μs
Rise Time	T_{RIS}	$V_{IN} = \pm 20mV$, $R_L \cong 2k\Omega$, $C_L \cong 100pF$		0.3		μs
Overshoot	OS	$V_{IN} = \pm 20mV$, $R_L \cong 2k\Omega$, $C_L \cong 100pF$		15		%
Input Resistance	R_{IN}		0.3	2		M Ω
Output Resistance	R_{OUT}			75		Ω
Total Harmonic Distortion	THD	$f=1kHz$, $A_v=20dB$, $R_L=2k\Omega$, $V_{OUT}=2V_{pp}$, $C_L=100pF$		0.008		%
Channel Separation	V_{O1}/V_{O2}			120		dB
FREQUENCY CHARACTERISTIC						
Unity Gain Bandwidth	BW		2.0	2.8		MHz

TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS(Cont.)



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