



TL072

LINEAR INTEGRATED CIRCUIT

LOW NOISE DUAL J-FET OPERATIONAL AMPLIFIER

DESCRIPTION

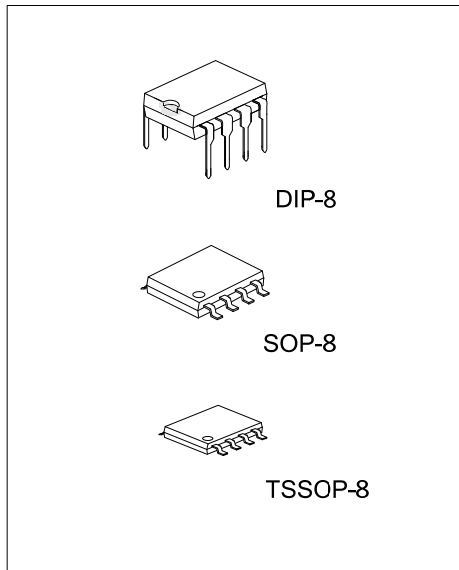
The UTC **TL072** is a high speed J-FET input quad operational amplifier. It incorporates well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit. The device features high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

FEATURES

- * Low power consumption
- * Wide common-mode (up to V_{CC+}) and differential voltage range
- * Low input bias and offset current
- * Low noise $e_n = 15nV / \sqrt{Hz}$ (typ.)
- * Output short-circuit protection
- * High input impedance J-FET input stage
- * Low harmonic distortion:0.01% (typ.)
- * Internal frequency compensation
- * Latch up free operation
- * High slewrate:10V/ μs (typ.)

ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
TL072L-D08-T	TL072G-D08-T	DIP-8	Tube
TL072L-S08-R	TL072G-S08-R	SOP-8	Tape Reel
TL072L-P08-R	TL072G-P08-R	TSSOP-8	Tape Reel

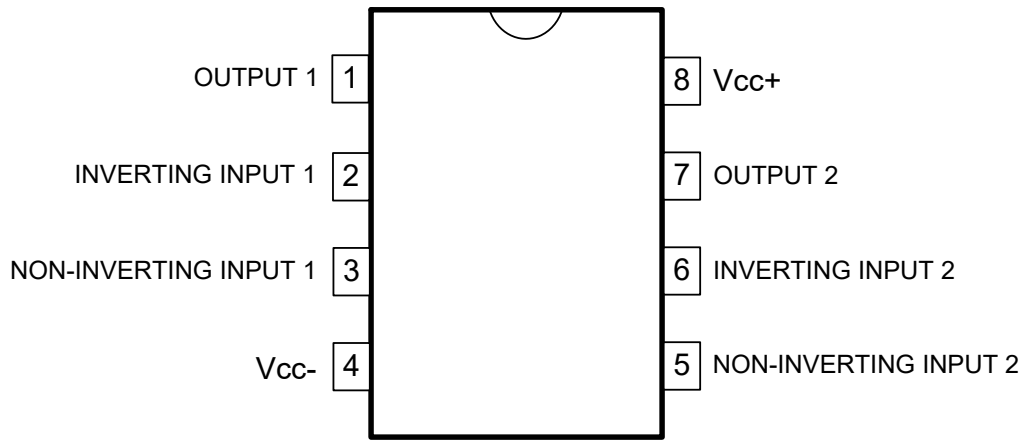


<p>TL072G-D08-T</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) T: Tube, R: Tape Reel (2) D08: DIP-8, S08: SOP-8, P08: TSSOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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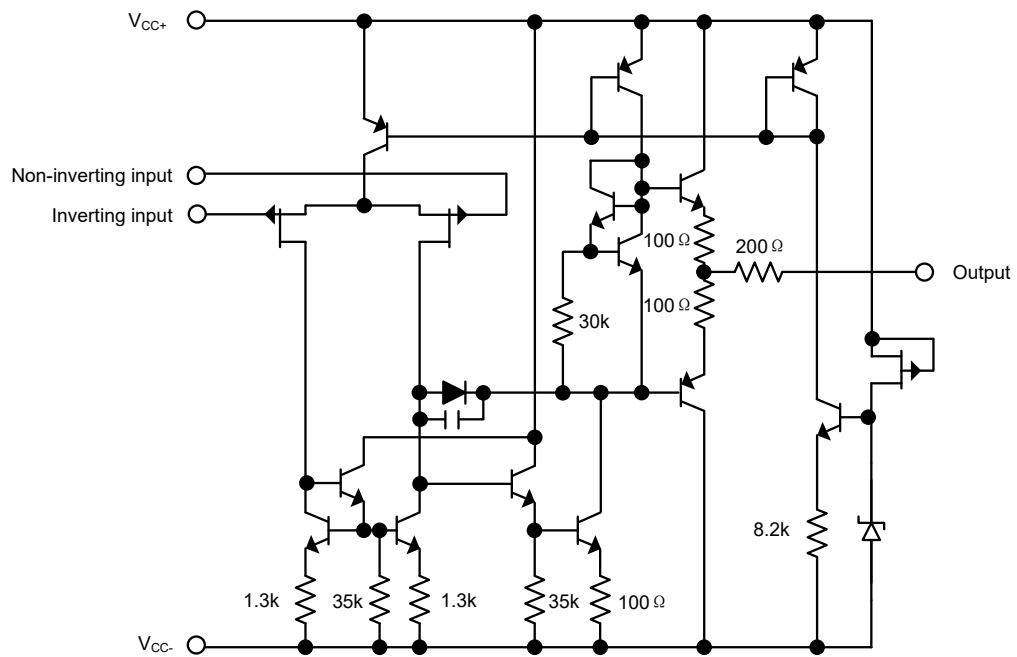
MARKING

DIP-8	SOP-8	TSSOP-8
<p>8 7 6 5 → Date Code UTC □□□□ TL072 □ L: Lead Free G: Halogen Free □□ → Lot Code 1 2 3 4</p>	<p>8 7 6 5 → Date Code UTC □□□□ TL072 □ L: Lead Free G: Halogen Free □□ → Lot Code 1 2 3 4</p>	<p>8 → Date Code 7 → L: Lead Free 6 → G: Halogen Free 5 → Lot Code UTC □□□□ TL072 □ 1 2 3 4</p>

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage (Note 2)		V _{CC}	±18	V
Input Voltage (Note 3)		V _{IN}	±15	V
Differential Input Voltage (Note 4)		V _{I(DIFF)}	±30	V
Power Dissipation	DIP-8	P _D	625	mW
	SOP-8		440	mW
	TSSOP-8		360	mW
Output Short-Circuit Duration (Note 5)			Infinite	
Operating Temperature		T _{OPR}	-40 ~ +125 (Note 6)	°C
Storage Temperature		T _{STG}	-65 ~ +150	°C

- Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC-} and V_{CC+}.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
5. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
6. It is guarantee by design, not 100% be tested.

■ ELECTRICAL CHARACTERISTICS ($V_{CC}=\pm 15V$, $T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Input Offset Voltage	$V_{I(OFF)}$	$R_S=50\Omega$	$T_A=25^\circ C$		3	10	mV
			$T_{MIN} \cong T_A \cong T_{MAX}$				13
Temperature Coefficient of Input Offset Voltage	$\Delta V_{I(OFF)}$	$R_S=50\Omega$			10		$\mu V/^\circ C$
Input Offset Current (Note)	$I_{I(OFF)}$		$T_A=25^\circ C$		5	100	pA
			$T_{MIN} \cong T_A \cong T_{MAX}$				10
Input Bias Current (Note)	$I_{I(BIAS)}$		$T_A=25^\circ C$		20	200	pA
			$T_{MIN} \cong T_A \cong T_{MAX}$				20
Input Common Mode Voltage	$V_{I(CM)}$			± 11	-12~+15		V
Output Voltage Swing	$V_{O(SW)}$	$R_L=2k\Omega$	$T_A=25^\circ C$	± 10	± 12		V
		$R_L=10k\Omega$		± 12	± 13.5		V
		$R_L=2k\Omega$	$T_{MIN} \cong T_A \cong T_{MAX}$	± 10			V
		$R_L=10k\Omega$		± 12			V
Large Signal Voltage Gain	G_V	$R_L=2k\Omega$, $V_{OUT}=\pm 10V$	$T_A=25^\circ C$	25	200		V/mV
			$T_{MIN} \cong T_A \cong T_{MAX}$	15			V/mV
Gain Bandwidth Product	GBW	$T_A=25^\circ C$, $R_L=10k\Omega$, $C_L=100pF$		2.5	4		MHz
Input Resistance	R_{IN}				10^{12}		Ω
Common Mode Rejection Ratio	CMR	$R_S=50\Omega$	$T_A=25^\circ C$	70	86		dB
			$T_{MIN} \cong T_A \cong T_{MAX}$	70			dB
Supply Voltage Rejection Ratio	SVR	$R_S=50\Omega$	$T_A=25^\circ C$	70	86		dB
			$T_{MIN} \cong T_A \cong T_{MAX}$	70			dB
Supply Current	I_{CC}	No load	$T_A=25^\circ C$		1.4	2.5	mA
			$T_{MIN} \cong T_A \cong T_{MAX}$				2.5
Channel Separation	V_{O1}/V_{O2}	$G_V=100$			120		dB
Output Short-circuit Current	I_{OS}		$T_A=25^\circ C$	10	40	60	mA
			$T_{MIN} \cong T_A \cong T_{MAX}$	10		60	mA
Slew Rate	SR	$V_{IN}=10V$, $R_L=2k\Omega$, $C_L=100pF$, unity gain		6	10		V/ μs
Rise Time	t_R	$V_{IN}=20mV$, $R_L=2k\Omega$, $C_L=100pF$, unity gain			0.1		μs
Overshoot Factor	K_{OV}	$V_{IN}=20mV$, $R_L=2k\Omega$, $C_L=100pF$, unity gain			10		%
Total Harmonic Distortion	THD	$G_V=20dB$, $f=1kHz$, $R_L=2k\Omega$, $C_L=100pF$, $V_{OUT}=2V_{pp}$			0.01		%
Phase Margin	ϕ_m				45		Degrees
Equivalent Input Noise Voltage	eN	$R_S=100\Omega$, $f=1kHz$			15		$\frac{nV}{\sqrt{Hz}}$

Note: The Input bias currents are junction leakage currents, which approximately double for every 10 °C increase in the junction temperature.

■ PARAMETER MEASUREMENT INFORMATION

Figure 1. Voltage Follower

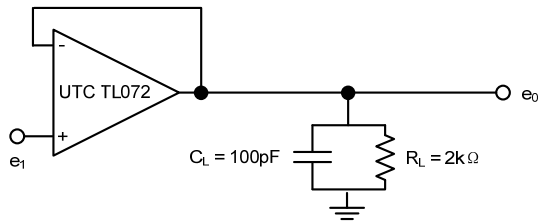
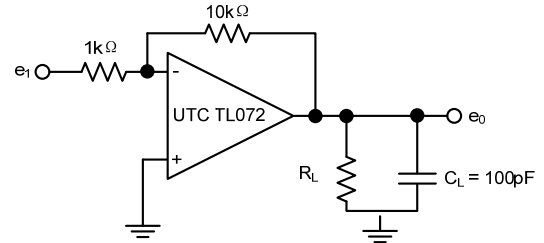
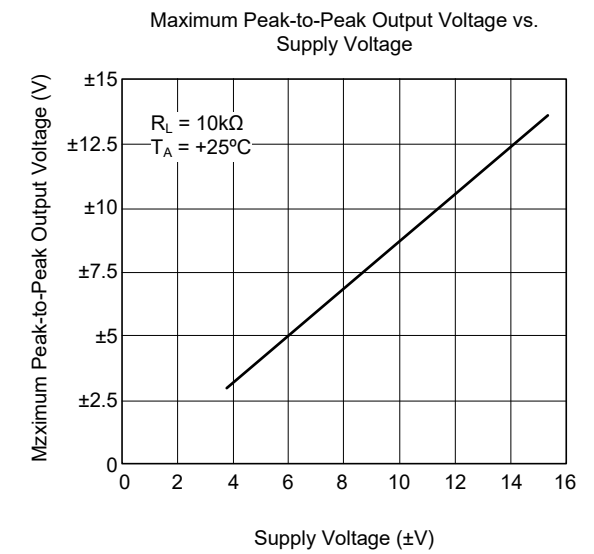
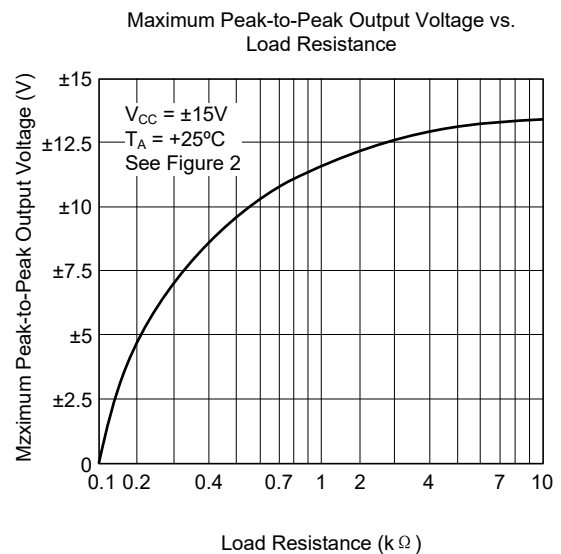
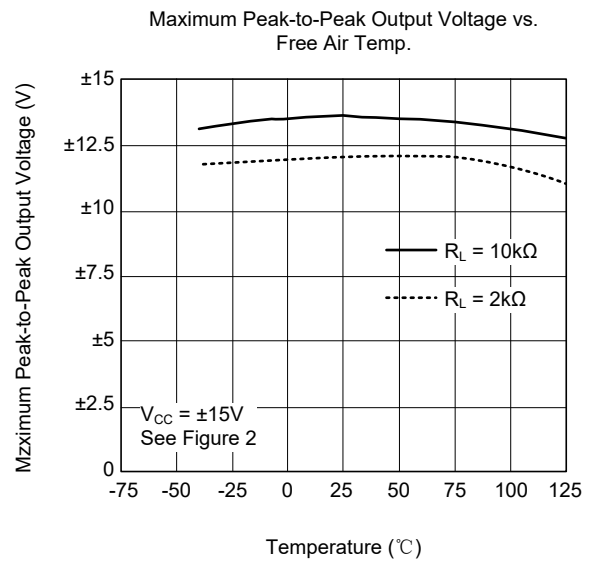
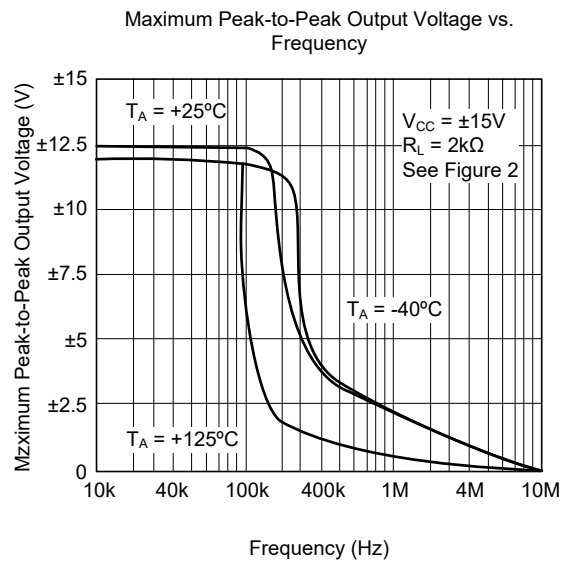
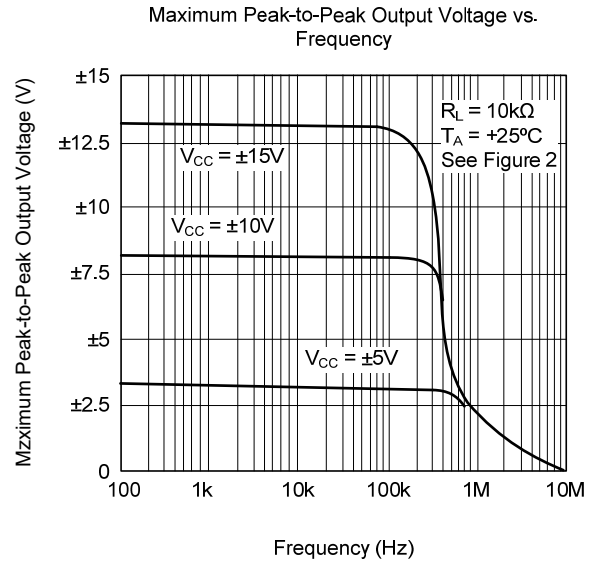
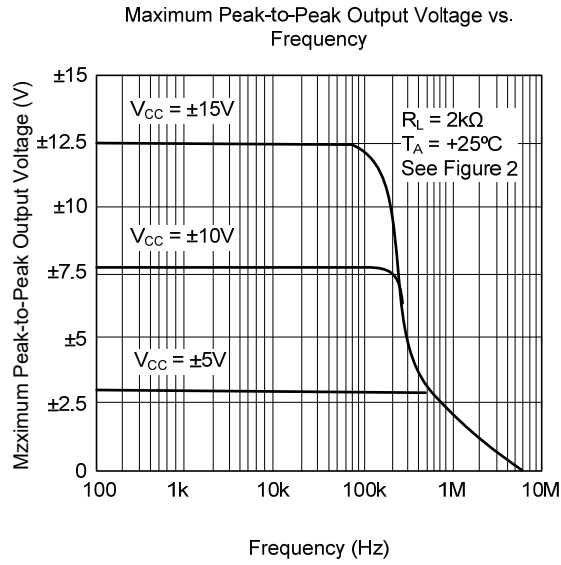


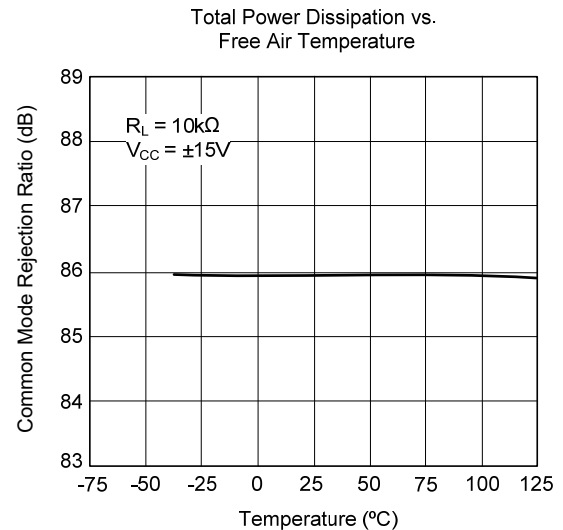
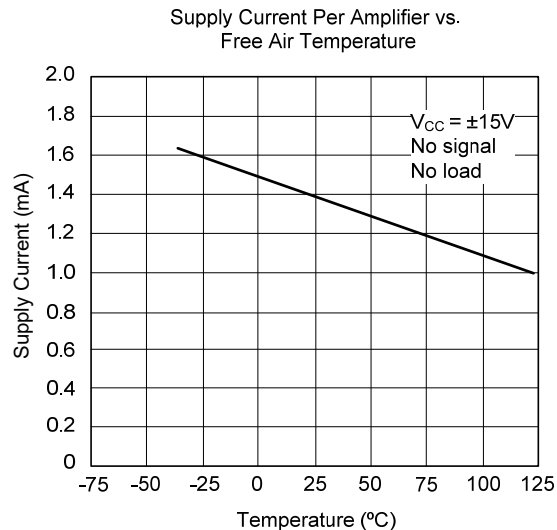
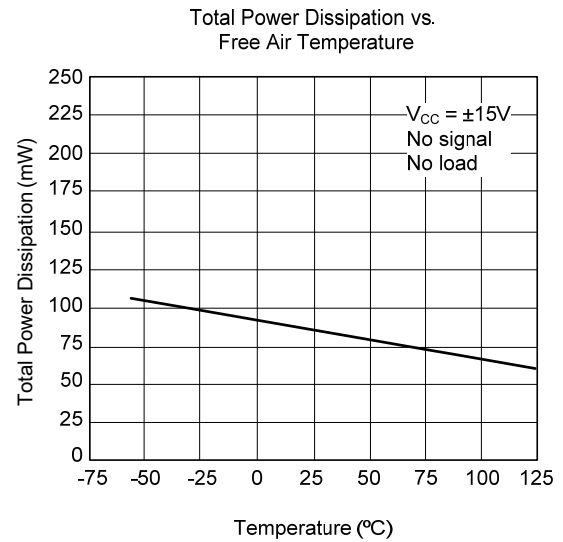
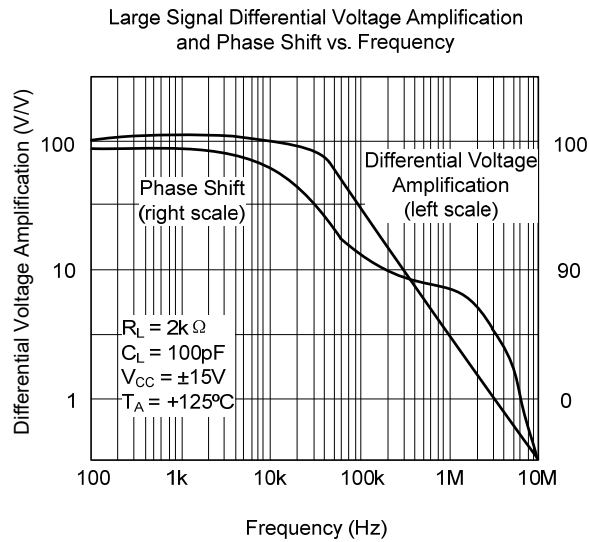
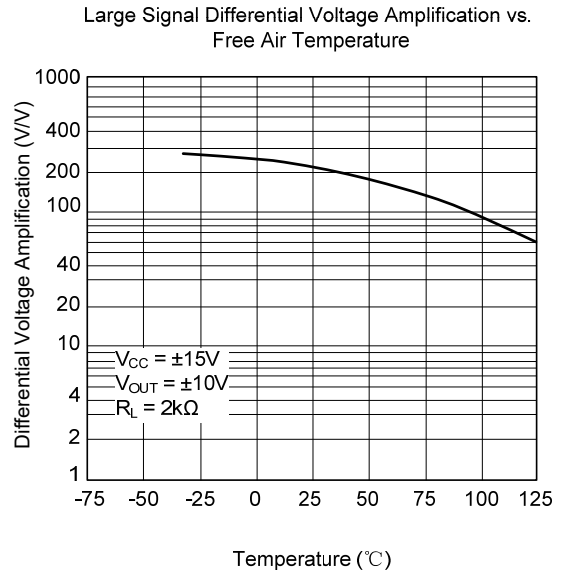
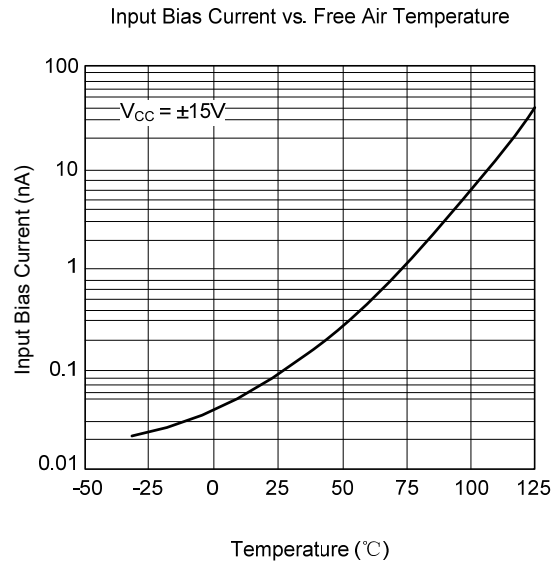
Figure 2. Gain-of-10 Inverting Amplifier



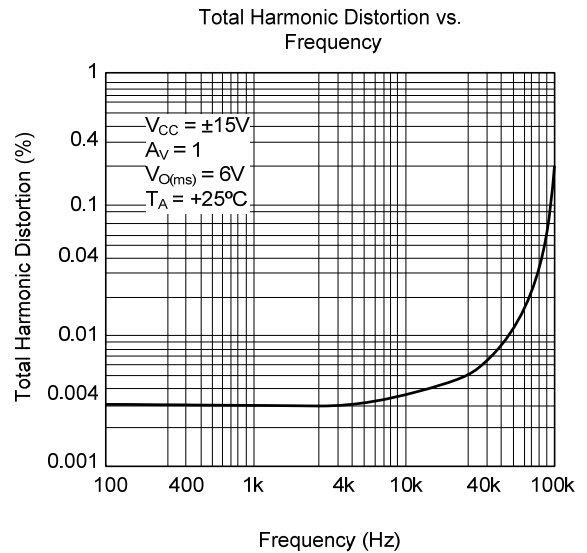
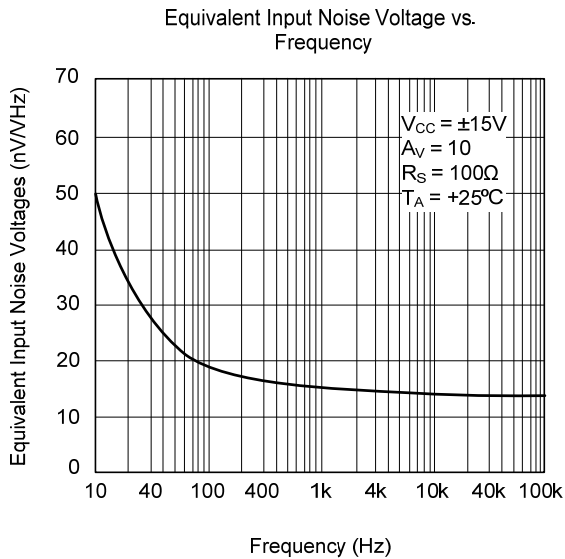
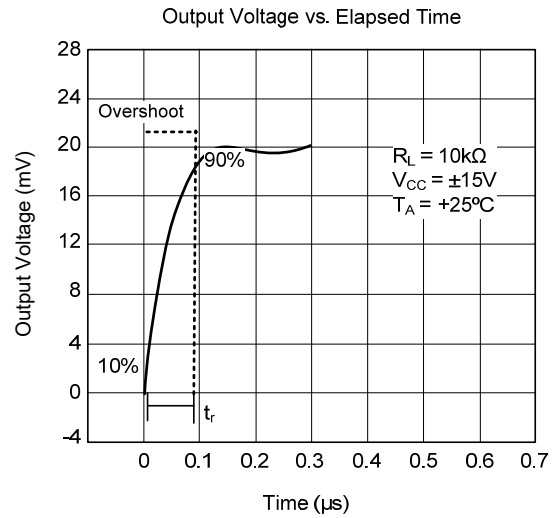
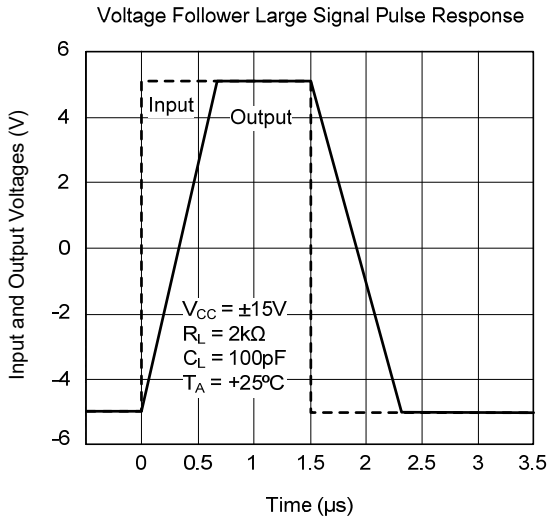
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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