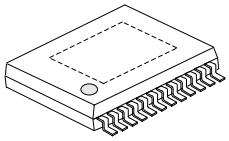
# PA3312

*CMOS IC*

# DUAL 2.6W AUDIO POWER AMPLIFIER WITH FOUR SELECTABLE GAIN SETTINGS AND INPUT-MUX CONTROL



HTSSOP-24

## ■ DESCRIPTION

The UTC **PA3312** is a monolithic integrated circuit that stereo bridged audio power amplifiers capable of producing 2.6W into 3Ω with less than 10% THD+N or 1W into 8Ω with less than 0.65% THD+N. This device minimizes the number of external components needed, simplifying the design, and freeing up board space for other features. Both of the depop circuitry and the thermal shutdown protection circuitry are integrated in UTC **PA3312**, that reduce pops and clicks noise during power up or shutdown mode operation .

Amplifier gain is internally configured and controlled by way of two terminals (GAIN0 and GAIN1). BTL gain setting of 6 dB, 10 dB, 15.6dB, 21.6dB (inverting) are provided, whereas SE gain is always configured as 4.1dB for headphone drive. A MUX control terminal (HP/$\overline{\text{LINE}}$) allows selection between the two sets of stereo input signals. To simplify the audio system design, UTC **PA3312** combines a stereo bridge-tied loads (BTL) mode for speaker drive and a stereo single-end (SE) mode for headphone drive into a single chip, where both modes are easily switched by the SE/$\overline{\text{BTL}}$ input control pin signal.

## ■ FEATURES

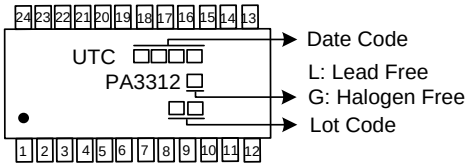
* Low operating current with 10mA
* Compatible with pc 99 desktop line-out into 10KΩ load
* Internal gain control ,which eliminates external gain-setting resistors
* 2.6w per channel output power into 3Ω at 5V , BTL mode
* Input MUX select terminal
* Pc-beep input
* Improves depop circuitry to eliminate turn-on and turn-off transients in output
* Fully differential input

## ■ ORDERING INFORMATION

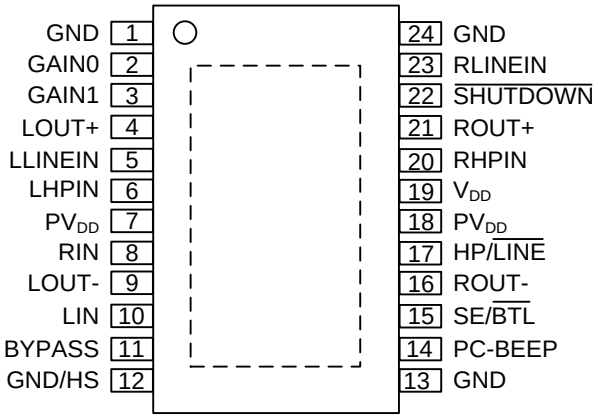
| Ordering Number | | Package | Packing |
|---|---|---|---|
| Lead Free | Halogen Free | | |
| PA3312L-N24-R | PA3312G-N24-R | HTSSOP-24 | Tape Reel |

| | |
|---|---|
| PA3312G-N24-R<br>(1)Packing Type<br>(2)Package Type<br>(3)Green Package | (1) R: Tape Reel<br>(2) N24: HTSSOP-24<br>(3) G: Halogen Free and Lead Free, Lead Free |

## ■ MARKING



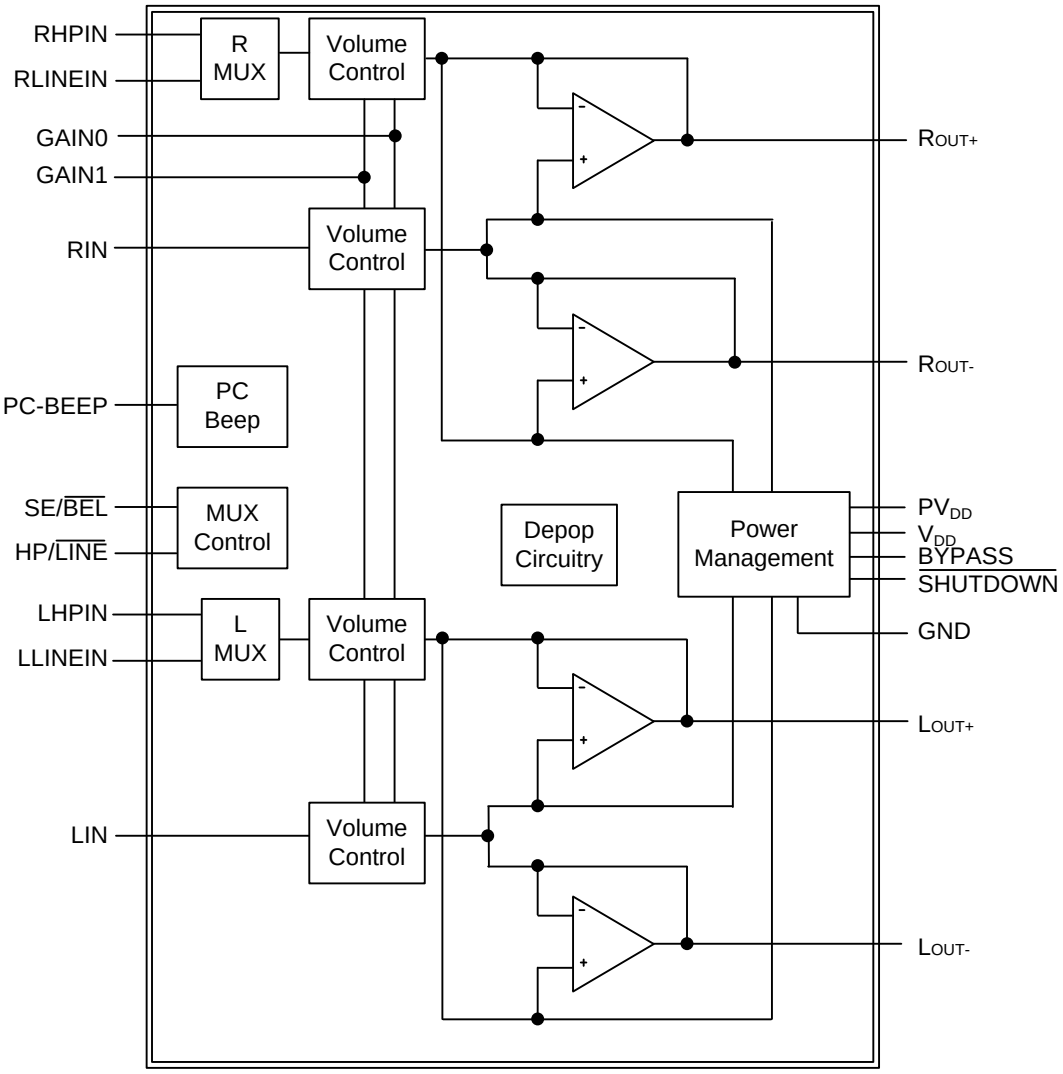
## ■ PIN CONFIGURATION




## ■ PIN DESCRIPTION

| PIN NO | PIN NAME | I/O | DESCRIPTION |
|---|---|---|---|
| 1, 12, 13, 24 | GND | | Ground connection for circuitry. Connected to the thermal pad. |
| 11 | BYPASS | | Tap to voltage divider for internal mid-supply bias generator |
| 2 | GAIN0 | I | Bit 0 of gain control |
| 3 | GANIN1 | I | Bit 1 of gain control |
| 5 | LLINEIN | I | Left-channel line input, selected when SE/$\overline{BTL}$ is held low |
| 6 | LHPIN | I | Left-channel headphone input, selected when SE/$\overline{BTL}$ is held high |
| 7, 18 | $PV_{DD}$ | I | Power supply for output stage |
| 8 | RIN | I | Common right input for fully differential input. AC ground for single-ended inputs. |
| 10 | LIN | I | Common left input for fully differential input. AC ground for single-ended inputs. |
| 14 | PC-BEEP | I | For PC Beep mode. PC-BEEP is enabled when a > 1.5-V (peak-to-peak) square wave is input |
| 17 | HP/$\overline{LINE}$ | I | HP/$\overline{LINE}$ is the input MUX control input. When the HP/LINE terminal is held high, the headphone inputs (LHPIN or RHPIN [6, 20]) are active. When the HP/$\overline{LINE}$ terminal is held low, the line inputs (LLINEIN or RLINEIN [5, 23]) are active. |
| 15 | SE/$\overline{BTL}$ | I | Hold SE/$\overline{BTL}$ low for BTL mode and hold high for SE mode. |
| 19 | $V_{DD}$ | I | Analog $V_{DD}$ input supply. This terminal needs to be isolated from $PV_{DD}$ to achieve highest performance. |
| 20 | RHPIN | I | Right-channel headphone input, selected when SE/$\overline{BTL}$ is held high |
| 23 | RLINEIN | I | Right-channel line input, selected when SE/$\overline{BTL}$ is held low |
| 22 | $\overline{SHUTDOWN}$ | I | Places entire IC in shutdown mode when held low, except PC-BEEP remains active |
| 4 | $L_{OUT+}$ | O | Left-channel positive output in BTL mode and positive output in SE mode |
| 9 | $L_{OUT-}$ | O | Left-channel negative output in BTL mode and high-impedance in SE mode |
| 21 | $R_{OUT+}$ | O | Right-channel positive output in BTL mode and positive output in SE mode |
| 16 | $R_{OUT-}$ | O | Right-channel negative output in BTL mode and high-impedance in SE mode |

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATING

Over operating free-air temperature range (unless otherwise specified)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 6 | V |
| Input Voltage | $V_{IN}$ | -0.3~$V_{DD}$ ~+0.3 | V |
| Power Dissipation | $P_D$ | Internally limited | |
| Junction Temperature | $T_J$ | +150 | °C |
| Operating Junction Temperature | $T_{OPR}$ | -40 ~ +85 | °C |
| Storage Temperature | $T_{STG}$ | -55 ~ +150 | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 4.5 | 5.5 | V |
| High-Level Input Voltage | $V_{IH}$ | SE/$\overline{BTL}$, HP/$\overline{LINE}$, GAIN0, GAIN1 | 0.8×$V_{DD}$ | | V |
| | | $\overline{SHUTDOWN}$ | 2 | | |
| Low-Level Input Voltage | $V_{IL}$ | SE/$\overline{BTL}$, HP/$\overline{LINE}$ | | 0.6×$V_{DD}$ | V |
| | | GAIN0, GAIN1 | | 0.4×$V_{DD}$ | |
| | | $\overline{SHUTDOWN}$ | | 0.8 | |
| Operating Free-Air Temperature | $T_A$ | | -40 | 85 | °C |

## ■ OPERATING CHARACTERISTICS ($V_{DD}$ = 5 V, $T_A$ = 25°C, $R_L$ = 8Ω , Gain = 6 dB, BTL mode)

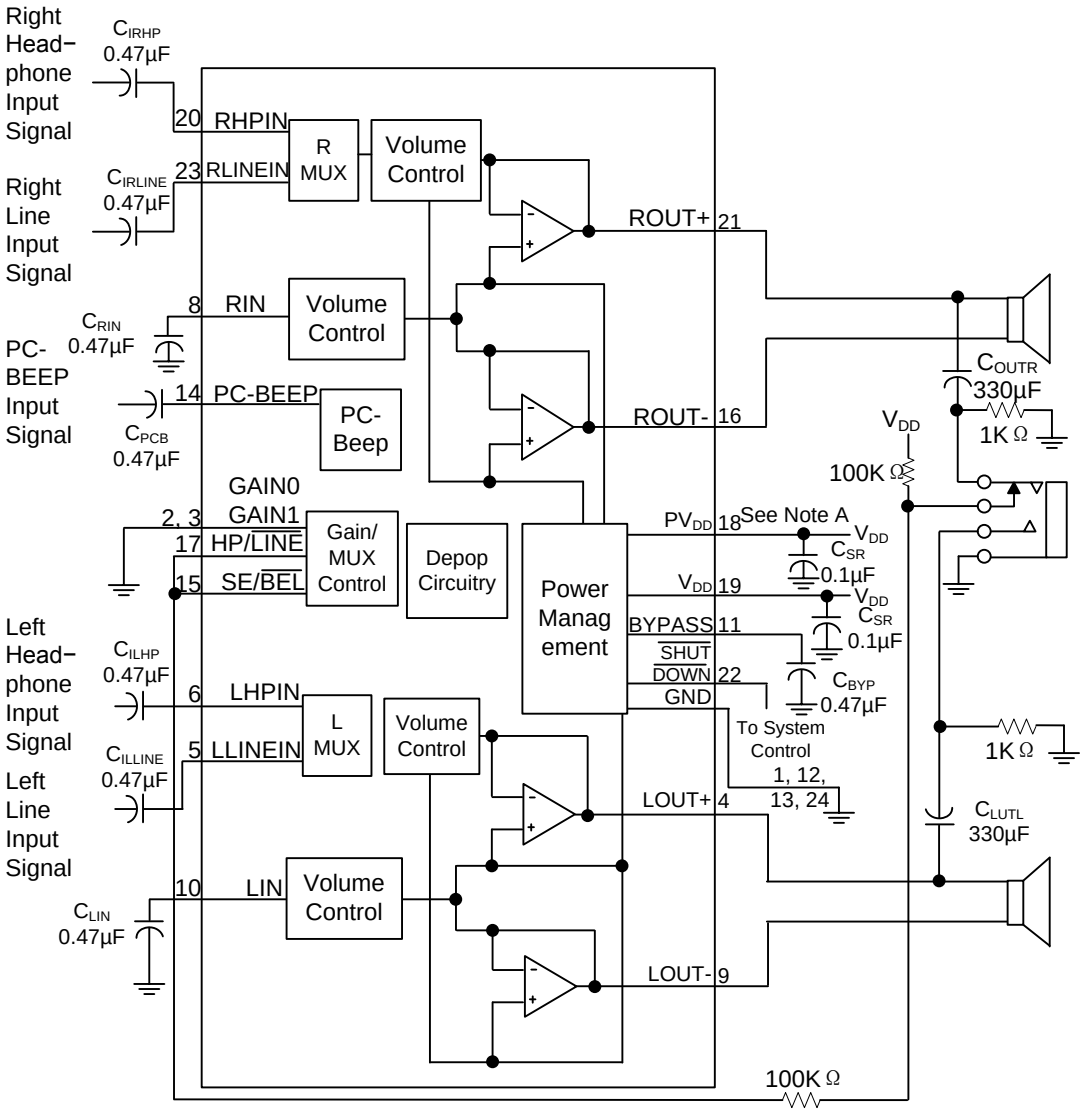
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Output Power | $P_{OUT}$ | $R_L$ = 3Ω | THD+N=10% | | 2.6 | | W |
| | | | THD+N=1% | | 2.05 | | |
| Total Harmonic Distortion Plus Noise | TDH+N | $P_{OUT}$ = 1 W, f = 20 Hz ~ 15 kHz | | | 0.65% | | |
| Maximum Output Power Bandwidth | $B_{OM}$ | THD = 5% | | | >15 | | KHz |
| Supply Ripple Rejection Ratio | RR | f = 1 kHz, $C_B$ = 0.47 μF | BTLmode | | 72 | | dB |
| Signal-to-Noise Ratio | SNR | | | | 105 | | dB |
| Noise Output Voltage | eN | $C_B$=0.47μF, f=20Hz ~ 20KHz | BTLmode | | 20 | | $\mu V_{RMS}$ |
| | | | SE mode | | 18 | | |

## ■ ELECTRICAL CHARACTERISTICS

($T_A$ = 25°C, $V_{DD}$ = 5 V, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Output Offset Voltage (Measured Differentially) | $\|V_{O(OFF)}\|$ | $V_{IN}$ = 0, $A_V$ = 6 dB | | | 25 | mV |
| Power Supply Rejection Ratio | PSRR | $V_{DD}$ = 4.5 V ~ 5.5 V | | 77 | | dB |
| High-Level Input Current | $\|I_{IH}\|$ | $V_{DD}$ = 5.5 V, $V_{IN}$ = $V_{DD}$ | | | 1 | μA |
| Low-Level Input Current | $\|I_{IL}\|$ | $V_{DD}$ = 5.5 V, $V_{IN}$ = 0 V | | | 1 | μA |
| Supply Current | $I_{DD}$ | BTL mode | | 6 | 10 | mA |
| | | SE mode | | 3 | 5 | |
| Supply Current, Shutdown Mode | $I_{DD(SD)}$ | | | 150 | 300 | μA |

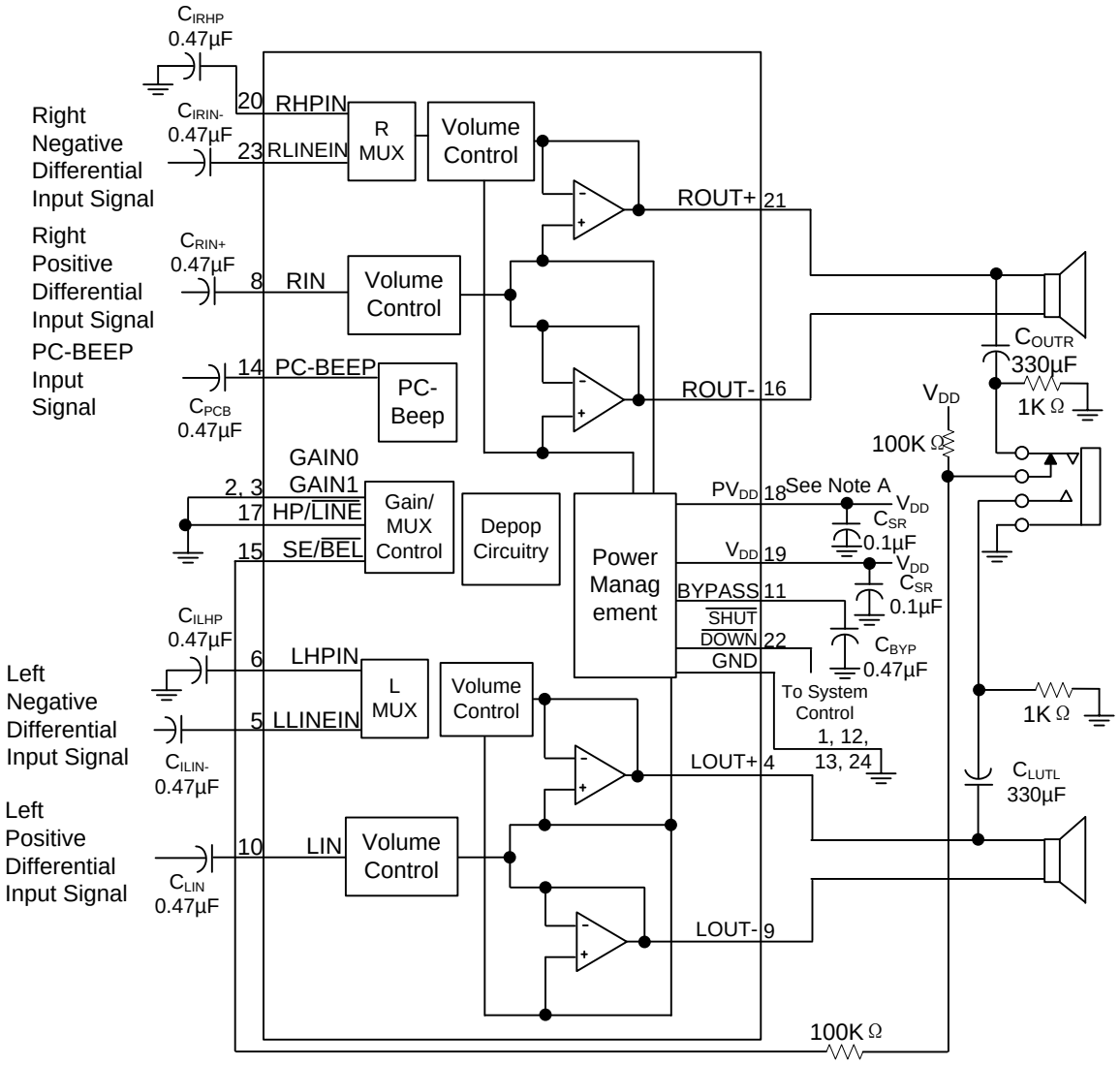
## ■ TYPICAL APPLICATION CIRCUIT




A. A 0.1-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Typical PA3312 Application Circuit Using Single-Ended Inputs and Input MUX

## ■ TYPICAL APPLICATION CIRCUIT (Cont.)

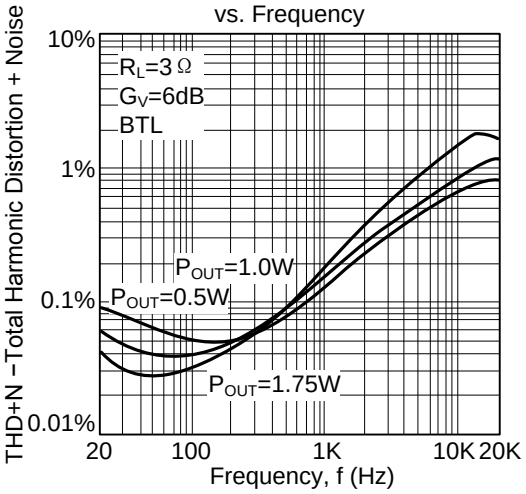



A. A 0.1-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

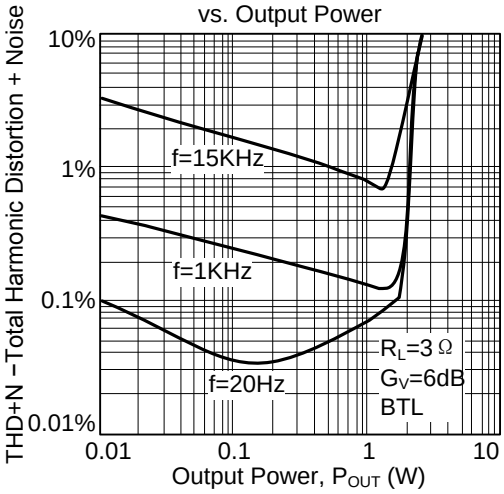
Typical PA3312 Application Circuit Using Differential Inputs

## ■ TYPICAL CHARACTERISTICS

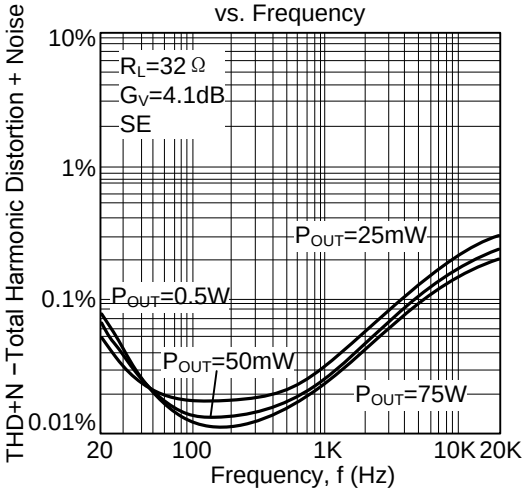
Total Harmonic Distortion Plus Noise vs. Frequency



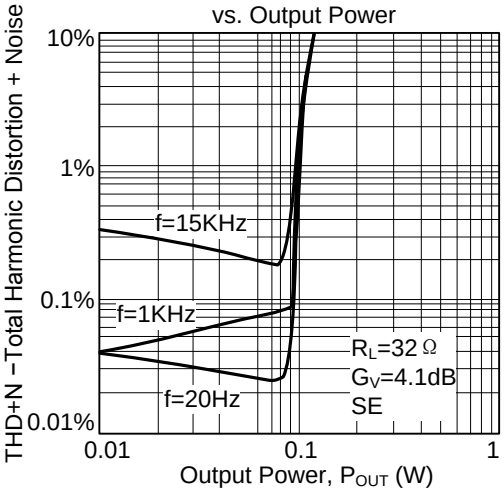

Total Harmonic Distortion Plus Noise vs. Output Power



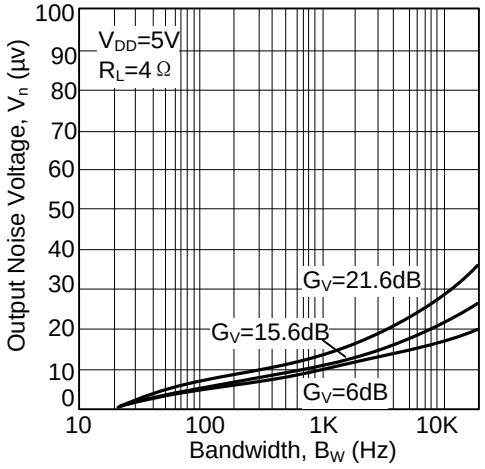

Total Harmonic Distortion Plus Noise vs. Frequency



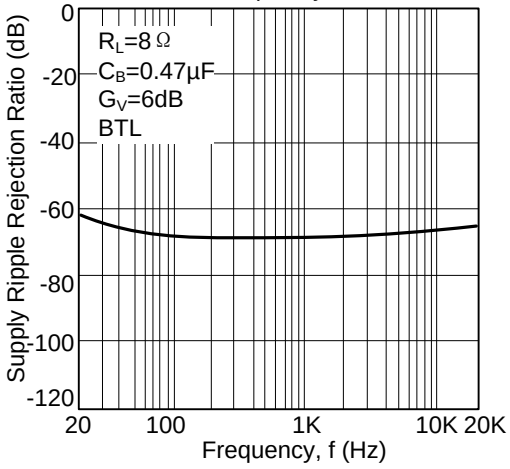

Total Harmonic Distortion Plus Noise vs. Output Power




Output Noise Voltage vs. Bandwidth

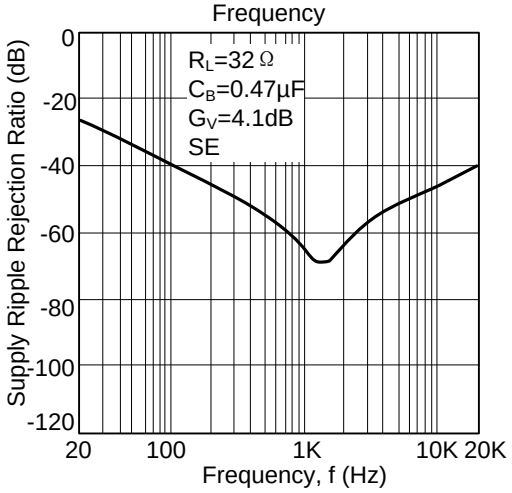



Supply Ripple Rejection Ratio vs. Frequency

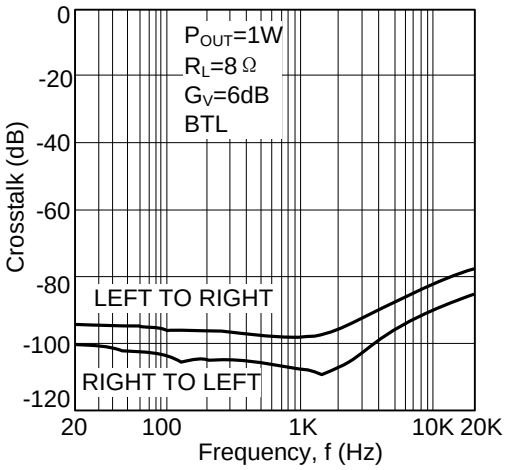


## ■ TYPICAL CHARACTERISTICS (Cont.)

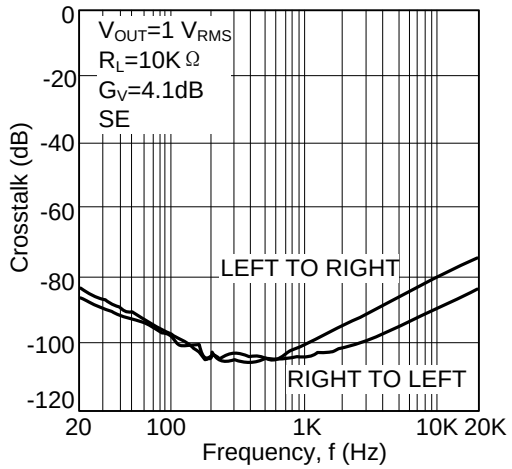
Supply Ripple Rejection Ratio vs. Frequency



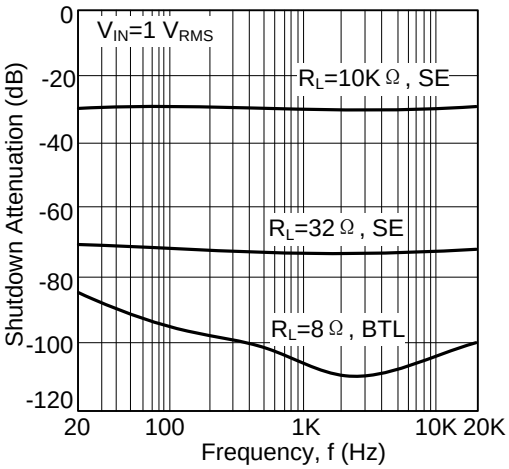

Crosstalk vs. Frequency



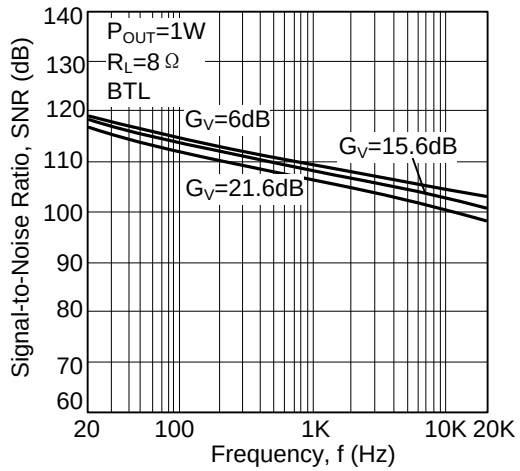

Crosstalk vs. Frequency



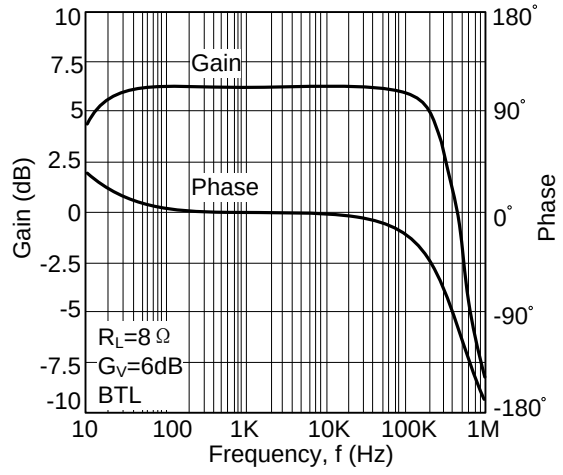

Shutdown Attenuation vs. Frequency




Signal-to-Noise Ratio vs. Frequency

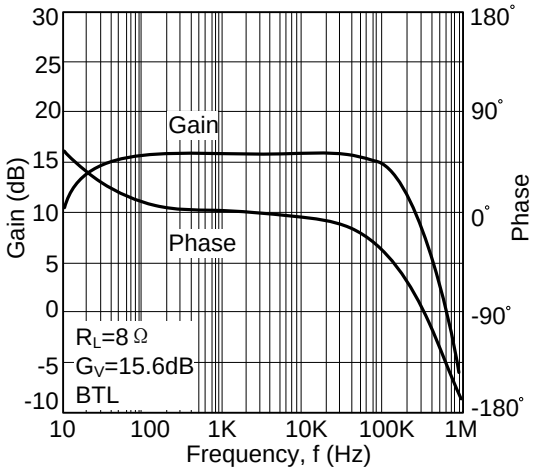



Closed-Loop Response

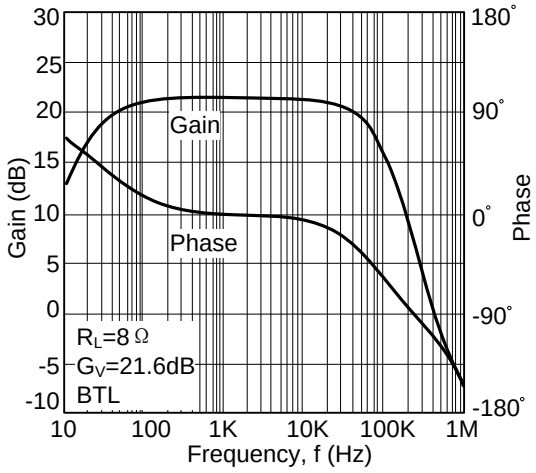


## ■ TYPICAL CHARACTERISTICS (Cont.)

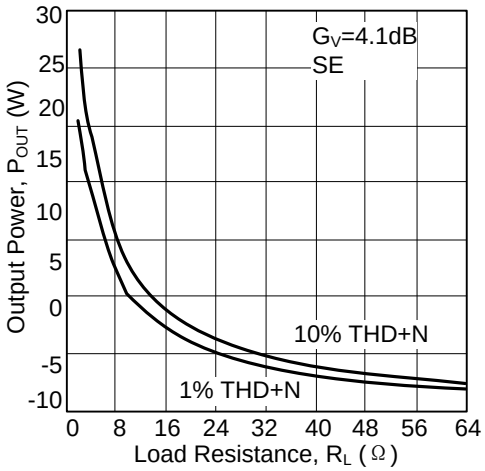
Closed-Loop Response



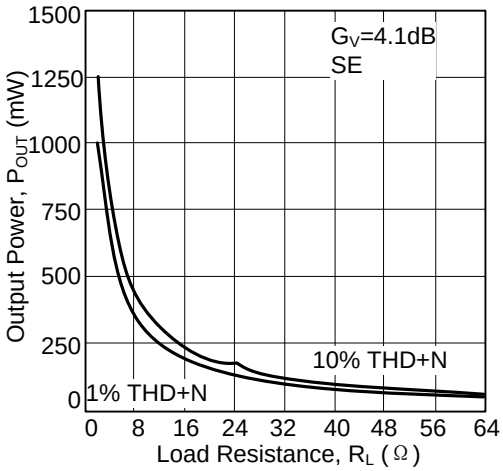

Closed-Loop Response



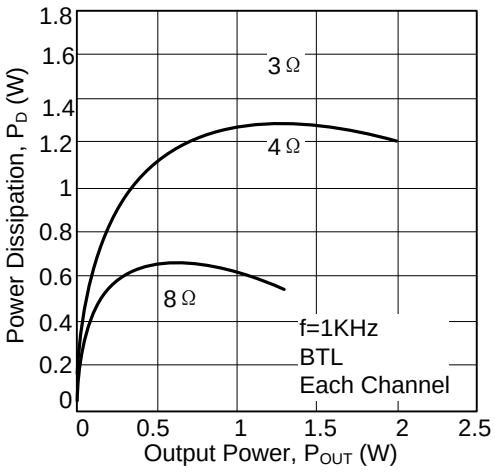

Output Power vs. Load Resistance




Output Power vs. Load Resistance




Power Dissipation vs. Output Power




Power Dissipation vs. Output Power