



U74LVC1G126

CMOS IC

BUS BUFFER/LINE DRIVER; 3-STATE

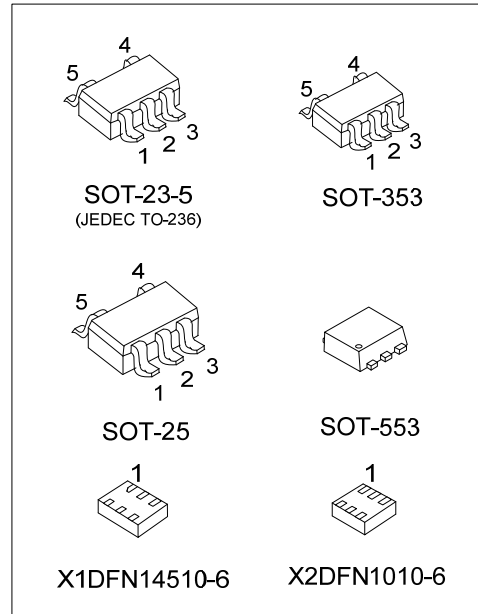
DESCRIPTION

The **U74LVC1G126** is single bus buffer/line driver with 3-state output. The output is disabled When the output enable (OE) is low. When OE is high, true data is will pass A input to the Y output.

This device has power-down protective circuit preventing device from destruction when it is powered down.

FEATURES

- * Operate From 1.65V to 5.5V
- * Inputs Accept Voltages to 5.5V
- * High Noise Immunity
- * Low Power Dissipation
- * Direct Interface With TTL level



ORDERING INFORMATION

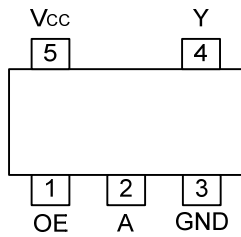
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC1G126L-AE5-R	U74LVC1G126G-AE5-R	SOT-23-5	Tape Reel
U74LVC1G126L-AF5-R	U74LVC1G126G-AF5-R	SOT-25	Tape Reel
U74LVC1G126L-AL5-R	U74LVC1G126G-AL5-R	SOT-353	Tape Reel
U74LVC1G126L-AN5-R	U74LVC1G126G-AN5-R	SOT-553	Tape Reel
U74LVC1G126L-KAP-R	U74LVC1G126G-KAP-R	X1DFN14510-6	Tape Reel
U74LVC1G126L-K06-1010X2-R	U74LVC1G126G-K06-1010X2-R	X2DFN1010-6	Tape Reel

<p>U74LVC1G126G-AE5-R</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) R: Tape Reel (2) AE5: SOT-23-5, AF5: SOT-25, AL5: SOT-353 AN5: SOT-553, KAP: X1DFN14510-6 K06-1010X2: X2DFN1010-6 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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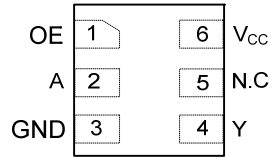
MARKING

SOT-23-5 / SOT-25 / SOT-353 / SOT-553	X1DFN14510-6 / X2DFN1010-6
<p>L: Lead Free G: Halogen Free</p>	<p>L: Lead Free G: Halogen Free</p>

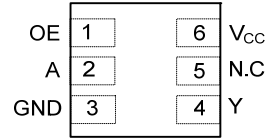
■ PIN CONFIGURATION



SOT-23-5 / SOT-25
SOT-353 / SOT-553



X1DFN14510-6
(TOP VIEW)



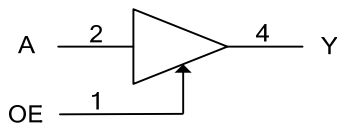
X2DFN1010-6
(TOP VIEW)

■ FUNCTION TABLE

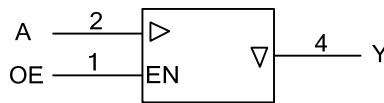
INPUT(OE)	INPUT(A)	OUTPUT(Y)
H	L	L
H	H	H
L	X	Z

Note: H: HIGH voltage level; L: LOW voltage level; X=don't care; Z=high-impedance OFF-state.

■ LOGIC DIAGRAM (Positive Logic)



Logic Symbol



IEC Logic Symbol

■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{CC}	-0.5 ~ +6.5	V
Input Voltage		V_{IN}	-0.5 ~ +6.5	V
Output Voltage	Enable mode	V_{OUT}	-0.5 ~ $V_{CC} + 0.5$	V
	Disable mode		-0.5 ~ +6.5	V
	Power-down mode		-0.5 ~ +6.5	V
V_{CC} or GND Current		I_{CC}	±100	mA
Continuous Output Current ($V_{OUT}=0$ to V_{CC})		I_{OUT}	±50	mA
Input Clamp Current ($V_{IN}<0$)		I_{IK}	-50	mA
Output Clamp Current ($V_{OUT}>V_{CC}$ or $V_{OUT}<0$)		I_{OK}	-50	mA
Power Dissipation ($T_A=-40^{\circ}C \sim +125^{\circ}C$)	SOT-23-5	P_D	300	mW
	SOT-25		360	mW
	SOT-353		250	mW
	SOT-553		210	mW
	X1DFN14510-6		200	mW
	X2DFN1010-6			
Storage Temperature		T_{STG}	-65 ~ +150	$^{\circ}C$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		5.5	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}	$V_{CC}=1.65V \sim 5.5V$; Enable mode	0		V_{CC}	V
		$V_{CC}=1.65V \sim 5.5V$; Disable mode	0		5.5	V
		$V_{CC}=0V$; Power-Down Mode	0		5.5	V
Input Transition Rise or Fall Rate	t_R / t_F	$V_{CC}=1.65V \sim 2.7V$			20	ns/V
		$V_{CC}=2.7V \sim 5.5V$			10	ns/V
Operating Temperature	T_A		-40		+125	$^{\circ}C$

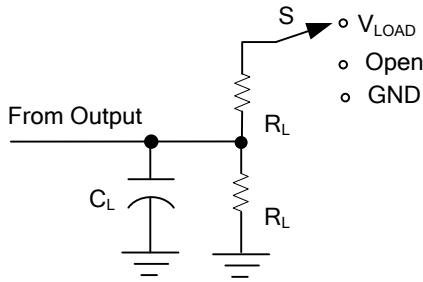
■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-Level Input Voltage	V _{IH}	V _{CC} =1.65V ~ 1.95V	0.65× V _{CC}			0.65× V _{CC}			V
		V _{CC} =2.3V ~ 2.7V	1.7			1.7			V
		V _{CC} =2.7V ~ 3.6V	2			2			V
		V _{CC} =4.5V ~ 5.5V	0.7× V _{CC}			0.7× V _{CC}			V
Low-Level Input Voltage	V _{IL}	V _{CC} =1.65V ~ 1.95V			0.35× V _{CC}			0.35× V _{CC}	V
		V _{CC} =2.3V ~ 2.7V			0.7			0.7	V
		V _{CC} =2.7V ~ 3.6V			0.8			0.8	V
		V _{CC} =4.5V ~ 5.5V			0.3× V _{CC}			0.3× V _{CC}	V
High-Level Output Voltage	V _{OH}	V _{CC} =1.65 ~ 5.5V, I _{OH} =-100μA	V _{CC} - 0.1			V _{CC} - 0.1			V
		V _{CC} =1.65V, I _{OH} =-4mA	1.2			0.95			V
		V _{CC} =2.3V, I _{OH} =-8mA	1.9			1.7			V
		V _{CC} =2.7V, I _{OH} =-12mA	2.2			1.9			V
		V _{CC} =3.0V, I _{OH} =-24mA	2.3			2.0			V
		V _{CC} =4.5V, I _{OH} =-32mA	3.8			3.4			V
Low-Level Output Voltage	V _{OL}	V _{CC} =1.65 ~ 5.5V, I _{OL} =100μA			0.1			0.1	V
		V _{CC} =1.65V, I _{OL} =4mA			0.45			0.7	V
		V _{CC} =2.3V, I _{OL} =8mA			0.3			0.45	V
		V _{CC} =2.7V, I _{OL} =12mA			0.4			0.6	V
		V _{CC} =3.0V, I _{OL} =24mA			0.55			0.8	V
		V _{CC} =4.5V, I _{OL} =32mA			0.55			0.8	V
Input Leakage Current	I _{I(LEAK)}	V _{CC} =5.5V, V _{IN} =5.5V or GND		±0.1	±5			±5	μA
Power OFF Leakage Current	I _{OFF}	V _{CC} =0V, V _{IN} or V _{OUT} =5.5V		±0.1	±10			±10	μA
3-State Output OFF-State Current	I _{OZ}	V _{CC} =5.5V V _{IN} =V _{IH} or V _{IL} , V _{OUT} =V _{CC} or GND		±0.1	±10			±10	μA
Quiescent Supply Current	I _{CC}	V _{CC} =5.5V, V _{IN} =V _{CC} or GND, I _{OUT} =0		0.1	10			10	μA
Additional Quiescent Supply Current Per Input Pin	ΔI _{CC}	V _{CC} =2.3 ~ 5.5V, V _{IN} =V _{CC} -0.6V, I _{OUT} =0		5	500			500	μA

■ SWITCHING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40°C~+125°C			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
Propagation Delay From Input (A) to Output (Y)	t _{PLH} / t _{PHL}	C _L =30pF	V _{CC} =1.8±0.15V, R _L =1KΩ	1.0		16			20	ns
			V _{CC} =2.5±0.2V, R _L =500Ω	0.5		10			14	ns
		C _L =50pF, R _L =500Ω	V _{CC} =2.7V	0.5		10			14	ns
			V _{CC} =3.3±0.3V	0.5		7			11	ns
			V _{CC} =5±0.5V	0.5		5			9	ns
3-State Output Enable Time From Input (OE) to Output (Y)	t _{PZH} / t _{PZL}	C _L =30pF	V _{CC} =1.8±0.15V, R _L =1KΩ	1.0		18			22	ns
			V _{CC} =2.5±0.2V, R _L =500Ω	0.5		11			14	ns
		C _L =50pF, R _L =500Ω	V _{CC} =2.7V	0.5		11			14	ns
			V _{CC} =3.3±0.3V	0.5		7			11	ns
			V _{CC} =5±0.5V	0.5		6			9	ns
3-State Output Disable Time From Input (OE) to Output (Y)	t _{PLZ} / t _{PHZ}	C _L =30pF	V _{CC} =1.8±0.15V, R _L =1KΩ	1.0		10			13	ns
			V _{CC} =2.5±0.2V, R _L =500Ω	0.5		7			10	ns
		C _L =50pF, R _L =500Ω	V _{CC} =2.7V	0.5		7			9	ns
			V _{CC} =3.3±0.3V	0.5		6			8	ns
			V _{CC} =5±0.5V	0.5		5			7	ns

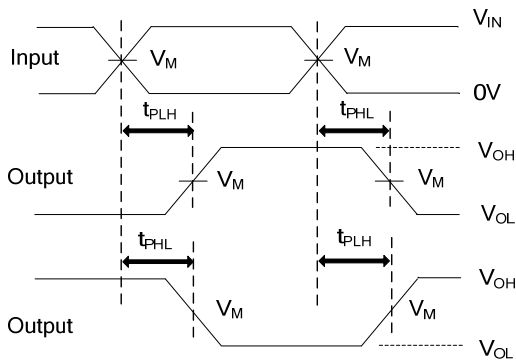
TEST CIRCUIT AND WAVEFORMS



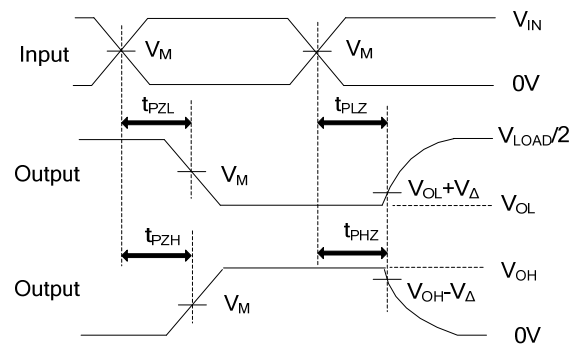
TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{LOAD}

TEST CIRCUIT

V_{CC}	INPUTS		V_M	V_{LOAD}	V_{Δ}	C_L	R_L
	V_{IN}	t_R, t_F					
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	0.15V	30pF	1K Ω
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	0.15V	30pF	500 Ω
2.7V	2.7V	$\leq 2.5ns$	1.5V	6V	0.3V	50pF	500 Ω
$3.3V \pm 0.3V$	2.7V	$\leq 2.5ns$	1.5V	6V	0.3V	50pF	500 Ω
$5V \pm 0.5V$	V_{CC}	$\leq 2.5ns$	$V_{CC}/2$	$2 \times V_{CC}$	0.3V	50pF	500 Ω



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: $P_{RR} \leq 10MHz$, $Z_o = 50\Omega$.

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