



U74AC00

CMOS IC

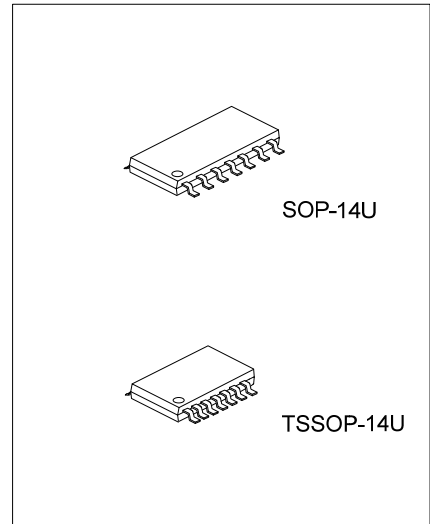
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

DESCRIPTION

The UTC **U74AC00** contains four independent 2-input NAND gates, and those gates perform the Boolean function of $Y = \overline{A \times B}$ or $Y = \overline{A + B}$ in positive logic.

FEATURES

- * Operation voltage range: 2V ~ 6V
- * Low power dissipation: $I_{CC} = 2\mu A$ (Max.)
- * High speed: $t_{PD} = 7ns$ (Typ.) @ 5.0V
- * Low input current: 0.1 μA (Max) @ 25°C

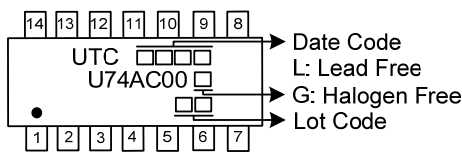


ORDERING INFORMATION

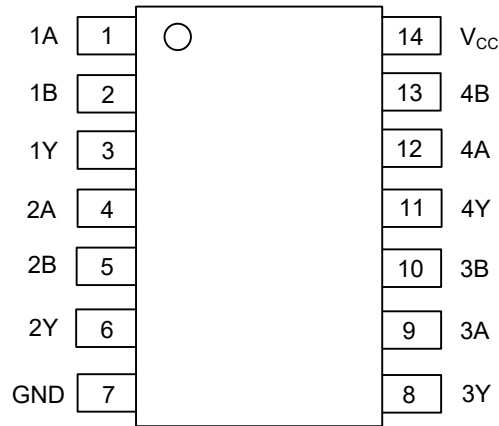
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AC00L-UEA-R	U74AC00G-UEA-R	SOP-14U	Tape Reel
U74AC00L-UEB-R	U74AC00G-UEB-R	TSSOP-14U	Tape Reel

<p>U74AC00G-UEA-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) UEA: SOP-14U, UEB: TSSOP-14U (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



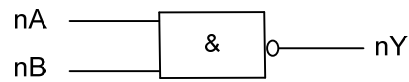
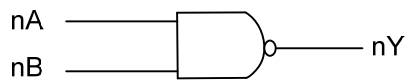
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT(A)	INPUT(B)	OUTPUT(Y)
H	H	L
H	L	H
L	H	H
L	L	H

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	-0.5 ~ 7	V
Input Voltage	V _{IN}	-0.5 ~ V _{CC} +0.5	V
Output Voltage	V _{OUT}	-0.5 ~ V _{CC} +0.5	V
Input Clamp Current	I _{IK}	±20	mA
Output Clamp Current	I _{OK}	±20	mA
Output Current	I _{OUT}	±50	mA
V _{CC} or GND Current	I _{CC}	±200	mA
Storage Temperature	T _{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}	2		6	V
Input Voltage	V _{IN}	0		V _{CC}	V
Output Voltage	V _{OUT}	0		V _{CC}	V
Input Transition Rise or Fall Rate	Δt/Δv			8	ns/V
Operating Temperature	T _A	-40		+125	°C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Case	SOP-14U	125	°C/W
	TSSOP-14U	150	°C/W

■ STATIC CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V _{IH}	V _{CC} =3V	2.1			V
		V _{CC} =4.5V	3.15			V
		V _{CC} =5.5V	3.85			V
Low-Level Input Voltage	V _{IL}	V _{CC} =3V			0.9	V
		V _{CC} =4.5V			1.35	V
		V _{CC} =5.5V			1.65	V
High-Level Output Voltage	V _{OH}	V _{CC} =3V, I _{OH} =-50μA	2.9			V
		V _{CC} =4.5V, I _{OH} =-50μA	4.4			V
		V _{CC} =5.5V, I _{OH} =-50μA	5.4			V
		V _{CC} =3V, I _{OH} =-12mA	2.56			V
		V _{CC} =4.5V, I _{OH} =-24mA	3.86			V
		V _{CC} =5.5V, I _{OH} =-24mA	4.86			V
Low-Level Output Voltage	V _{OL}	V _{CC} =3V, I _{OL} =50μA		0.002	0.1	V
		V _{CC} =4.5V, I _{OL} =50μA		0.001	0.1	V
		V _{CC} =5.5V, I _{OL} =50μA		0.001	0.1	V
		V _{CC} =3V, I _{OL} =12mA			0.36	V
		V _{CC} =4.5V, I _{OL} =24mA			0.36	V
		V _{CC} =5.5V, I _{OL} =24mA			0.36	V
		V _{CC} =5.5V, I _{OL} =75mA(Note)			1.65	V
Input Leakage Current	I _{I(LEAK)}	V _{CC} =5.5V, V _{IN} =V _{CC} or GND			0.1	μA
Quiescent Supply Current	I _Q	V _{CC} =5.5V, V _{IN} =V _{CC} or GND, I _{OUT} =0			2	μA
Input Capacitance	C _{IN}	V _{CC} =5V, V _{IN} =V _{CC} or GND		2.6		pF

Note: Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

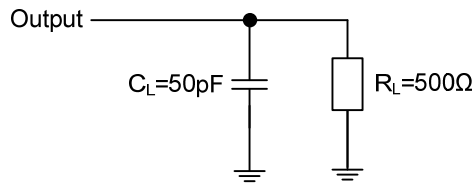
■ DYNAMIC CHARACTERISTICS (Input: $t_R=t_F=2.5\text{ns}$, $T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from Input (A or B) to Output (Y)	t_{PLH}	$V_{CC}=3.3V\pm 0.3V$, $C_L=50\text{pf}$, $R_L=500\Omega$	2	7	9.5	ns
		$V_{CC}=5V\pm 0.5V$, $C_L=50\text{pF}$, $R_L=500\Omega$	1.5	6	8	ns
	t_{PHL}	$V_{CC}=3.3V\pm 0.3V$, $C_L=50\text{pf}$, $R_L=500\Omega$	1.5	5.5	8	ns
		$V_{CC}=5V\pm 0.5V$, $C_L=50\text{pF}$, $R_L=500\Omega$	1.5	4.5	6.5	ns

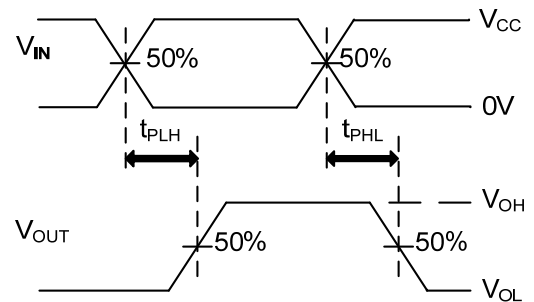
■ OPERATING CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	$C_L=50\text{pF}$, $f=1\text{MHz}$		40		pF

■ TEST CIRCUIT AND WAVEFORMS



Definitions for test circuit



Propagation Delay Times

Note: C_L includes probe and jig capacitance.
 $PRR \leq 1\text{MHz}$, $Z_0 = 50\Omega$, $t_r \leq 2.5\text{ns}$, $t_f \leq 2.5\text{ns}$.

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