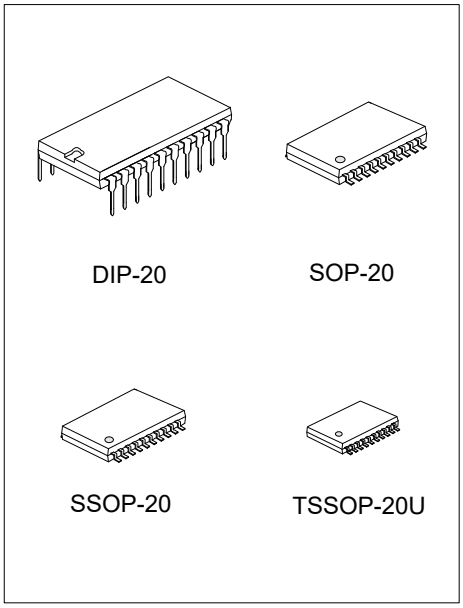
U74HC574

CMOS IC

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS



■ DESCRIPTION

The **U74HC574** is a octal edge-triggered D-type flip-flops with 3-state outputs, and it has 8 channels.

■ FEATURES

* Operate from 2V to 6V
* Max t_{pd} of 66ns at 4.5 V
* Typical V_{OL}< 0.17V at V_{CC}=4.5V, T_A=25°C
* Typical V_{OH}> 4.3V at V_{CC}=4.5V, T_A=25°C

■ ORDERING INFORMATION

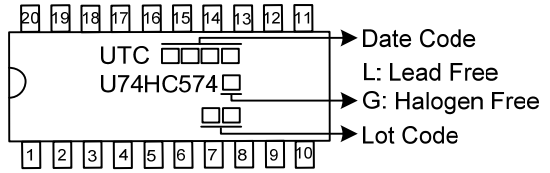
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC574L-D20-T	U74HC574G-D20-T	DIP-20	Tube
U74HC574L-S20-R	U74HC574G-S20-R	SOP-20	Tape Reel
U74HC574L-R20-R	U74HC574G-R20-R	SSOP-20	Tape Reel
U74HC574L-ULA-R	U74HC574G-ULA-R	TSSOP-20U	Tape Reel

U74HC574G-D20-T
(1)Packing Type
(2)Package Type
(3)Green Package

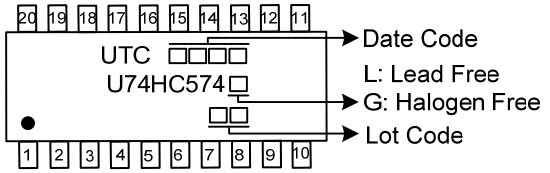
(1) T: Tube, R: Tape Reel
(2) D20: DIP-20, S20: SOP-20, R20: SSOP-20, ULA: TSSOP-20U
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

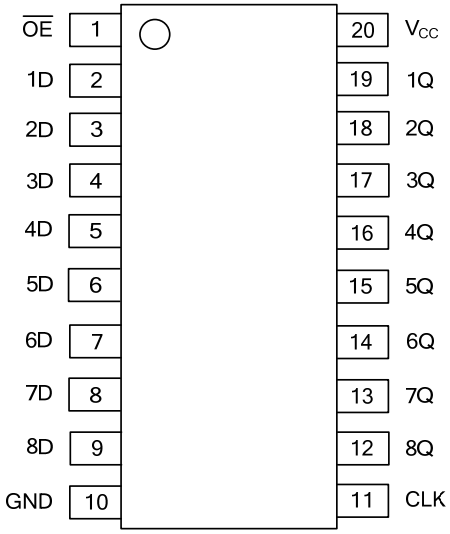
DIP-20



SOP-20 / SSOP-20 / TSSOP-20U



■ PIN CONFIGURATION

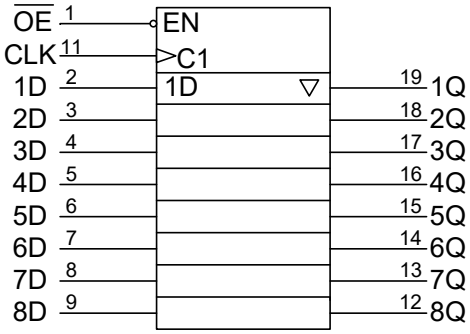


■ FUNCTION TABLE

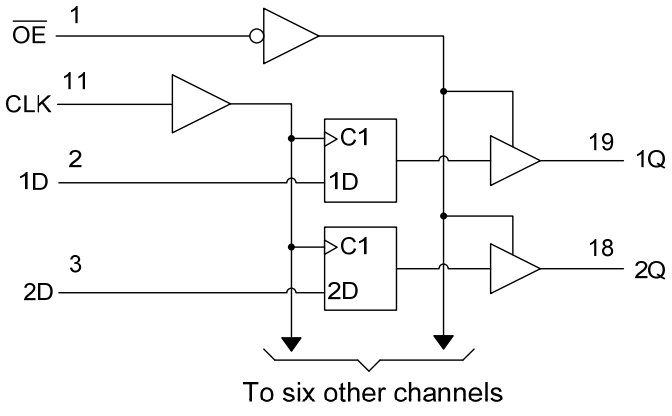
INPUTS($\overline{OE}$)	INPUTS(CLK)	INPUTS(D)	OUTPUT(Q)
L	↑	H	H
L	↑	L	L
L	L /H	X	Q_0
H	X	X	Z

Note: H: HIGH voltage level; L: LOW voltage level.

■ LOGIC SYMBOL



■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ +7	V
V_{CC} or GND Current	I_{CC}	±70	mA
Output Current	I_{OUT}	±35	mA
Input Clamp Current	I_{IK}	±20	mA
Output Clamp Current	I_{OK}	±20	mA
Storage Temperature	T_{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2	5	6	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}	High or low state	0		V_{CC}	V
Input Rise or Fall Times	t_R, t_F	V_{CC}=2.0V	0		1	μs
		V_{CC}=4.5V	0		0.5	μs
		V_{CC}=6.0V	0		0.4	μs
Operating Temperature	T_A		-40		+125	°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	DIP-20	θ_{JA}	90	°C/W
	SOP-20		115	°C/W
	SSOP-20		130	°C/W
	TSSOP-20U		135	°C/W

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-level Input Voltage	V_{IH}	V_{CC}=2.0V	1.5			1.5			V
		V_{CC}=4.5V	3.15			3.15			V
		V_{CC}=6.0V	4.2			4.2			V
Low-level Input Voltage	V_{IL}	V_{CC}=2.0V			0.5			0.5	V
		V_{CC}=4.5V			1.35			1.35	V
		V_{CC}=6.0V			1.8			1.8	V
Output Voltage High-Level	V_{OH}	V_{CC}=2.0V, I_{OH}=-20μA	1.9	1.998		1.9			V
		V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.499		4.4			V
		V_{CC}=6.0V, I_{OH}=-20μA	5.9	5.999		5.9			V
		V_{CC}=4.5V, I_{OH}=-6mA	3.98	4.3		3.7			V
		V_{CC}=6.0V, I_{OH}=-7.8mA	5.48	5.8		5.2			V
Output Voltage Low-Level	V_{OL}	V_{CC}=2.0V, I_{OL}=20μA		0.002	0.1			0.1	V
		V_{CC}=4.5V, I_{OL}=20μA		0.001	0.1			0.1	V
		V_{CC}=6.0V, I_{OL}=20μA		0.001	0.1			0.1	V
		V_{CC}=4.5V, I_{OL}=6mA		0.17	0.26			0.4	V
		V_{CC}=6.0V, I_{OL}=7.8mA		0.15	0.26			0.4	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=6.0V, V_{IN}=V_{CC} or GND		±0.1	±100			±1000	nA
Disable Output Leakage Current	I_{OZ}	V_{CC}=6.0V, V_{OUT}=V_{CC} or GND		±0.01	±0.5			±10	μA
Quiescent Supply Current	I_Q	V_{CC}=6.0V, V_{IN}=V_{CC} or GND, I_{OUT}=0			8			160	μA

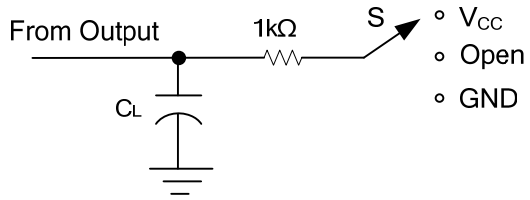
■ SWITCHING CHARACTERISTICS (See TEST CIRCUIT AND WAVEFORMS)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation delay from input (CLK) to output (Q)	t_{PLH}/t_{PHL}	V_{CC}=2.0V, C_L=50pF		90	180			225	ns
		V_{CC}=4.5V, C_L=50pF		28	36			45	ns
		V_{CC}=6.0V, C_L=50pF		24	31			38	ns
		V_{CC}=2.0V, C_L=150pF		105	265			330	ns
		V_{CC}=4.5V, C_L=150pF		36	53			66	ns
		V_{CC}=6.0V, C_L=150pF		31	46			57	ns
Output enable time from input ($\overline{OE}$) to output (Q)	t_{PZL}/t_{PZH}	V_{CC}=2.0V, C_L=50pF		77	150			210	ns
		V_{CC}=4.5V, C_L=50pF		26	30			42	ns
		V_{CC}=6.0V, C_L=50pF		23	26			36	ns
		V_{CC}=2.0V, C_L=150pF		95	235			315	ns
		V_{CC}=4.5V, C_L=150pF		32	47			63	ns
		V_{CC}=6.0V, C_L=150pF		28	41			55	ns
Output disable time from input ($\overline{OE}$) to output (Q)	t_{PLZ}/t_{PHZ}	V_{CC}=2.0V, C_L=50pF		52	150			190	ns
		V_{CC}=4.5V, C_L=50pF		24	30			38	ns
		V_{CC}=6.0V, C_L=50pF		22	26			32	ns
Maximum Clock Frequency	f_{MAX}	V_{CC}=2.0V, C_L=50pF	6	11		4			MHz
		V_{CC}=4.5V, C_L=50pF	30	36		20			MHz
		V_{CC}=6.0V, C_L=50pF	36	40		24			MHz
		V_{CC}=2.0V, C_L=150pF	6			4			MHz
		V_{CC}=4.5V, C_L=150pF	30			20			MHz
		V_{CC}=6.0V, C_L=150pF	36			24			MHz
Clock Frequency	f_{CLOCK}	V_{CC}=2.0V			6			4	MHz
		V_{CC}=4.5V			30			20	MHz
		V_{CC}=6.0V			38			24	MHz
Pulse Width	t_W	V_{CC}=2.0V	80			120			ns
		V_{CC}=4.5V	16			24			ns
		V_{CC}=6.0V	14			20			ns
Setup Time	t_{SU}	V_{CC}=2.0V	100			125			ns
		V_{CC}=4.5V	20			25			ns
		V_{CC}=6.0V	17			21			ns
Hold Time	t_H	V_{CC}=2.0V	5			5			ns
		V_{CC}=4.5V	5			5			ns
		V_{CC}=6.0V	5			5			ns

■ OPERATING CHARACTERISTICS (Unless otherwise specified)

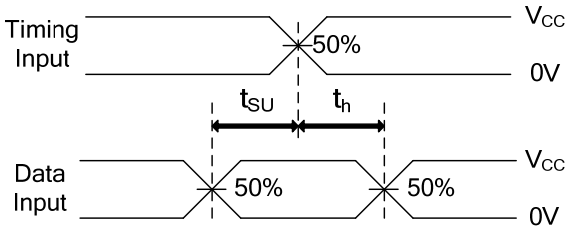
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_{IN}	V_{CC}=2.0V~ 6.0V		3	10	pF
Power Dissipation Capacitance	C_{PD}	No Load		100		pF

■ TEST CIRCUIT AND WAVEFORMS

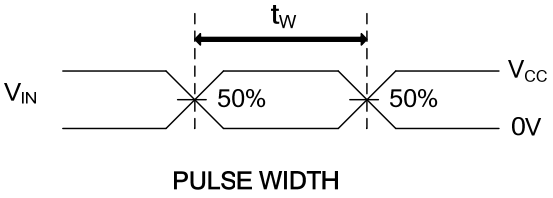


TEST CIRCUIT

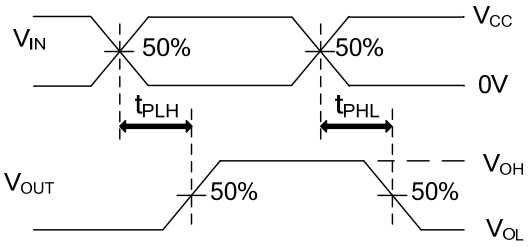
TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{CC}



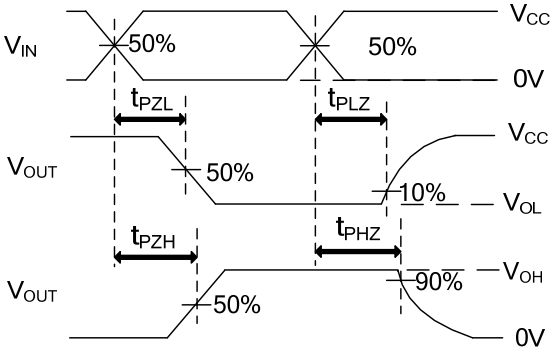
SETUP TIME AND HOLD TIME



PULSE WIDTH



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Note: C_L includes probe and jig capacitance.
PRR≦1MHz, Zo=50Ω, t_R≦6ns, t_F≦6ns.