



UT4414

Power MOSFET

N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

DESCRIPTION

The UTC **UT4414** is an N-channel enhancement mode FET with excellent trench technology to provide customers perfect $R_{DS(ON)}$ and low gate charge. The source leads are separated to allow a Kelvin connection to the source, which may be used to bypass the source inductance.

This device can be applied in a load switch or in PWM applications.

FEATURES

* $V_{DSS} = 30V$

* $I_D = 8.5A @ V_{GS} = 10V$

For SOT-23

* $R_{DS(ON)} \leq 26 m\Omega @ V_{GS} = 10V, I_D = 8.5A$

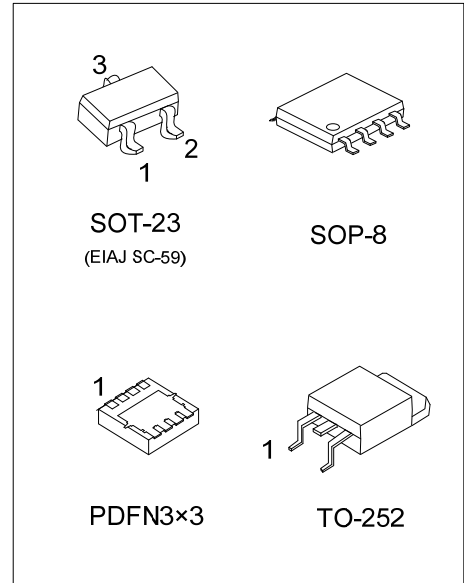
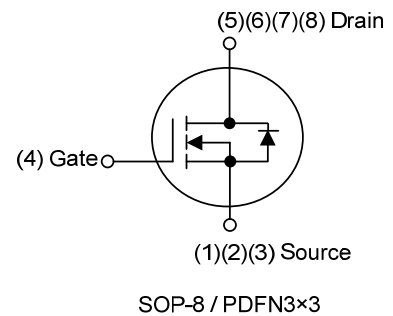
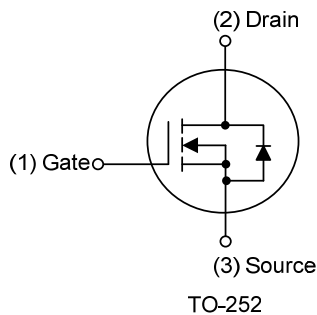
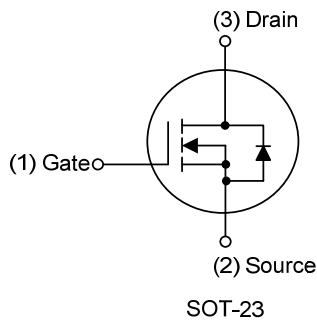
* $R_{DS(ON)} \leq 40 m\Omega @ V_{GS} = 4.5V, I_D = 5.0A$

For SOP-8/TO-252/ PDFN3x3

* $R_{DS(ON)} \leq 24 m\Omega @ V_{GS} = 10V, I_D = 8.5A$

* $R_{DS(ON)} \leq 35 m\Omega @ V_{GS} = 4.5V, I_D = 5.0A$

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT4414L-AE3-R	UT4414G-AE3-R	SOT-23	G	S	D	-	-	-	-	-	Tape Reel
UT4414L-TN3-R	UT4414G-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
UT4414L-S08-R	UT4414G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
UT4414L-P3030-R	UT4414G-P3030-R	PDFN3x3	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate S: Source D: Drain

<p>UT4414G-AE3-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) AE3: SOT-23, TN3: TO-252, S08: SOP-8 P3030: PDFN3x3 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING

SOT-23	TO-252
<p>L: Lead Free G: Halogen Free</p>	<p>UTC UT4414 Lot Code ← □ □ □ □ □ □ □ □ → Date Code 1</p>
SOP-8	PDFN3x3
<p>UTC □ □ □ □ □ □ □ □ → Date Code L: Lead Free G: Halogen Free ● □ □ □ □ □ □ □ □ → Lot Code</p>	<p>UT 4414 ● □ □ □ □ □ □ □ □ → Date Code</p>

■ ABSOLUTE MAXIMUM RATING ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain to Source Voltage		V_{DSS}	30	V
Gate to Source Voltage		V_{GSS}	± 20	V
Continuous Drain Current		I_D	8.5	A
Pulsed Drain Current		I_{DM}	50	A
Avalanche Energy (Note 3)	Single Pulsed	E_{AS}	5	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1	V/nS
Total Power Dissipation	SOT-23	P_D	0.67	W
	TO-252		2.5	W
	SOP-8		0.8	W
	PDFN3x3		1.5	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = 10.4\text{A}$, $V_{DD} = 25\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$.

4. $I_{SD} \leq 8.5\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOT-23	θ_{JA}	185	$^{\circ}\text{C}/\text{W}$
	TO-252		50	$^{\circ}\text{C}/\text{W}$
	SOP-8		156	$^{\circ}\text{C}/\text{W}$
	PDFN3x3		83.3	$^{\circ}\text{C}/\text{W}$

Notes: 1. The value of θ_{JA} is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user's specific board design.

The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

2. The θ_{JA} is the sum of the thermal impedance from junction to lead θ_{JL} and lead to ambient.

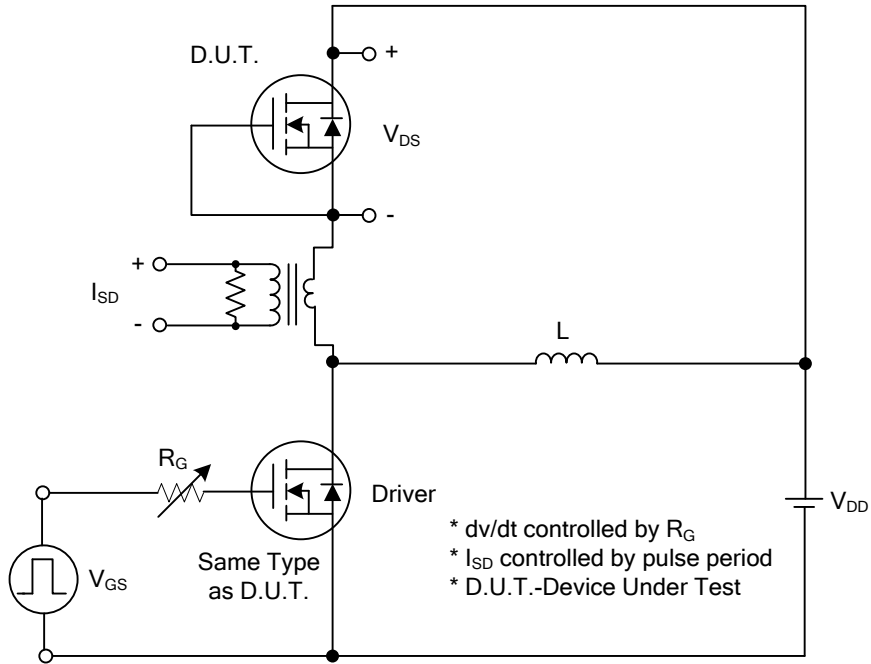
■ ELECTRICAL CHARACTERISTICS (T_J =25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =250μA	30			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =24V, V _{GS} =0V			1	μA
Gate-Source Leakage Current		I _{GSS}	V _{DS} =0V, V _{GS} =±20V			100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} = V _{GS} , I _D =250μA	1.0		3.0	V
Drain-Source On-State Resistance	SOT-23	R _{DS(ON)}	V _{GS} =10V, I _D =8.5A			26	mΩ
			V _{GS} =4.5V, I _D =5.0A			40	mΩ
	TO-252 SOP-8 PDFN3×3		V _{GS} =10V, I _D =8.5A			24	mΩ
			V _{GS} =4.5V, I _D =5.0A			35	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{DS} =15V, V _{GS} =0V, f=1MHz		292		pF
Output Capacitance		C _{OSS}			88		pF
Reverse Transfer Capacitance		C _{RSS}			71		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q _G	V _{DS} =24V, V _{GS} =10V, I _D =8.5A		19		nC
Gate-Source Charge		Q _{GS}			3.2		nC
Gate-Drain Charge		Q _{GD}			4.2		nC
Turn-ON Delay Time		t _{D(ON)}	V _{DS} =15V, V _{GS} =10V, I _D =8.5A R _G =3Ω		4		ns
Turn-ON Rise Time		t _R			15		ns
Turn-OFF Delay Time		t _{D(OFF)}			12		ns
Turn-OFF Fall Time		t _F			24		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				8.5	A
Drain-Source Diode Forward Voltage		V _{SD}	I _S =1.0A, V _{GS} =0V		0.76	1	V
Body Diode Reverse Recovery Time		t _{rr}	I _F =8.5A, dI/dt=100A/μs		244		ns
Body Diode Reverse Recovery Charge		Q _{rr}			495		nC

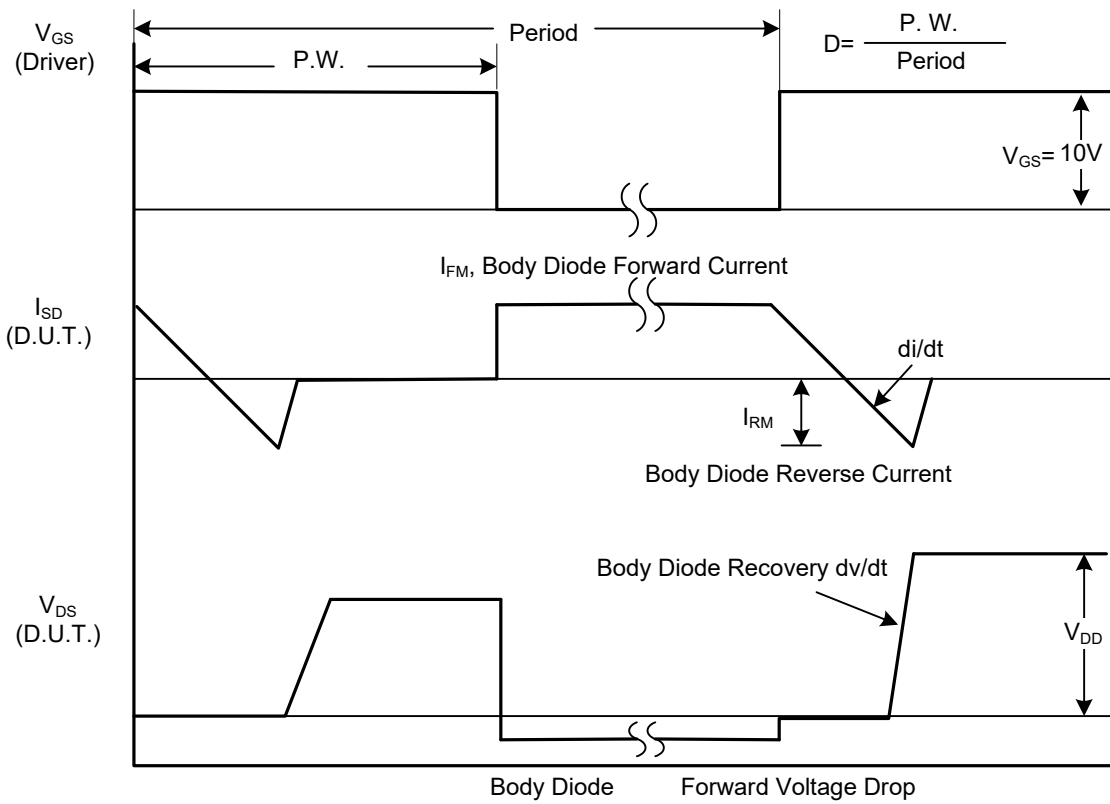
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

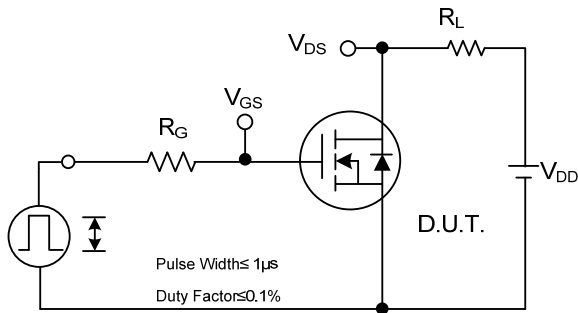


Peak Diode Recovery dv/dt Test Circuit

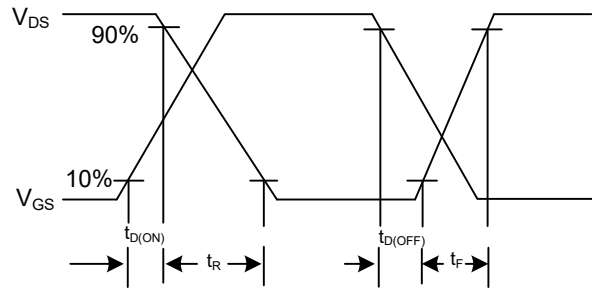


Peak Diode Recovery dv/dt Waveforms

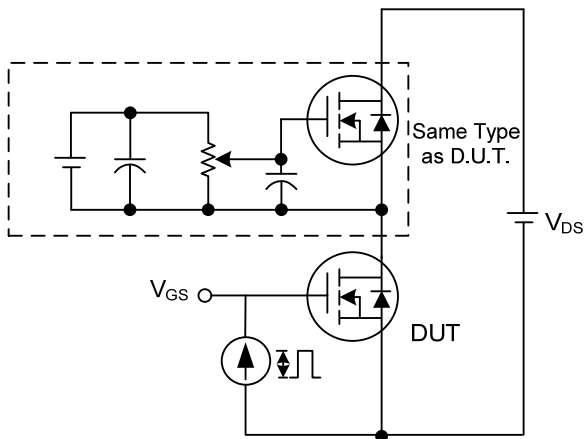
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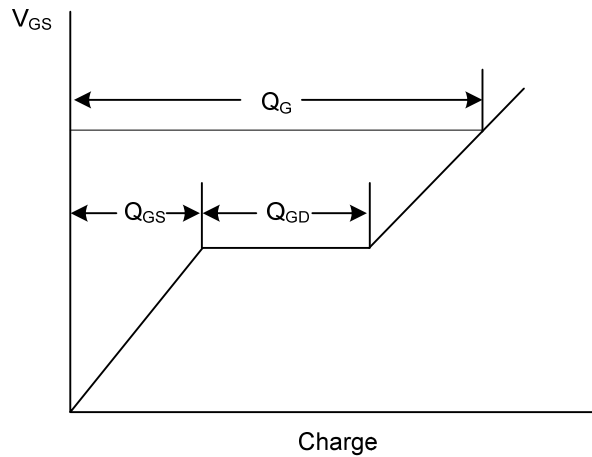
Switching Test Circuit



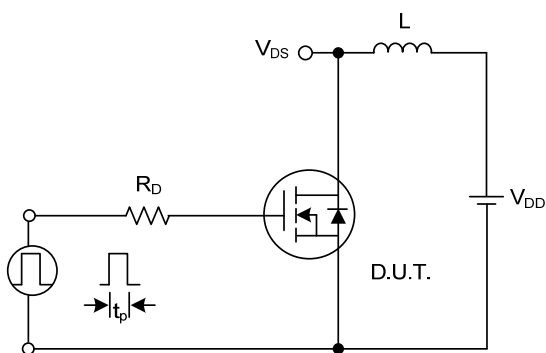
Switching Waveforms



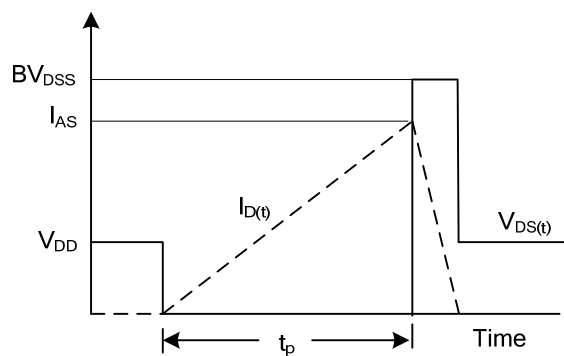
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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