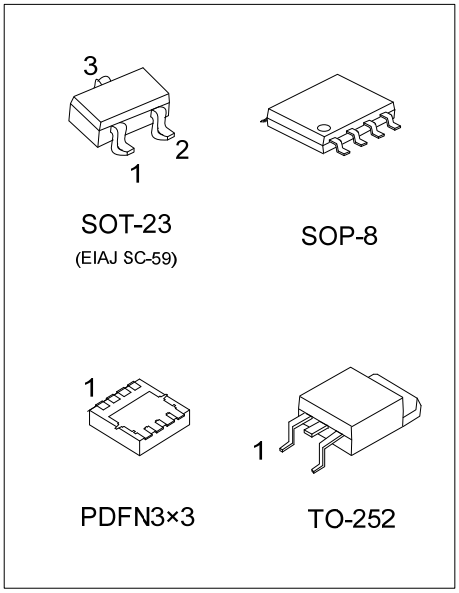
UT4414

Power MOSFET

N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR



■ DESCRIPTION

The UTC **UT4414** is an N-channel enhancement mode FET with excellent trench technology to provide customers perfect $R_{DS(ON)}$ and low gate charge. The source leads are separated to allow a Kelvin connection to the source, which may be used to bypass the source inductance.

This device can be applied in a load switch or in PWM applications.

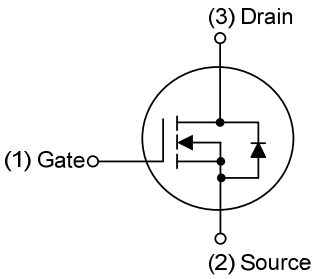
■ FEATURES

* V_{DSS} = 30V
* I_D=8.5A @ V_{GS}=10V

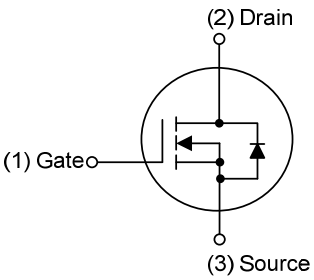
For SOT-23
* $R_{DS(ON)}$ ≤ 26 mΩ @ V_{GS}=10V,I_D=8.5A
* $R_{DS(ON)}$ ≤ 40 mΩ @ V_{GS}=4.5V, I_D=5.0A

For SOP-8/TO-252/ PDFN3×3
* $R_{DS(ON)}$ ≤ 24 mΩ @ V_{GS}=10V,I_D=8.5A
* $R_{DS(ON)}$ ≤ 35 mΩ @ V_{GS}=4.5V, I_D=5.0A

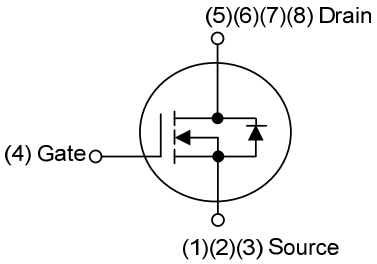
■ SYMBOL



SOT-23



TO-252

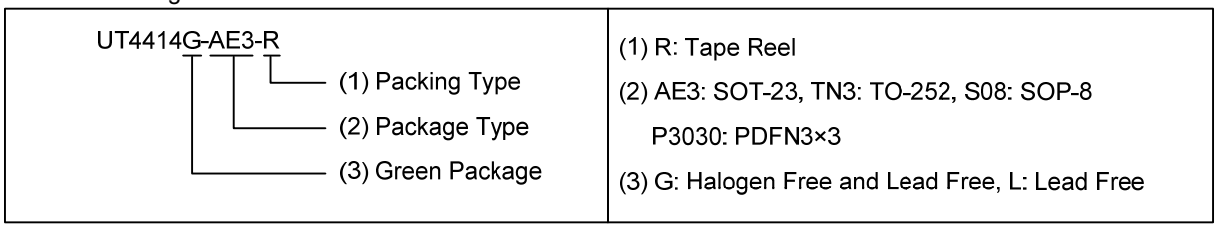


SOP-8 / PDFN3×3

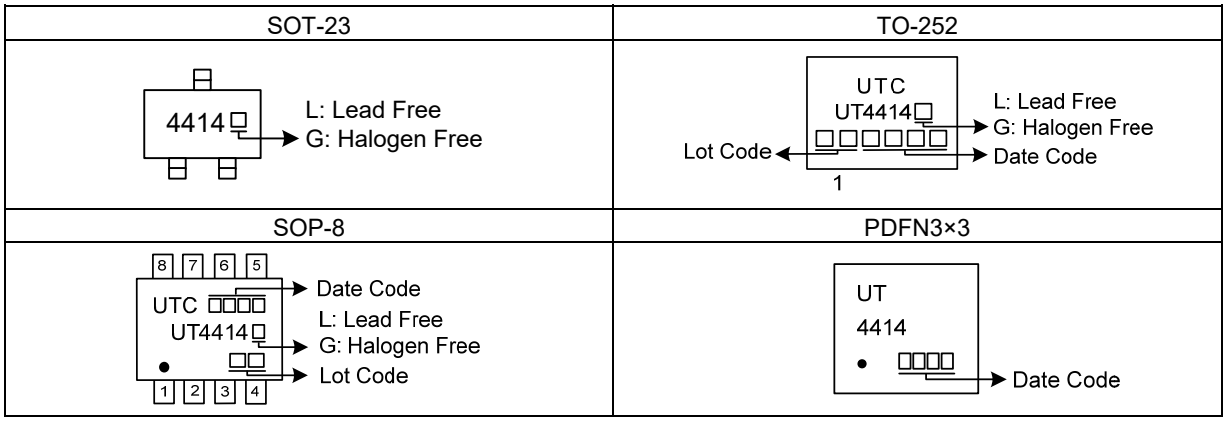
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT4414L-AE3-R	UT4414G-AE3-R	SOT-23	G	S	D	-	-	-	-	-	Tape Reel
UT4414L-TN3-R	UT4414G-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
UT4414L-S08-R	UT4414G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
UT4414L-P3030-R	UT4414G-P3030-R	PDFN3×3	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate S: Source D: Drain



■ MARKING



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain to Source Voltage		V_{DSS}	30	V
Gate to Source Voltage		V_{GSS}	±20	V
Continuous Drain Current		I_D	8.5	A
Pulsed Drain Current		I_{DM}	50	A
Avalanche Energy (Note 3)	Single Pulsed	E_{AS}	5	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1	V/nS
Total Power Dissipation	SOT-23	P_D	0.67	W
	TO-252		2.5	W
	SOP-8		0.8	W
	PDFN3×3		1.5	W
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. L = 0.1mH, I_{AS} = 10.4A, V_{DD} = 25V, R_G = 25Ω, Starting T_J = 25°C.
4. I_{SD} ≤ 8.5A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOT-23	θ_{JA}	185	°C/W
	TO-252		50	°C/W
	SOP-8		156	°C/W
	PDFN3×3		83.3	°C/W

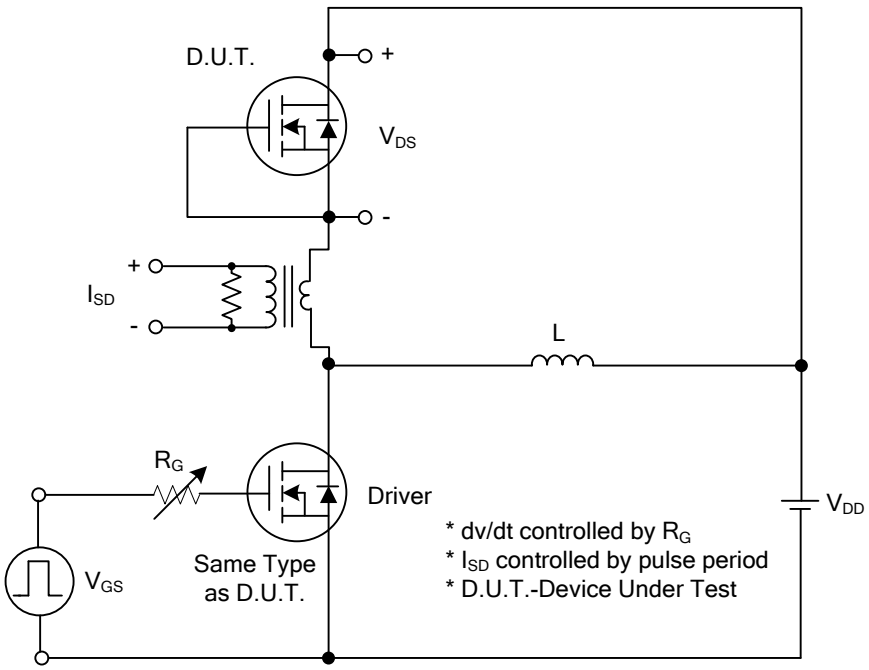
Notes: 1. The value of θ_{JA} is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific boar design. The current rating is based on the t ≤ 10s thermal resistance rating.
2. The θ_{JA} is the sum of the thermal impedance from junction to lead θ_{JL} and lead to ambient.

■ ELECTRICAL CHARACTERISTICS (T_J =25°C, unless otherwise specified)

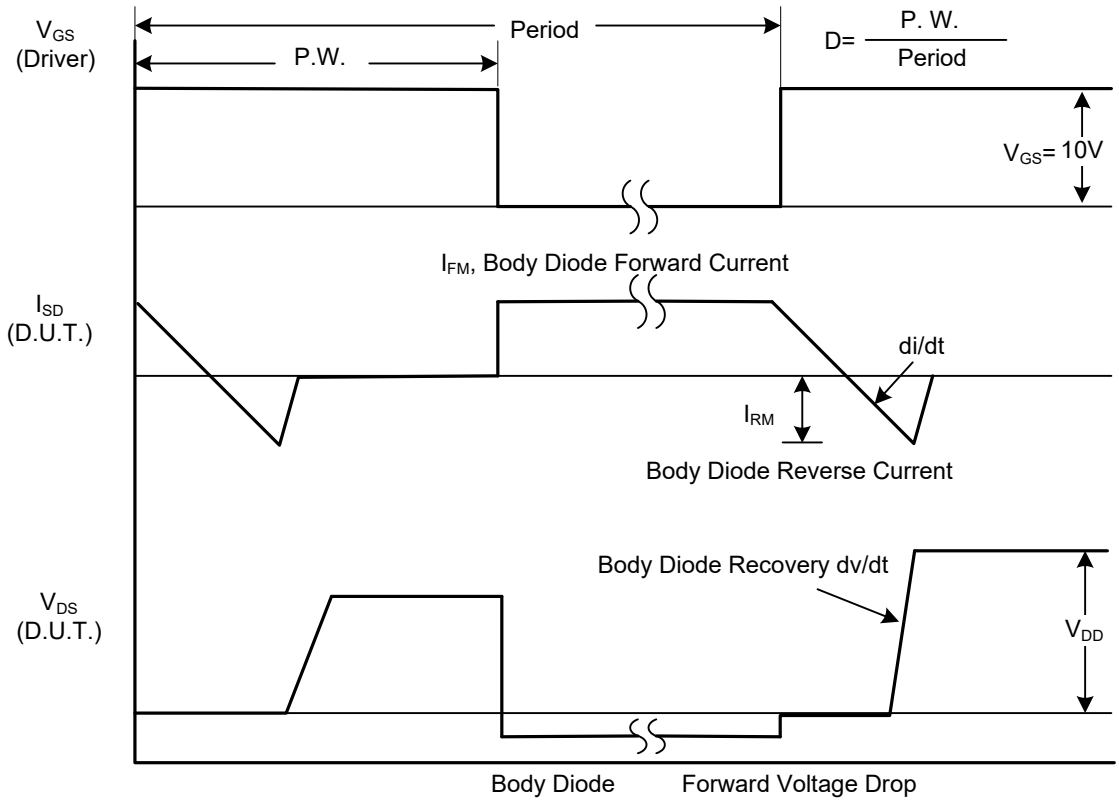
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V, I_D=250μA	30			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=24V, V_{GS}=0V			1	μA
Gate-Source Leakage Current		I_{GSS}	V_{DS}=0V , V_{GS}=±20V			100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}= V_{GS}, I_D=250μA	1.0		3.0	V
Drain-Source On-State Resistance	SOT-23	$R_{DS(ON)}$	V_{GS}=10V, I_D=8.5A			26	mΩ
			V_{GS}=4.5V, I_D=5.0A			40	mΩ
	TO-252 SOP-8 PDFN3×3		V_{GS}=10V, I_D=8.5A			24	mΩ
			V_{GS}=4.5V, I_D=5.0A			35	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{DS}=15V, V_{GS}=0V, f=1MHz		292		pF
Output Capacitance		C_{OSS}			88		pF
Reverse Transfer Capacitance		C_{RSS}			71		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q_G	V_{DS}=24V, V_{GS}=10V, I_D=8.5A		19		nC
Gate-Source Charge		Q_{GS}			3.2		nC
Gate-Drain Charge		Q_{GD}			4.2		nC
Turn-ON Delay Time		$t_{D(ON)}$	V_{DS}=15V, V_{GS}=10V, I_D=8.5A R_G=3Ω		4		ns
Turn-ON Rise Time		t_R			15		ns
Turn-OFF Delay Time		$t_{D(OFF)}$			12		ns
Turn-OFF Fall Time		t_F			24		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				8.5	A
Drain-Source Diode Forward Voltage		V_{SD}	I_S =1.0A, V_{GS}=0V		0.76	1	V
Body Diode Reverse Recovery Time		t_{rr}	I_F=8.5A, dI/dt=100A/μs		244		ns
Body Diode Reverse Recovery Charge		Q_{rr}			495		nC

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

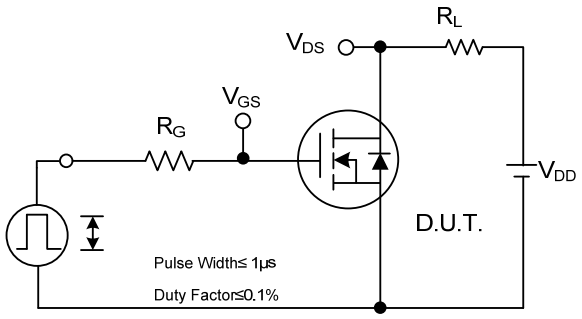


Peak Diode Recovery dv/dt Test Circuit

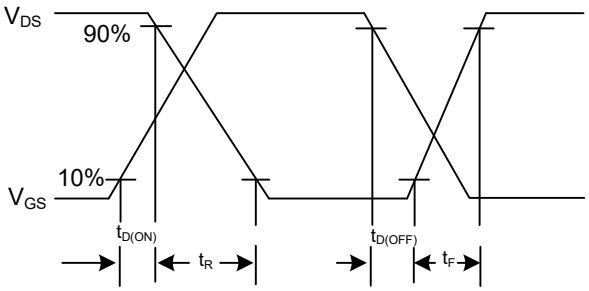


Peak Diode Recovery dv/dt Waveforms

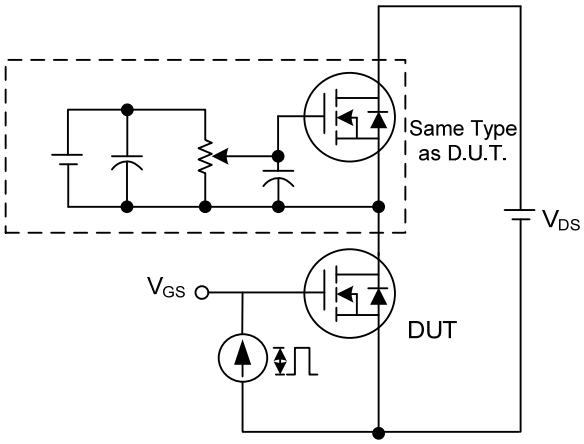
■ TEST CIRCUITS AND WAVEFORMS



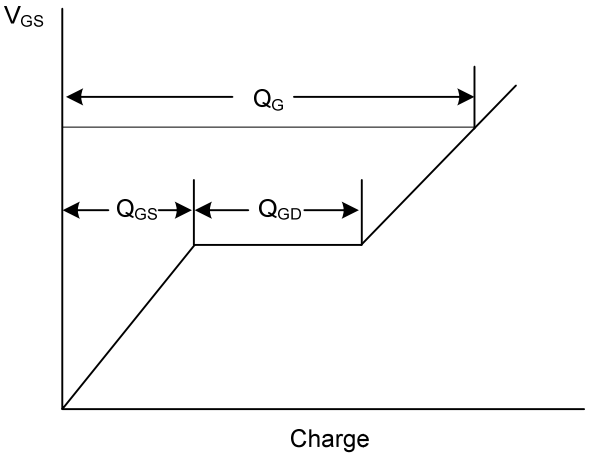
Switching Test Circuit



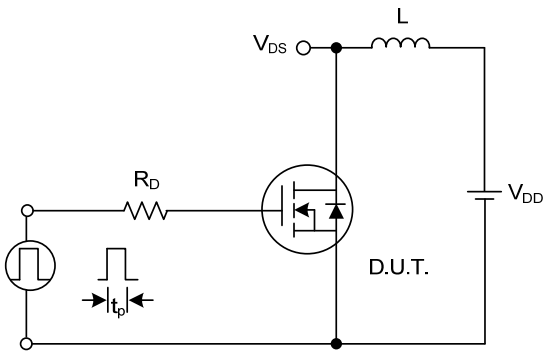
Switching Waveforms



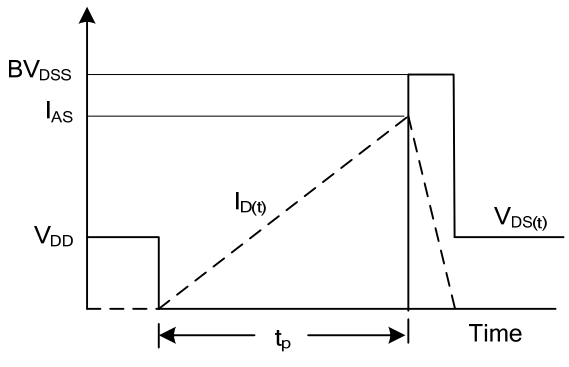
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms