



9N100

Preliminary

Power MOSFET

9A, 1000V N-CHANNEL POWER MOSFET

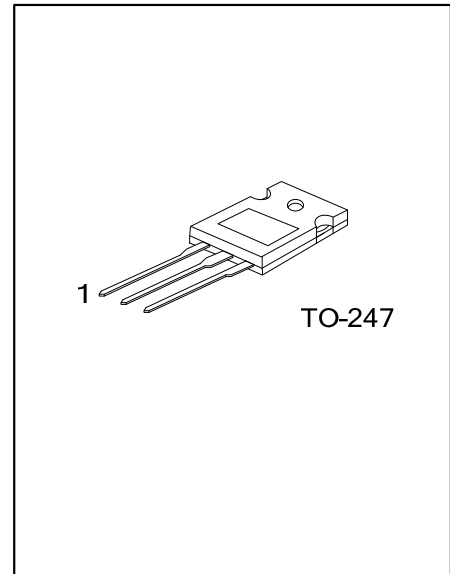
DESCRIPTION

The UTC **9N100** is an N-channel mode power MOSFET using UTC's advanced technology to provide costumers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

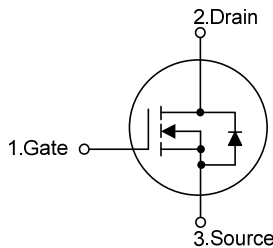
The UTC **9N100** is generally applied in high efficiency switch mode power supplies.

FEATURES

- * $R_{DS(ON)} < 1.7\Omega @ V_{GS}=10V$
- * Fast Switching Speed
- * 100% Avalanche Tested
- * Improved dv/dt Capability



SYMBOL



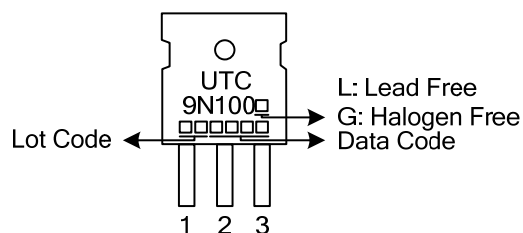
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
9N100L-T47-T	9N100G-T47-T	TO-247	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>9N100L-T47-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Lead Free</p>	<p>(1) T: Tube</p> <p>(2) T47: TO-247</p> <p>(3) L: Lead Free, G: Halogen Free</p>
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MARKING INFORMATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Drain to Source Voltage	V_{DSS}	1000	V
Gate to Source Voltage	V_{GSS}	± 30	V
Continuous Drain Current ($T_C=25^\circ\text{C}$)	I_D	9	A
Pulsed Drain Current (Note 1)	I_{DM}	36	A
Avalanche Current (Note 1)	I_{AR}	9	A
Single Pulsed Avalanche Energy (Note 2)	E_{AS}	600	mJ
Peak Diode Recovery dv/dt (Note 3)	dv/dt	4.0	V/ns
Power Dissipation ($T_C=25^\circ\text{C}$)	P_D	160	W
Linear Derating Factor above $T_C=25^\circ\text{C}$		1.28	W/ $^\circ\text{C}$
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55~+150	$^\circ\text{C}$

- Note: 1. Repetitive Rating : Pulse width limited by maximum junction temperature
 2. $L=14.75\text{mH}$, $I_{AS}=9\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
 3. $I_{SD}\leq 9\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$
 4. Absolute maximum ratings are those values beyond which the device could be permanently damaged.
 Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	50	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	0.78	$^\circ\text{C}/\text{W}$

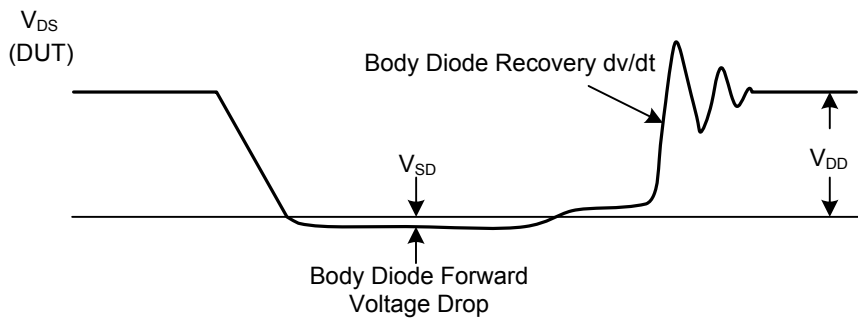
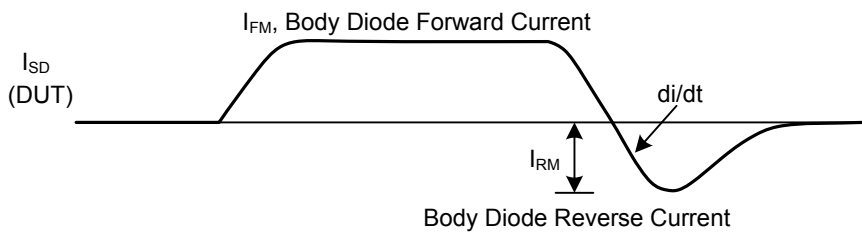
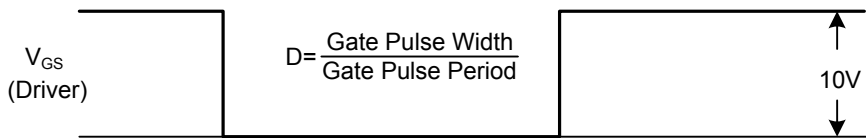
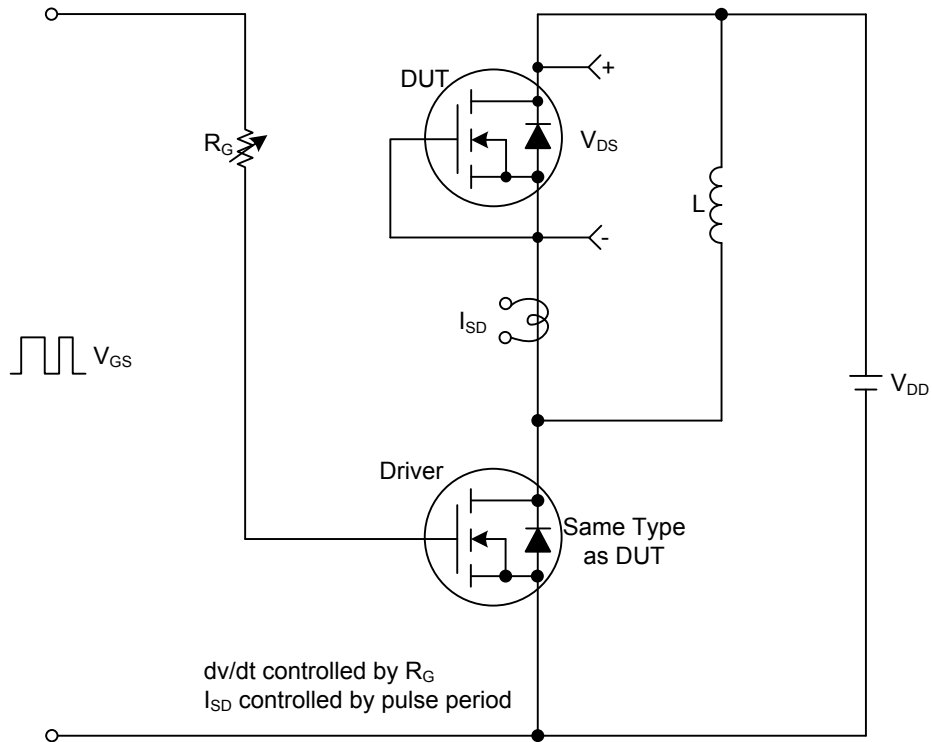
■ ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	1000			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	$I_D=250\mu\text{A}$, Referenced to 25°C		1.4		V/ $^\circ\text{C}$
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=1000\text{V}$, $V_{GS}=0\text{V}$			10	μA
		$V_{DS}=800\text{V}$, $T_C=125^\circ\text{C}$			100	μA
Gate-Source Leakage Current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	3.0		5.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=4.5\text{A}$		1500	1700	m Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$		960	3220	pF
Output Capacitance	C_{OSS}			160	255	pF
Reverse Transfer Capacitance	C_{RSS}			20	24	pF
SWITCHING PARAMETERS (Note 1, Note 2)						
Total Gate Charge	Q_G	$V_{DS}=120\text{V}$, $V_{GS}=10\text{V}$, $I_D=9\text{A}$		225	260	nC
Gate-Source Charge	Q_{GS}			22		nC
Gate-Drain Charge	Q_{GD}			58		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=30\text{V}$, $I_D=1\text{A}$, $R_G=25\Omega$		100	110	ns
Turn-ON Rise Time	t_R			170	200	ns
Turn-OFF Delay Time	$t_{D(OFF)}$			350	400	ns
Turn-OFF Fall Time	t_F			175	190	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				9	A
Maximum Body-Diode Pulsed Current	I_{SM}				36	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_S=9\text{A}$, $V_{GS}=0\text{V}$			1.4	V

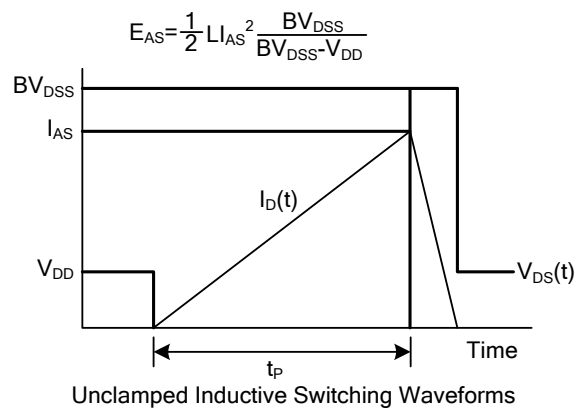
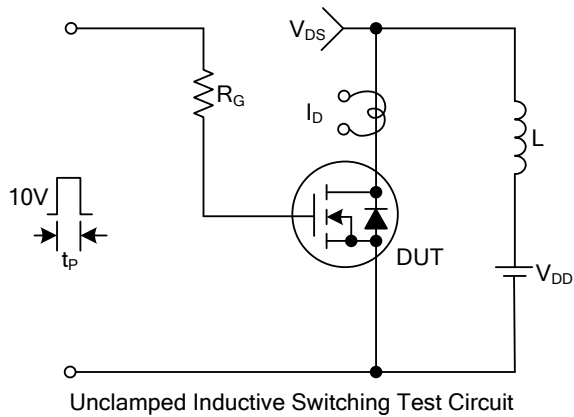
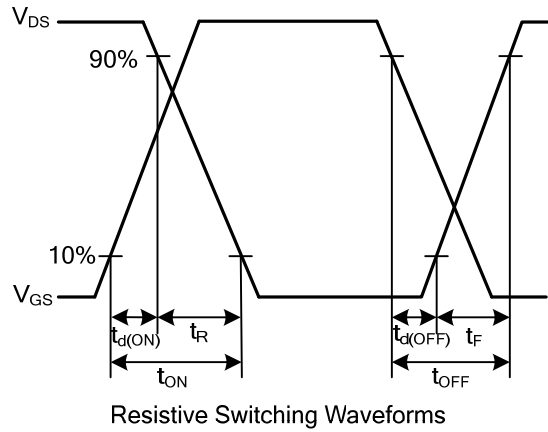
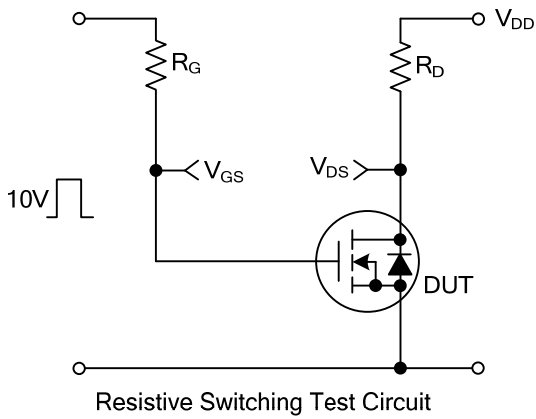
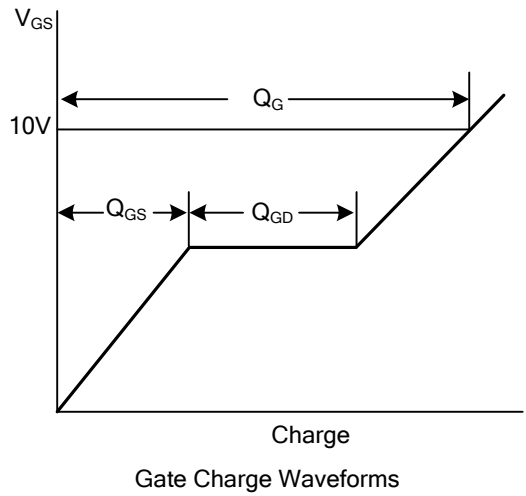
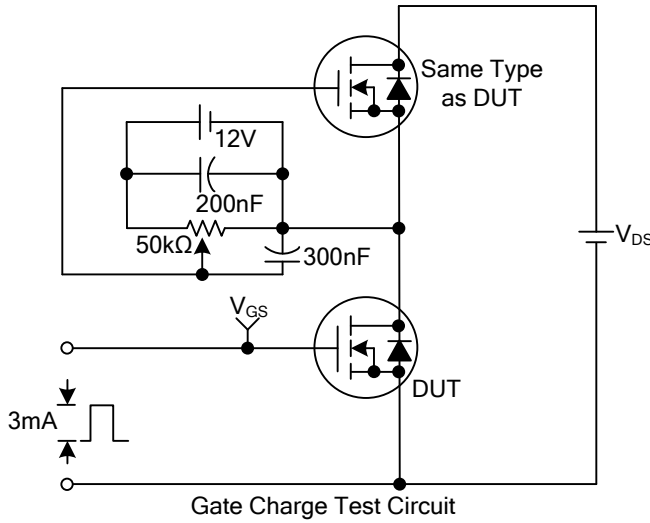
- Note: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
 2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

Peak Diode Recovery dv/dt Test Circuit & Waveforms



■ TEST CIRCUITS AND WAVEFORMS(Cont.)



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