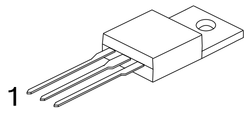
UTC **UNISONIC TECHNOLOGIES CO., LTD**

MJE13007-M

NPN SILICON TRANSISTOR

NPN BIPOLAR POWER TRANSISTOR FOR SWITCHING POWER SUPPLY APPLICATIONS



TO-220

■ DESCRIPTION

The UTC **MJE13007-M** is designed for high-voltage and high-speed power switching inductive circuits where fall time is critical. It is particularly suited for 115 and 220 V switch mode applications.

■ FEATURES

* $V_{CEO(SUS)}$ 400V
* 700V Blocking Capability

■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
MJE13007L-M-TA3-T	MJE13007G-M-TA3-T	TO-220	B	C	E	Tube

MJE13007L-M-TA3-T	
(1)Packing Type	(1)T: Tube
(2)Package Type	(2) TA3: TO-220
(3)Lead Free	(3) G: Halogen Free, L: Lead Free

■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
Collector-Emitter Sustaining Voltage		V_{CEO}	400	V
Collector-Emitter Breakdown Voltage		V_{CBO}	700	V
Emitter-Base Voltage		V_{EBO}	9.0	V
Collector Current	Continuous	I_C	8.0	A
	Peak (1)	I_{CM}	16	A
Base Current	Continuous	I_B	4.0	A
	Peak (1)	I_{BM}	8.0	A
Emitter Current	Continuous	I_E	12	A
	Peak (1)	I_{EM}	24	A
Power Dissipation	T_C = 25°C	P_D	80	W
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55~+150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	°C/W
Junction to Case	θ_{JC}	1.56	°C/W

Note 1: Pulse Test: Pulse Width = 5.0 ms, Duty Cycle≤10%.
Measurement made with thermocouple contacting the bottom insulated mounting surface of the package (in a location beneath the die), the device mounted on a heatsink with thermal grease applied at a mounting torque of 6 to 8•lbs.

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Collector-Emitter Sustaining Voltage	$V_{CEO(SUS)}$	I_C=10mA, I_B=0	400			V
Collector Cutoff Current	I_{CBO}	V_{CES}=700V			0.1	mA
		V_{CES}=700V, T_C=125°C			1.0	mA
Emitter Cutoff Current	I_{EBO}	V_{EB}=9.0V, I_C=0			100	μA
DC Current Gain	h_{FE1}	I_C=2.0A, V_{CE}=5.0V	8.0		40	
	h_{FE2}	I_C=5.0A, V_{CE}=5.0V	5.0		30	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C=2.0A, I_B=0.4A			1.0	V
		I_C=5.0A, I_B=1.0A			2.0	
		I_C=5.0A, I_B=1.0A, T_C=100°C			3.0	
		I_C=5.0A, I_B=2.5A			0.6	
		I_C=8.0A, I_B=2.0A			3.0	
Base-Emitter Saturation Voltage	$V_{BE(SAT)}$	I_C=2.0A, I_B=0.4A			1.2	V
		I_C=5.0A, I_B=1.0A			1.6	
		I_C=5.0A, I_B=1.0A, T_C=100°C			1.5	
		I_C=5.0A, I_B=2.5A		1.2	1.5	
Current-Gain-Bandwidth Product	f_T	I_C=500mA, V_{CE}=10V, f=1.0 MHz	4.0	14		MHz
Output Capacitance	C_{OB}	V_{CB}=10V, I_E=0, f=0.1MHz		80		pF
RESISTIVE LOAD (TABLE 1)						
Delay Time	t_D	V_{CC}=125V, I_C=5.0A, I_{B1}=I_{B2}=1.0A, t_P=25μs, Duty Cycle≤1.0%		0.025	0.1	μs
Rise Time	t_R			0.5	1.5	μs
Storage Time	t_S			1.8	3.0	μs
Fall Time	t_F			0.23	0.7	μs

Note: Pulse Test: Pulse Width≤300μs, Duty Cycle≤2.0%

■ TYPICAL THERMAL RESPONSE

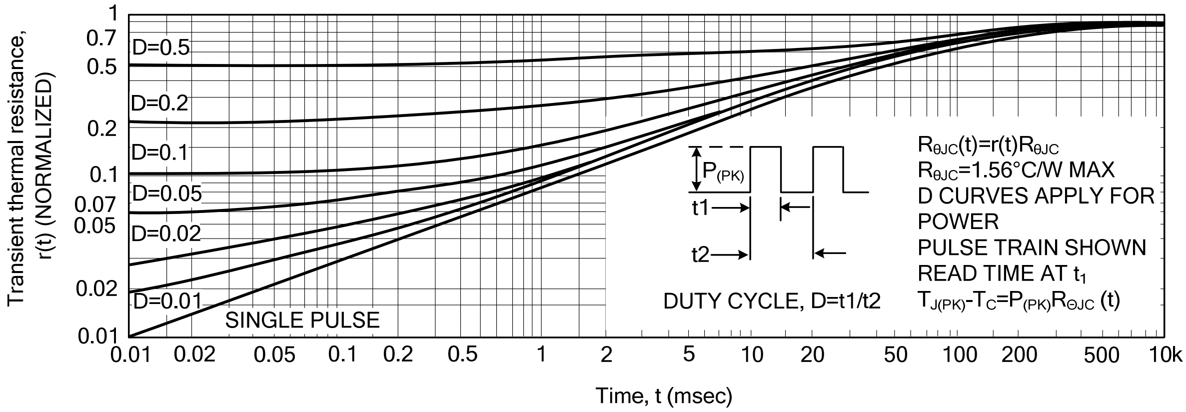


Fig. 1 Typical Thermal Response

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Fig. 7 is based on T_C = 25°C; $T_{J(PK)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be debated when $T_C \geq 25$°C. Second breakdown limitations do not debate the same as thermal limitations. Allowable current at the voltages shown on Fig. 7 may be found at any case temperature by using the appropriate curve on Fig. 9.

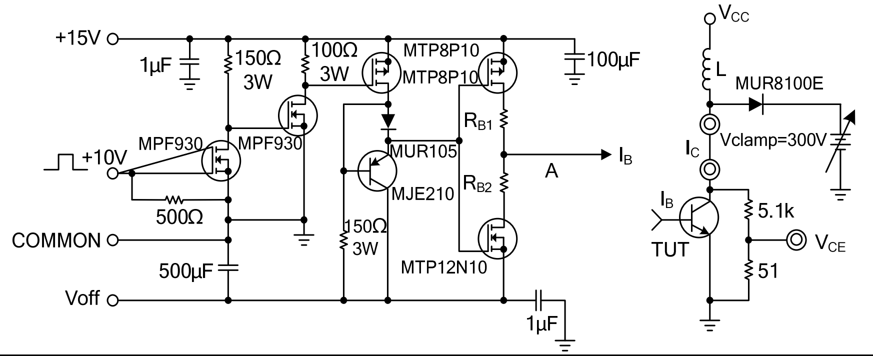
At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Fig. 8) is discussed in the applications information section.

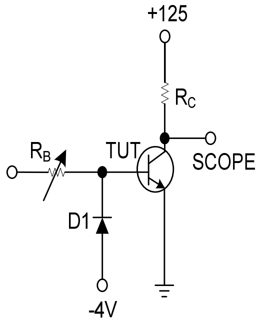
Table 1. Test Conditions for Dynamic Performance

TEST CIRCUITS

REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING



RESISTIVE SWITCHING

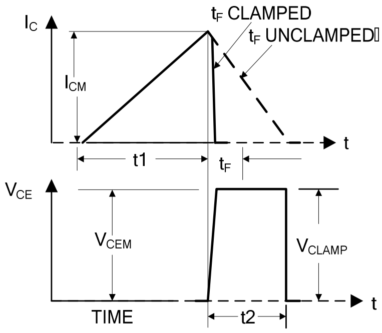


CIRCUIT VALUES

$BV_{CEO(SUS)}$	Inductive Switching	RBSOA
L=10mH R_{B2}=8 V_{CC}=20V $I_{C(PK)}$=100mA	L=20mH R_{B2}=0 V_{CC}=15V R_{B1} selected for desired I_{B1}	L=500mH R_{B2}=0 V_{CC}=15Volts R_{B1} selected for desired I_{B1}

Resistive switching:

V_{CC}=125V
R_C=25Ω
D1=1N5820 OR EQUIV



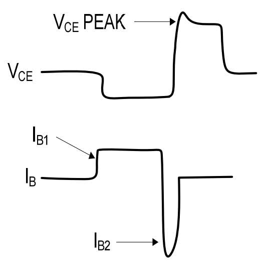
t1 ADJUSTED TO OBTAIN I_C

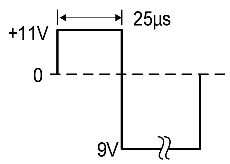
$t1 \le \frac{Lcoil(I_{CM})}{V_{CC}}$

$t2 \le \frac{Lcoil(I_{CM})}{V_{CLAMP}}$

Test Equipment
Scope-Tektronix
475 or Equivalent

TYPICAL WAVEFORMS





t_r, t_f<10ns
DUTY CYCLE=1.0%
RB AND RC ADJUSTED
FOR DESIRED IB AND I_C

■ TYPICAL CHARACTERISTICS

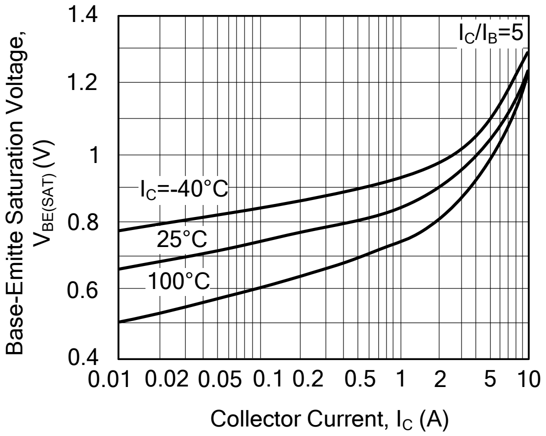


Fig. 2 Base-Emitter Saturation Voltage

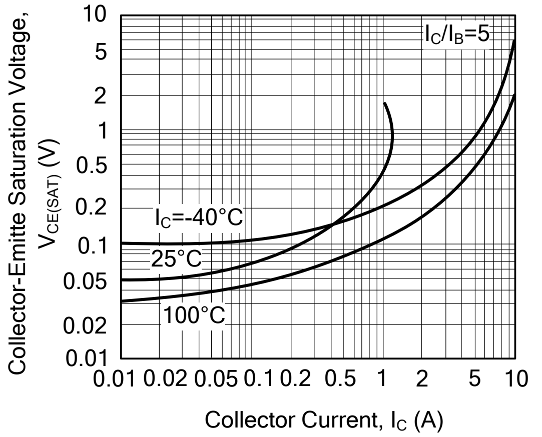


Fig. 3 Collector-Emitter Saturation Voltage

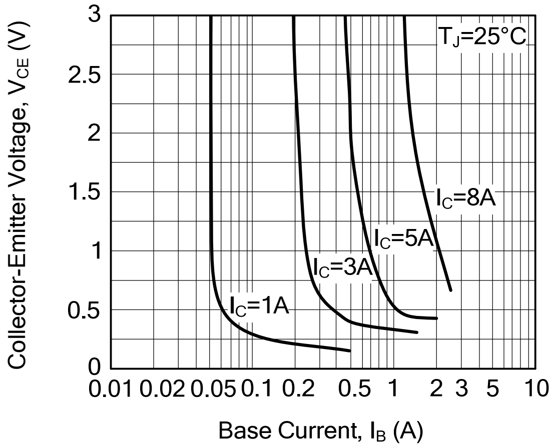


Fig. 4 Collector Saturation Region

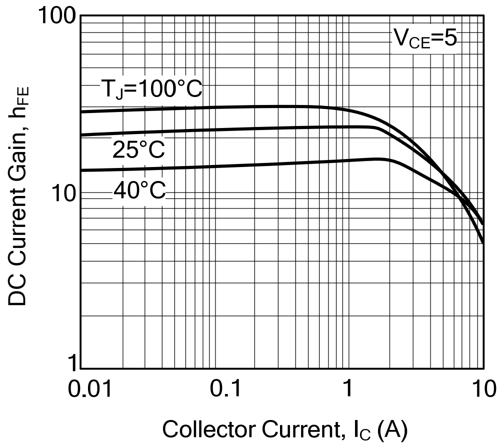


Fig. 5 DC Current Gain

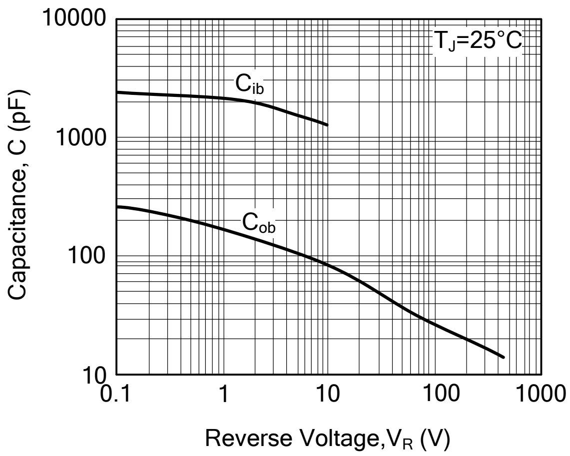


Fig. 6 Capacitance

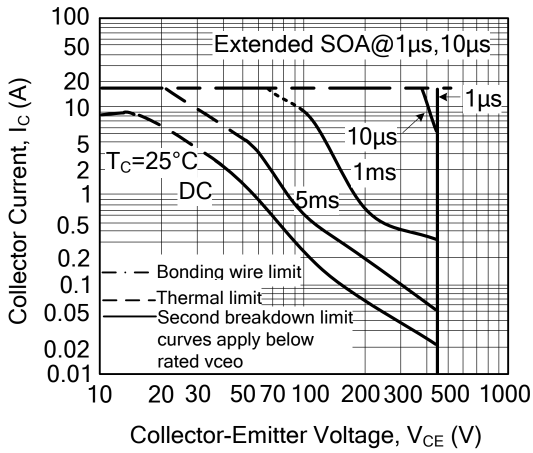


Fig. 7 Maximum Forward Bias Safe Operating Area

■ TYPICAL CHARACTERISTICS

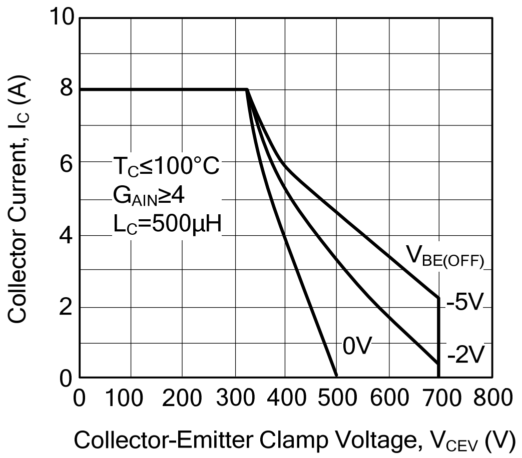


Fig. 8 Maximum Reverse Bias Switching Safe Operating Area

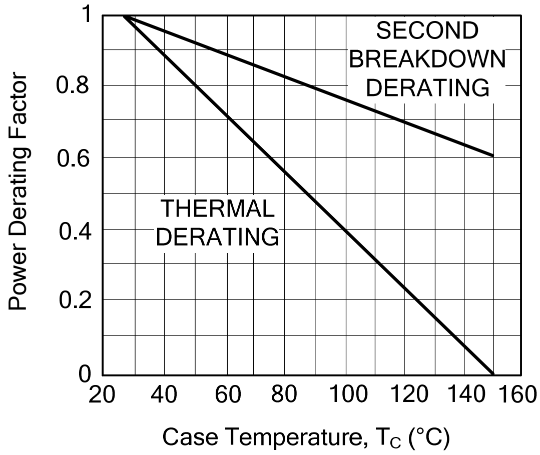


Fig. 9 Forward Bias Power Derating

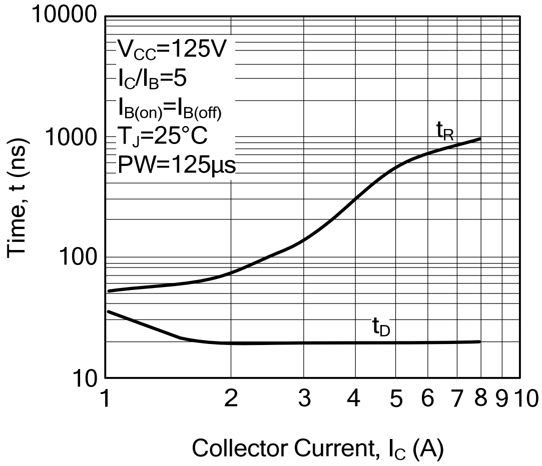


Fig. 10 Turn-On Time(Resistive Load)

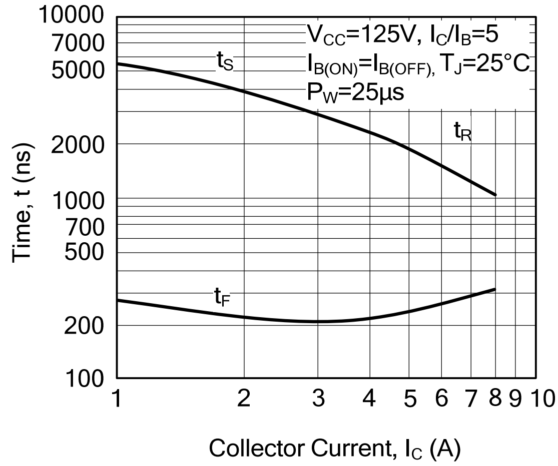


Fig. 11 Turn-Off Time(Resistive Load)