

**U74HC74****CMOS IC****DUAL D FLIP-FLOP WITH SET
AND RESET, POSITIVE-EDGE
TRIGGER****DESCRIPTION**

The **U74HC74** contains dual D flip-flops and each flip-flop has independent DATA, $\overline{\text{SET}}$, $\overline{\text{RESET}}$ and clock inputs and complementary outputs Q and $\overline{\text{Q}}$. A low level at appropriate input helps $\overline{\text{SET}}$ and $\overline{\text{RESET}}$ adjust the output. Data will be transferred to the output during the low-to-high transition of the CLK while $\overline{\text{SET}}$ and $\overline{\text{RESET}}$ are high.

FEATURES

- * Operation Voltage Range: 2 ~ 6V
- * Buffered Inputs
- * Asynchronous Set and Reset
- * Complementary Outputs
- * High Noise Immunity

ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC74L-D14-T	U74HC74G-D14-T	DIP-14	Tube
U74HC74L-UEA-R	U74HC74G-UEA-R	SOP-14U	Tape Reel
U74HC74L-UEB-R	U74HC74G-UEB-R	TSSOP-14U	Tape Reel

U74HC74G-D14-T

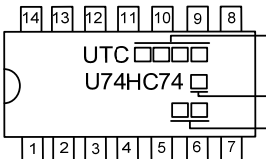
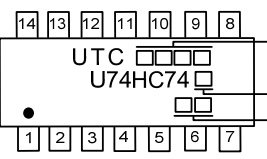
- (1) Packing Type
- (2) Package Type
- (3) Green Package

(1) T: Tube, R: Tape Reel

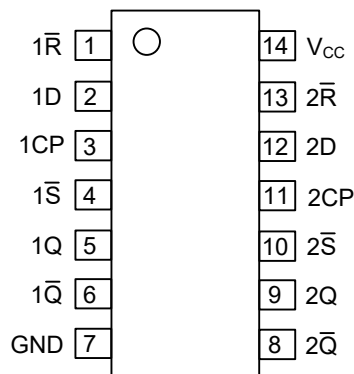
(2) D14: DIP-14, UEA: SOP-14U, UEB: TSSOP-14U

(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING

DIP-14	SOP-14U / TSSOP-14U
 14 13 12 11 10 9 8 UTC □□□□ U74HC74 □ □ 1 2 3 4 5 6 7 → Date Code L: Lead Free → G: Halogen Free → Lot Code	 14 13 12 11 10 9 8 UTC □□□□ U74HC74 □ □ 1 2 3 4 5 6 7 → Date Code L: Lead Free → G: Halogen Free → Lot Code

PIN CONFIGURATION



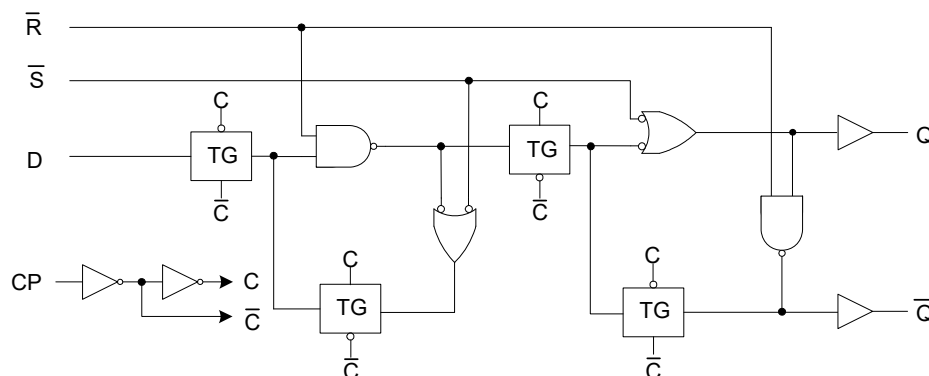
FUNCTION TABLE (each gate)

INPUT			OUTPUT		
SET	RESET	CP	D	Q	$\bar{Q}$
L	H	x	x	H	L
H	L	x	x	L	H
H	H	$\uparrow$	H	H	L
H	H	$\uparrow$	L	L	H
H	H	L	x	Q0	$\bar{Q}0$
L	L	x	x	H (note)	H (note)

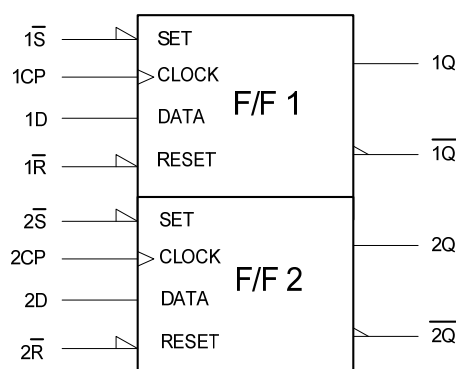
Note: Unstable state, it will not persist when set and reset inputs return to their inactive level.

FUNCTIONAL DIAGRAM

Logic Diagram



IEC logic symbol



■ **ABSOLUTE MAXIMUM RATING** (Unless otherwise specified)(Note)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ +7	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Input Clamp Current	I_{IK}	±20	mA
Output Clamp Current	I_{OK}	±20	mA
Output Current	I_{OUT}	±25	mA
V_{CC} or GND Current	I_{CC}	±50	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	2		6	V
Input Voltage	V_{IN}	0		V_{CC}	V
Output Voltage	V_{OUT}	0		V_{CC}	V
Input Transition Rise or Fall Rate	$V_{CC}=2V$	t_r, t_f		1000	ns
	$V_{CC}=4.5V$			500	ns
	$V_{CC}=6V$			400	ns
Operating Temperature	T_A	-40		+125	°C

■ **STATIC CHARACTERISTICS** (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A=25^{\circ}C$			$T_A=-40\sim+125^{\circ}C$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-Level Input Voltage	V_{IH}	$V_{CC}=2.0V$	1.5			1.5			V
		$V_{CC}=4.5V$	3.15			3.15			V
		$V_{CC}=6.0V$	4.2			4.2			V
Low-Level Input Voltage	V_{IL}	$V_{CC}=2.0V$			0.5			0.5	V
		$V_{CC}=4.5V$			1.35			1.35	V
		$V_{CC}=6.0V$			1.8			1.8	V
High-Level Output Voltage	V_{OH}	$V_{CC}=2.0V, I_{OH}=-20\mu A$	1.9			1.62			V
		$V_{CC}=4.5V, I_{OH}=-20\mu A$	4.4			4.12			V
		$V_{CC}=6.0V, I_{OH}=-20\mu A$	5.9			5.72			V
		$V_{CC}=4.5V, I_{OH}=-4mA$	3.98			3.7			V
		$V_{CC}=6V, I_{OH}=-5.2mA$	5.48			5.2			V
Low-Level Output Voltage	V_{OL}	$V_{CC}=2.0V, I_{OL}=20\mu A$			0.1			0.14	V
		$V_{CC}=4.5V, I_{OL}=20\mu A$			0.1			0.14	V
		$V_{CC}=6.0V, I_{OL}=20\mu A$			0.1			0.14	V
		$V_{CC}=4.5, I_{OL}=4mA$			0.26			0.33	V
		$V_{CC}=6, I_{OL}=5.2mA$			0.26			0.33	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=6.0V, V_{IN}=V_{CC}$ or GND			±0.1			±0.1	μA
Quiescent Supply Current	I_Q	$V_{CC}=6.0V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$			4			40	μA

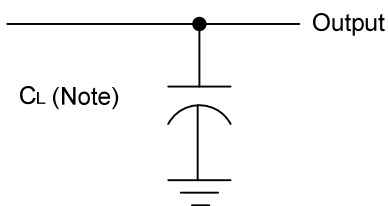
■ DYNAMIC CHARACTERISTICS (Input: $t_R, t_F=6\text{ns}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A=25^\circ\text{C}$			$T_A=-40\sim+125^\circ\text{C}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation delay from input (CP) to output(Q, $\bar{Q}$)	t_{PLH}/t_{PHL}	$V_{CC}=2.0\text{V}, C_L=50\text{pF}$			175			265	ns
		$V_{CC}=4.5\text{V}, C_L=50\text{pF}$			35			53	ns
		$V_{CC}=6.0\text{V}, C_L=50\text{pF}$			30			45	ns
Propagation delay from input ($\bar{R}, \bar{S}$) to output (Q, $\bar{Q}$)	t_{PLH}/t_{PHL}	$V_{CC}=2.0\text{V}, C_L=50\text{pF}$			200			300	ns
		$V_{CC}=4.5\text{V}, C_L=50\text{pF}$			40			60	ns
		$V_{CC}=6.0\text{V}, C_L=50\text{pF}$			34			51	ns
Output Transition Time	t_{TLH}/t_{THL}	$V_{CC}=2.0\text{V}, C_L=50\text{pF}$			75			110	ns
		$V_{CC}=4.5\text{V}, C_L=50\text{pF}$			15			22	ns
		$V_{CC}=6.0\text{V}, C_L=50\text{pF}$			13			19	ns
CP frequency	f_{MAX}	$V_{CC}=5\text{V}, C_L=15\text{pF}$		50			50		MHZ

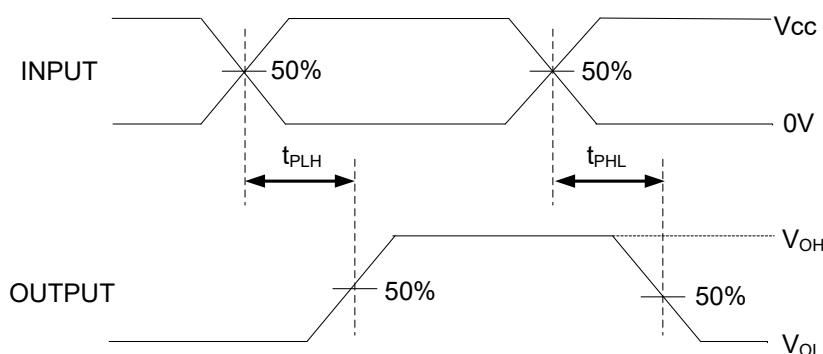
■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_{IN}	$V_{CC}=6.0\text{V}, V_{IN}=V_{CC}$ or GND			10	pF
Power Dissipation Capacitance	C_{PD}	No Load		25		pF

■ TEST CIRCUIT AND WAVEFORMS



Note: C_L includes probe and jig capacitance.



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