



8N50H

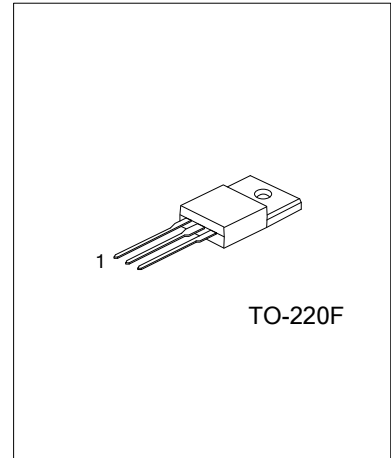
Power MOSFET

8A, 500V N-CHANNEL POWER MOSFET

DESCRIPTION

The UTC **8N50H** is an N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

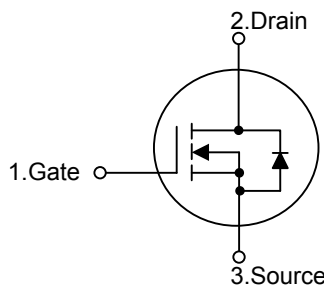
The UTC **8N50H** is generally applied in high efficiency switch mode power supplies, active power factor correction and electronic lamp ballasts based on half bridge topology.



FEATURES

- * $R_{DS(ON)}=0.8\Omega @ V_{GS}=10V$
- * High Switching Speed
- * 100% Avalanche Tested

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
8N50HL-TF3-T	8N50HG-TF3-T	TO-220F	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>8N50HL-TA3-T</p> <ul style="list-style-type: none"> (1)Packing Type (2)Package Type (3)Lead Free 	<ul style="list-style-type: none"> (1) T: Tube (2) TF3: TO-220F (3) G: Halogen Free, L: Lead Free
--	--

■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	500	V
Gate-Source Voltage	V_{GSS}	± 30	V
Drain Current	I_D	7 (Note 2)	A
Continuous ($T_C=25^\circ\text{C}$)			
Avalanche Current (Note 3)	I_{AR}	7	A
Single Pulsed Avalanche Energy (Note 4)	E_{AS}	270	mJ
Power Dissipation	P_D		W
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55~+150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Drain current limited by maximum junction temperature

3. Repetitive Rating: Pulse width limited by maximum junction temperature

4. $L = 10\text{mH}$, $I_{AS} = 8\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}		$^\circ\text{C/W}$
Junction to Case	θ_{JC}		$^\circ\text{C/W}$

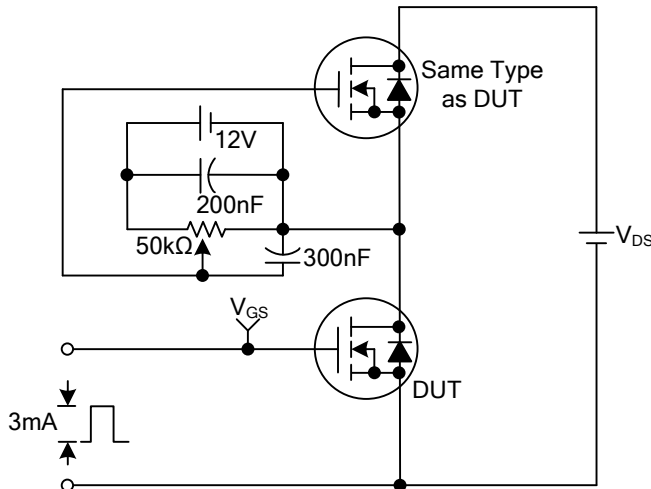
■ ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	500			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate- Source Leakage Current	I_{GSS}	Forward			+100	nA
		Reverse			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=3.5\text{A}$		0.8	1	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$				pF
Output Capacitance	C_{OSS}					pF
Reverse Transfer Capacitance	C_{RSS}					pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{DD}=50\text{V}$, $I_D=1.3\text{A}$, $I_G=100\mu\text{A}$, $V_{GS}=10\text{V}$ (Note 1, 2)		12.8	16.6	nC
Gate to Source Charge	Q_{GS}			3.7		nC
Gate to Drain Charge	Q_{GD}			5.8		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=30\text{V}$, $I_D=0.5\text{A}$, $R_G=25\Omega$, $V_{GS}=0\sim 10\text{V}$ (Note 1, 2)		6	20	ns
Rise Time	t_R			55	120	ns
Turn-OFF Delay Time	$t_{D(OFF)}$			25	60	ns
Fall-Time	t_F			35	80	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				7	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_S=7\text{A}$, $V_{GS}=0\text{V}$			1.4	V

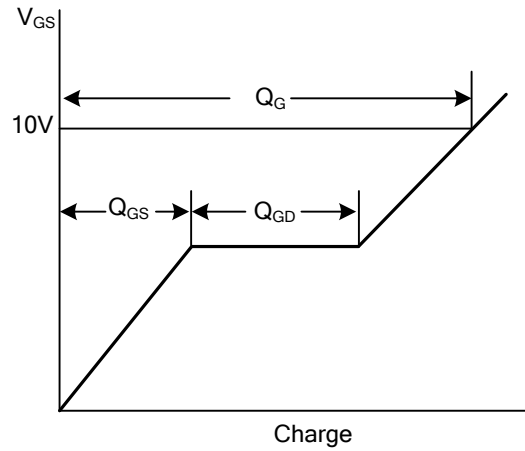
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

2. Essentially independent of operating temperature

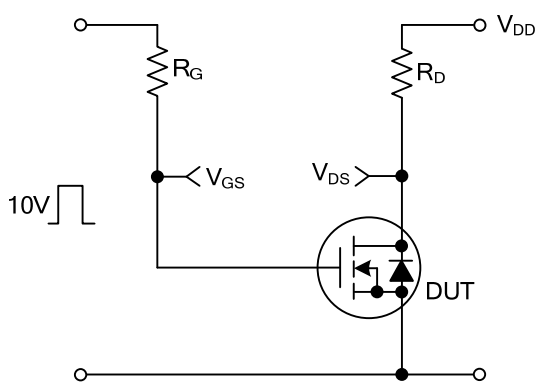
TEST CIRCUITS AND WAVEFORMS



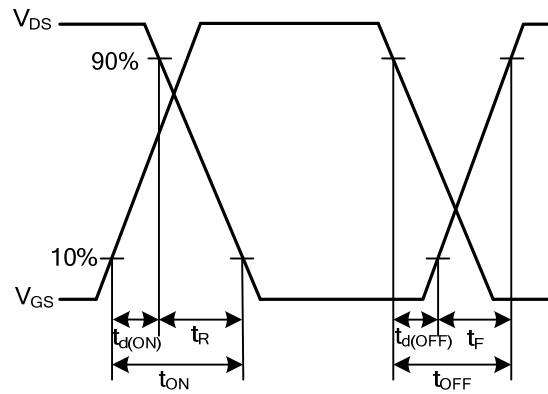
Gate Charge Test Circuit



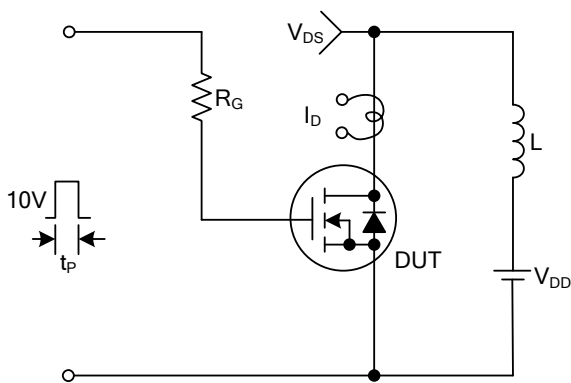
Gate Charge Waveforms



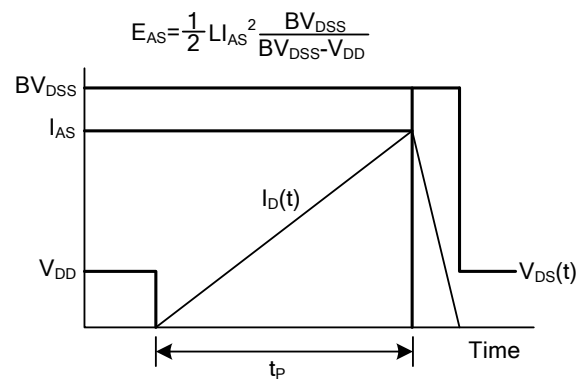
Resistive Switching Test Circuit



Resistive Switching Waveforms

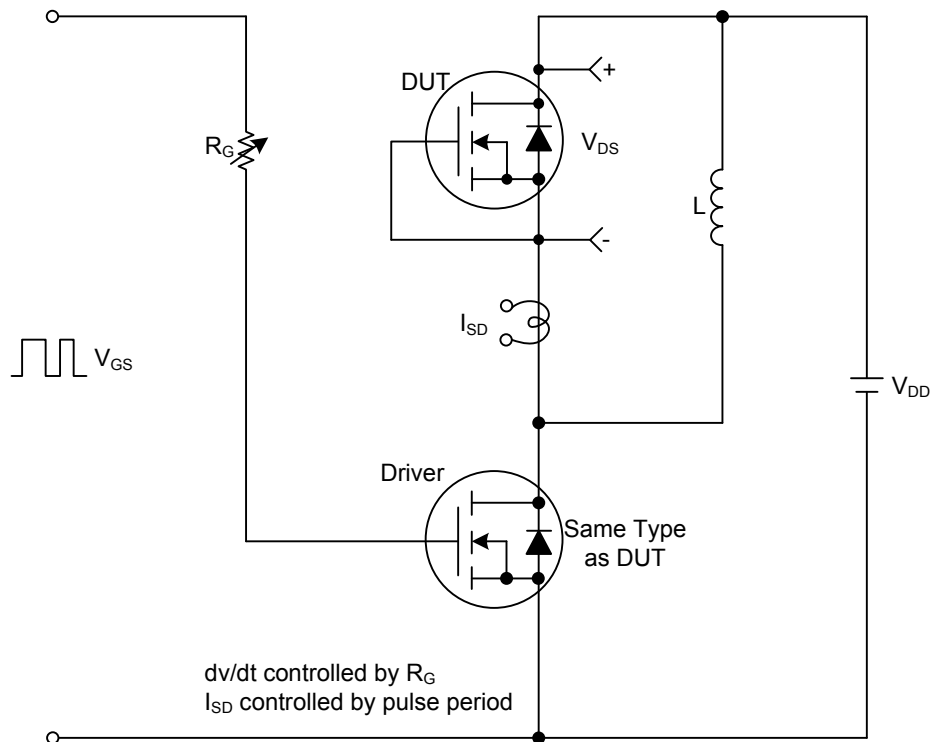


Unclamped Inductive Switching Test Circuit

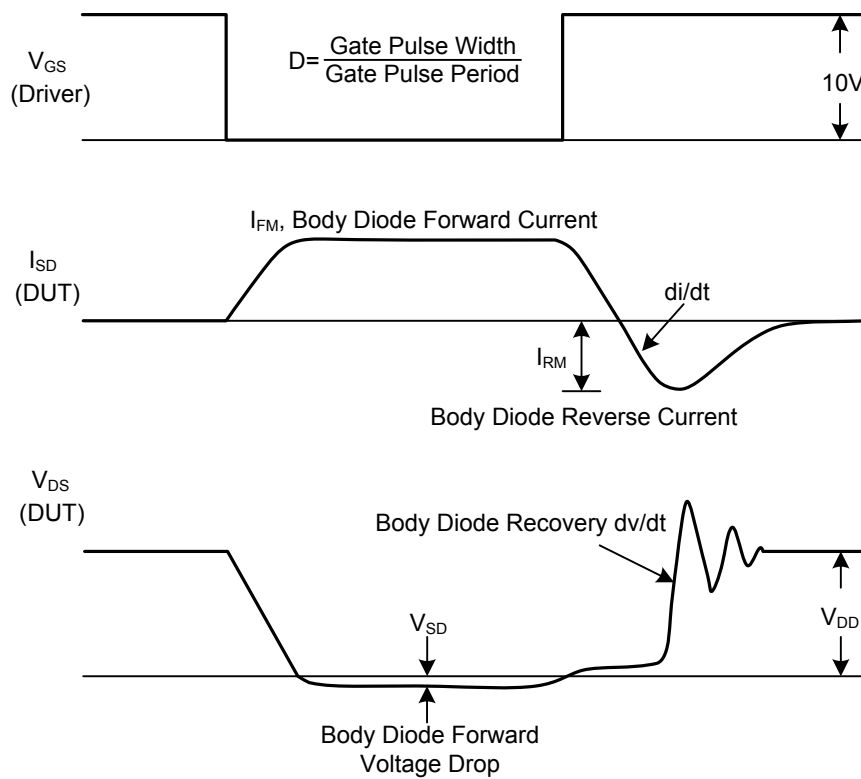


Unclamped Inductive Switching Waveforms

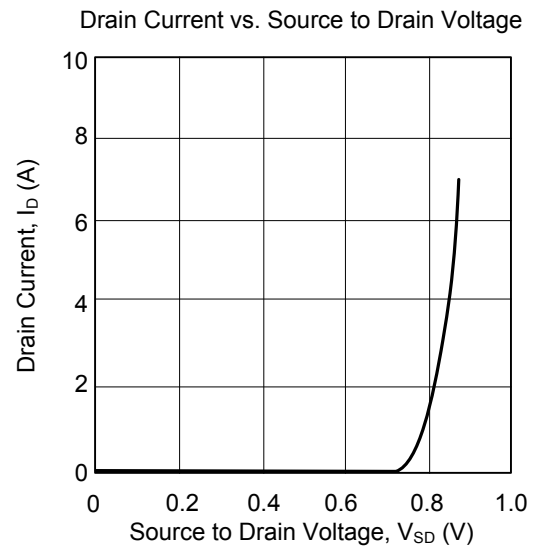
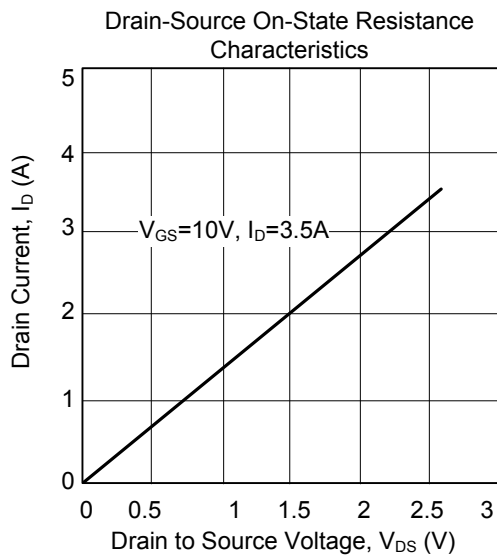
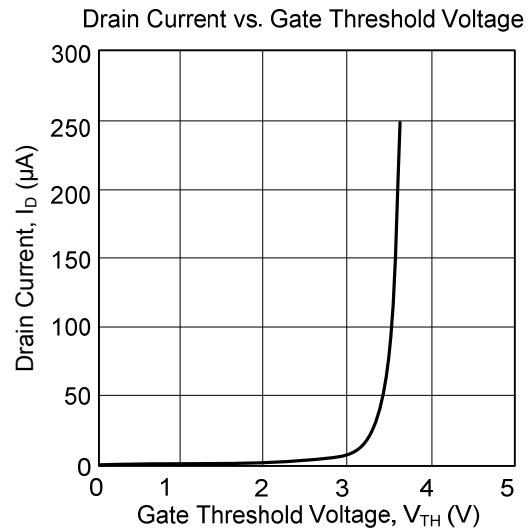
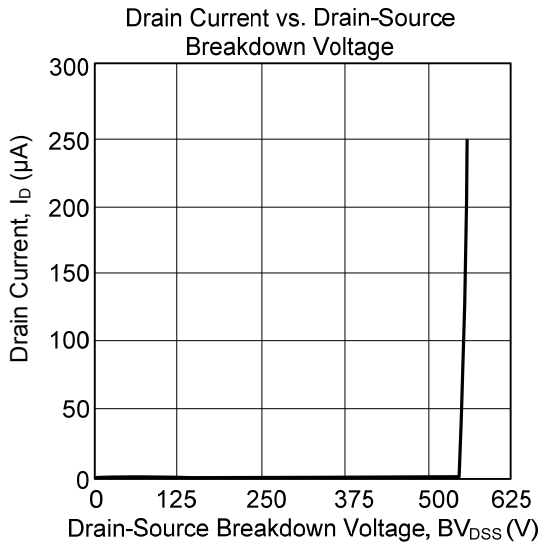
■ TEST CIRCUITS AND WAVEFORMS(Cont.)



Peak Diode Recovery dv/dt Test Circuit & Waveforms



■ TYPICAL CHARACTERISTICS



UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.