



U74LVC2G132

CMOS IC

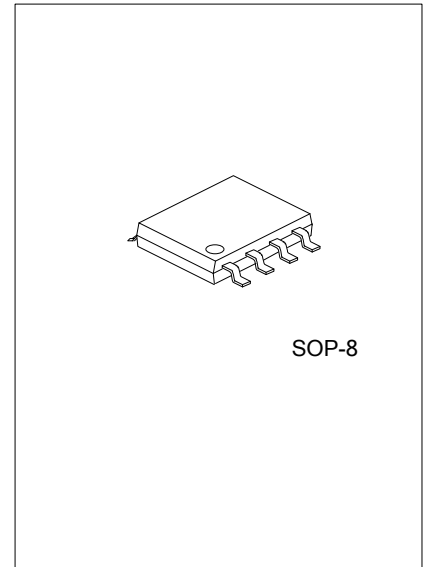
DUAL 2-INPUT NAND GATE WITH SCHMITT-TRIGGER INPUTS

DESCRIPTION

The **U74LVC2G132** is a dual 2-input NAND gate with Schmitt-trigger inputs circuit and it contains two inverters that perform the function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$

The device have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals because of the Schmitt-trigger action in the input.

This device has power-down protective circuit, preventing device destruction when it is powered down.



SOP-8

FEATURES

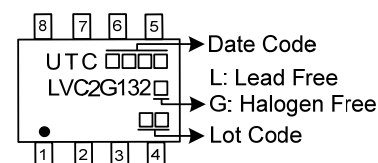
- * Operate from 1.65V to 5.5V
- * Inputs accept voltages to 5.5V
- * I_{off} supports partial-power-down mode
- * Low power dissipation: $I_{CC} = 10\mu A$ (Max)
- * Max t_{PD} of 5.3 ns at 3.3V
- * $\pm 24mA$ output drive ($V_{CC} = 3.3V$)

ORDERING INFORMATION

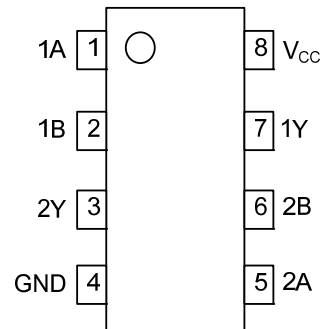
Ordering Number		Package	Packing
Free Plating	Halogen Free		
U74LVC2G132L-S08-R	U74LVC2G132G-S08-R	SOP-8	Tape Reel

U74LVC2G132G-S08-R (1) Packing Type (2) Package Type (3) Green Package	(1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING



PIN CONFIGURATION

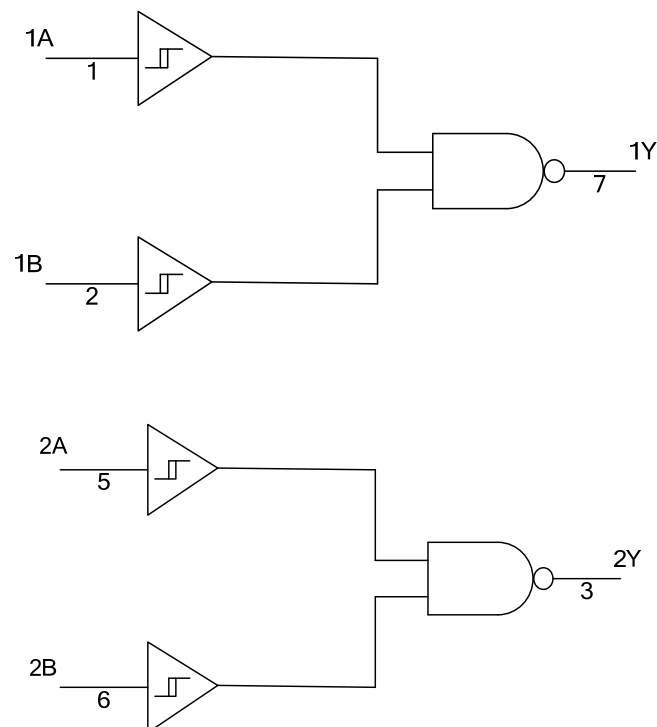


FUNCTION TABLE (EACH GATE)

INPUT		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

Note: H: HIGH voltage level; L: LOW voltage level

LOGIC DIAGRAM (positive logic)



IEC logic symbol

■ ABSOLUTE MAXIMUM RATING ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{CC}	-0.5 ~ +6.5	V
Input Voltage		V_{IN}	-0.5 ~ +6.5	V
Output Voltage	Output in the high or low state	V_{OUT}	-0.5 ~ $V_{CC}+0.5$	V
	Output in the high-impedance or power-off state		-0.5 ~ +6.5	V
V_{CC} or GND Current		I_{CC}	± 100	mA
Continuous Output Current ($V_{OUT}=0$ to V_{CC})		I_{OUT}	± 50	mA
Input Clamp Current ($V_{IN}<0$)		I_{IK}	-50	mA
Output Clamp Current ($V_{OUT}<0$)		I_{OK}	-50	mA
Storage Temperature Range		T_{STG}	-65 ~ +150	$^{\circ}\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}	High or low state	0		V_{CC}	V
High-level Output Current	I_{OH}	$V_{CC}=1.65\text{V}$			-4	mA
		$V_{CC}=2.3\text{V}$			-8	mA
		$V_{CC}=3\text{V}$			-16	mA
		$V_{CC}=3\text{V}$			-24	mA
		$V_{CC}=4.5\text{V}$			-32	mA
Low-level Output Current	I_{OL}	$V_{CC}=1.65\text{V}$			4	mA
		$V_{CC}=2.3\text{V}$			8	mA
		$V_{CC}=3\text{V}$			16	mA
		$V_{CC}=3\text{V}$			24	mA
		$V_{CC}=4.5\text{V}$			32	mA
Operating Temperature	T_A		-40		+125	$^{\circ}\text{C}$

■ ELECTRICAL CHARACTERISTICS ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive-Going Input Threshold Voltage	V_{T+}	$V_{CC}=1.65\text{V}$	0.79		1.16	V
		$V_{CC}=2.3\text{V}$	1.11		1.56	
		$V_{CC}=3.0\text{V}$	1.5		1.87	
		$V_{CC}=4.5\text{V}$	2.16		2.74	
		$V_{CC}=5.5\text{V}$	2.61		3.33	
Negative-Going Input Threshold Voltage	V_{T-}	$V_{CC}=1.65\text{V}$	0.39		0.62	V
		$V_{CC}=2.3\text{V}$	0.58		0.87	
		$V_{CC}=3.0\text{V}$	0.84		1.14	
		$V_{CC}=4.5\text{V}$	1.41		1.79	
		$V_{CC}=5.5\text{V}$	1.87		2.29	
Hysteresis Voltage ($V_{T+}-V_{T-}$)	ΔV_T	$V_{CC}=1.65\text{V}$	0.37		0.62	V
		$V_{CC}=2.3\text{V}$	0.48		0.77	
		$V_{CC}=3.0\text{V}$	0.56		0.87	
		$V_{CC}=4.5\text{V}$	0.71		1.04	
		$V_{CC}=5.5\text{V}$	0.71		1.11	

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	V_{OH}	$V_{CC}=1.65V \sim 5.5V, I_{OH}=-100\mu A$	$V_{CC}-0.1$			V
		$V_{CC}=1.65V, I_{OH}=-4mA$	1.2			
		$V_{CC}=2.3V, I_{OH}=-8mA$	1.9			
		$V_{CC}=3.0V, I_{OH}=-16mA$	2.4			
		$V_{CC}=3.0V, I_{OH}=-24mA$	2.3			
		$V_{CC}=4.5V, I_{OH}=-32mA$	3.8			
Low-Level Output Voltage	V_{OL}	$V_{CC}=1.65V \sim 5.5V, I_{OL}=100\mu A$			0.1	V
		$V_{CC}=1.65V, I_{OL}=4mA$			0.45	
		$V_{CC}=2.3V, I_{OL}=8mA$			0.3	
		$V_{CC}=3.0V, I_{OL}=16mA$			0.4	
		$V_{CC}=3.0V, I_{OL}=24mA$			0.55	
		$V_{CC}=4.5V, I_{OL}=32mA$			0.55	
Input Leakage Current (A or B port)	$I_{I(LEAK)}$	$V_{CC}=1.65V \sim 5.5V, V_{IN}=V_{CC}$ or GND			± 1	μA
Power OFF Leakage Current	I_{OFF}	$V_{CC}=0V, V_{IN}$ or $V_{OUT}=5.5V$			± 10	μA
Quiescent Supply Current	I_Q	$V_{CC}=1.65V \sim 5.5V, V_{IN}=5.5V$ or GND, $I_{OUT}=0$			10	μA
Additional Quiescent Supply Current	ΔI_Q	$V_{CC}=3V \sim 5.5V$, One input at $V_{CC}-0.6V$, other inputs at V_{CC} or GND			500	μA
Input Capacitance	C_{IN}	$V_{CC}=3.3V, V_{IN}=V_{CC}$ or GND		3.5		pF

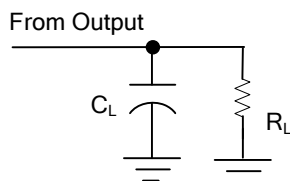
■ DYNAMIC CHARACTERISTICS ($T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (A or B) to output(Y)	t_{PLH}/t_{PHL}	$V_{CC}=1.8V \pm 0.15V, C_L=15pF$	4		16	ns
		$V_{CC}=1.8V \pm 0.15V, C_L=30pF$	4		16	ns
		$V_{CC}=2.5V \pm 0.2V, C_L=15pF$	2.5		7	ns
		$V_{CC}=2.5V \pm 0.2V, C_L=30pF$	3		7.5	ns
		$V_{CC}=3.3V \pm 0.3V, C_L=15pF$	2		5.3	ns
		$V_{CC}=3.3V \pm 0.3V, C_L=50pF$	2		6	ns
		$V_{CC}=5V \pm 0.5V, C_L=15pF$	1.5		4.4	ns
		$V_{CC}=5V \pm 0.5V, C_L=50pF$	2		5	ns

■ OPERATING CHARACTERISTICS ($T_A=25^\circ C$, unless otherwise specified)

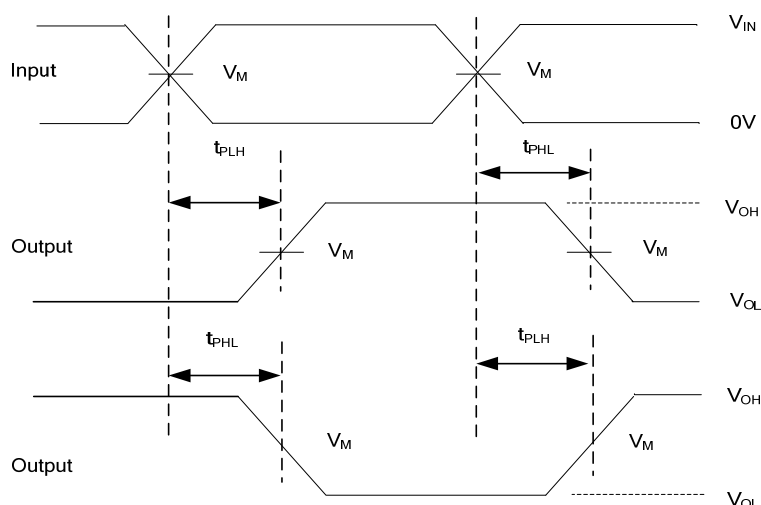
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	$V_{CC}=3.3V, f=10MHz$		18		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

V_{CC}	Inputs		V_M	C_L	R_L
	V_{IN}	t_R, t_F			
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	15pF/30pF	1M Ω /1K Ω
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	15pF/30pF	1M Ω /500 Ω
$3.3V \pm 0.3V$	3V	$\leq 2.5ns$	1.5V	15pF/50pF	1M Ω /500 Ω
$5V \pm 0.5V$	V_{CC}	$\leq 2.5ns$	$V_{CC}/2$	15pF/50pF	1M Ω /500 Ω



PROPAGATION DELAY TIMES

Note: C_L includes probe and jig capacitance.

All input pulses are supplied by generators having the following characteristics: PRR $\leq 10MHz$, $Z_o = 50\Omega$.

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