



U74HC04

CMOS IC

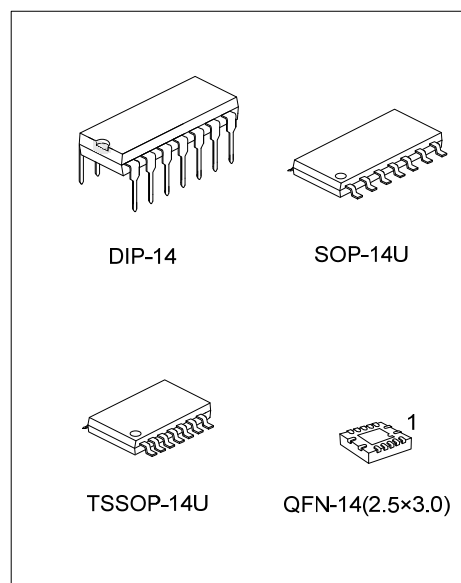
HEX INVERTERS

DESCRIPTION

The **U74HC04** devices contain six independent inverters.
They perform the Boolean function $Y = \overline{A}$ in positive logic.

FEATURES

- * Wide operating voltage range of 2V to 6V
- * Low power consumption, 2μA max. I_{CC}
- * Typical $t_{PD}=8ns$
- * ±4mA Output drive at 4.5V
- * Low input current of 100nA max



ORDERING INFORMATION

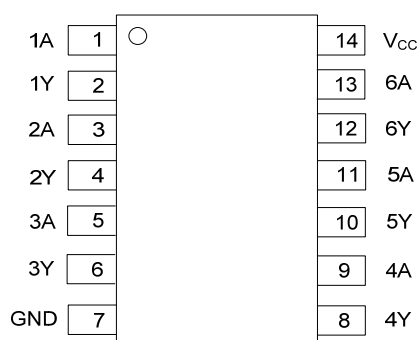
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC04L-D14-T	U74HC04G-D14-T	DIP-14	Tube
U74HC04L-UEA-R	U74HC04G-UEA-R	SOP-14U	Tape Reel
U74HC04L-UEB-R	U74HC04G-UEB-R	TSSOP-14U	Tape Reel
U74HC04L-QAF-R	U74HC04G-QAF-R	QFN-14(2.5×3.0)	Tape Reel

U74HC04G-D14-T (1) Packing Type (2) Package Type (3) Green Package	(1) T: Tube, R: Tape Reel (2) DIP: DIP-14, UEA: SOP-14U, UEB: TSSOP-14U QAF: QFN-14(2.5×3.0) (3) G: Halogen Free and Lead Free, L: Lead Free
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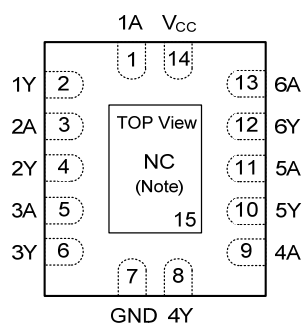
MARKING

PACKAGE	MARKING
DIP-14	
SOP-14U TSSOP-14U	
QFN-14(2.5×3.0)	

PIN CONFIGURATION



SOP-14U / TSSOP-14U



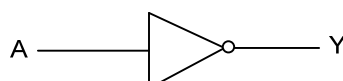
QFN-14(2.5×3.0)

Note: No connect.

FUNCTION TABLE (each gate)

INPUT(A)	OUTPUT(Y)
L	H
H	L

LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING ($T_A = 25^\circ\text{C}$, unless otherwise specified) (Note 2)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7	V
Input Clamp Current	I_{IK}	± 20	mA
Output Clamp Current	I_{OK}	± 20	mA
Output Current	I_{OUT}	± 25	mA
V_{CC} or GND Current	I_{CC}	± 50	mA
Storage Temperature	T_{STG}	-65 ~ +150	$^\circ\text{C}$

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	DIP-14	80	$^\circ\text{C/W}$
	SOP-14U	125	$^\circ\text{C/W}$
	TSSOP-14U	150	$^\circ\text{C/W}$
	QFN-14(2.5×3.0)	130	$^\circ\text{C/W}$

■ RECOMMENDED OPERATING COMDITIONS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	2	5	6	V
Input Voltage	V_I		0		V_{CC}	V
Output Voltage	V_O		0		V_{CC}	V
Input transition rise/fall time	$\Delta t/\Delta v$	$V_{CC}=2V$			1000	ns
		$V_{CC}=4.5V$			500	ns
		$V_{CC}=6V$			400	ns
Operating Temperature	T_A		-40		+125	$^\circ\text{C}$

■ STATIC CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	$V_{CC}=2V$	1.5			V
		$V_{CC}=4.5V$	3.15			V
		$V_{CC}=6V$	4.2			V
Low-Level Input Voltage	V_{IL}	$V_{CC}=2V$			0.5	V
		$V_{CC}=4.5V$			1.35	V
		$V_{CC}=6V$			1.8	V
High-Level Output Voltage	V_{OH}	$V_{CC}=2V, I_{OH}=-20\mu A$	1.9	1.998		V
		$V_{CC}=4.5V, I_{OH}=-20\mu A$	4.4	4.499		V
		$V_{CC}=6V, I_{OH}=-20\mu A$	5.9	5.999		V
		$V_{CC}=4.5V, I_{OH}=-4mA$	3.98	4.3		V
		$V_{CC}=6V, I_{OH}=-5.2mA$	5.48	5.8		V
Low-Level Output Voltage	V_{OL}	$V_{CC}=2V, I_{OL}=20\mu A$		0.002	0.1	V
		$V_{CC}=4.5V, I_{OL}=20\mu A$		0.001	0.1	V
		$V_{CC}=6V, I_{OL}=20\mu A$		0.001	0.1	V
		$V_{CC}=4.5V, I_{OL}=4mA$		0.17	0.26	V
		$V_{CC}=6V, I_{OL}=5.2mA$		0.15	0.26	V
Input Leakage Current	I_I	$V_{CC}=6V, V_I=V_{CC}$ or GND		± 0.1	± 100	nA
Quiescent Supply Current	I_{CC}	$V_{CC}=6V, V_I=V_{CC}$ or GND $I_O=0$			2	μA
Input Capacitance	C_i	$V_{CC}=2V$ to $6V$		3	10	pF

■ DYNAMIC CHARACTERISTICS (Input: $t_R, t_F=6\text{ns}$, $C_L=50\text{pF}$; $\text{PRR}\leq 1\text{MHz}$)

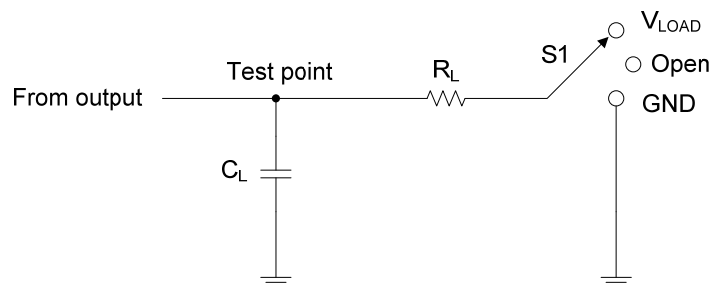
See Fig. 1 and Fig. 2 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (A) to output(Y)	t_{PLH}/t_{PHL}	$V_{CC}=2\text{V}$		45	95	ns
		$V_{CC}=4.5\text{V}$		9	19	ns
		$V_{CC}=6\text{V}$		8	16	ns
Rise/fall time for output(Y)	t_t	$V_{CC}=2\text{V}$		38	75	ns
		$V_{CC}=4.5\text{V}$		8	15	ns
		$V_{CC}=6\text{V}$		6	13	ns

■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No Load		20		pF

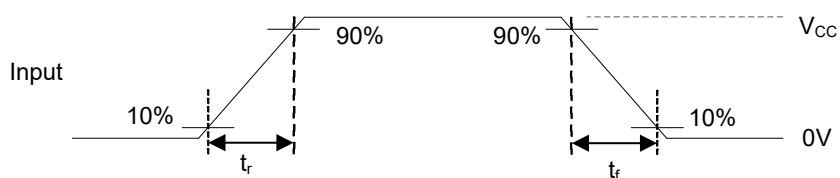
■ TEST CIRCUIT AND WAVEFORMS



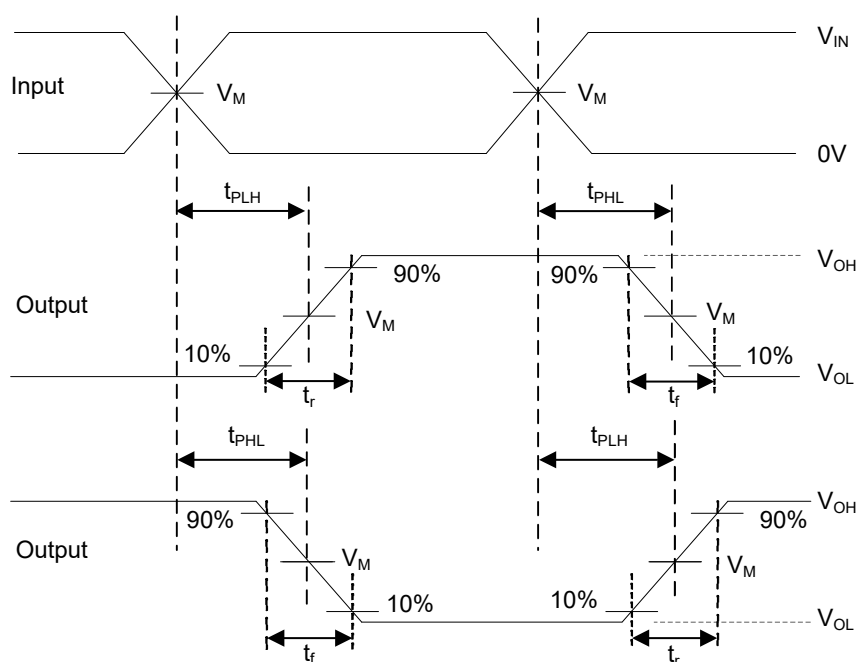
TEST CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open

Inputs		V_M	V_{LOAD}	C_L
V_{IN}	t_r, t_f			
V_{CC}	6 ns	$V_{CC}/2$	V_{CC}	50 pF



**Fig 1. VOLTAGE WAVEFORMS
INPUT RISE AND FALL TIMES**



**Fig 2. VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES**

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