



UZ0107

TRIAC

LOGIC LEVEL FOUR-QUADRANT TRIAC

DESCRIPTION

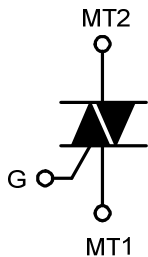
The UTC **UZ0107** is a logic level four-quadrant triac, it uses UTC's advanced technology to provide customers with enhanced current surge capability and high blocking voltage, etc.

The UTC **UZ0107** is suitable for low power AC Fan controllers, industrial process control and general purpose low power motor control, etc.

FEATURES

- * $I_{GT} \leq 5\text{mA}$, $I_{GT} \leq 10\text{mA}$ (T2- G+), $I_{TSM} \leq 12.5\text{A}$ ($t_p=20\text{ms}$)
- $I_{TSM} \leq 13.8\text{A}$ ($t_p=16.7\text{ms}$), $I_{T(RMS)} \leq 1\text{A}$
- * Enhanced current surge capability
- * Direct interfacing to logic level ICs
- * High blocking voltage of 800V
- * Enhanced noise immunity
- * Sensitive gate in four quadrants

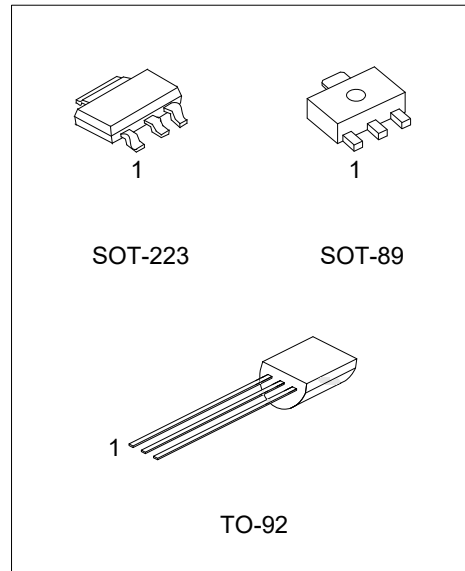
SYMBOL



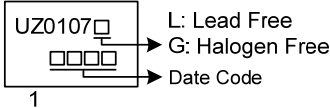
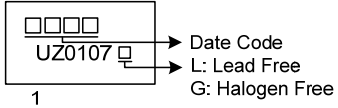
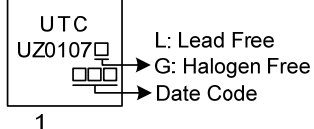
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UZ0107L-x-AA3-R	UZ0107G-x-AA3-R	SOT-223	MT1	MT2	GATE	Tape Reel
UZ0107L-x-AB3-R	UZ0107G-x-AB3-R	SOT-89	MT1	MT2	GATE	Tape Reel
UZ0107L-x-T92-B	UZ0107G-x-T92-B	TO-92	MT1	GATE	MT2	Tape Box
UZ0107L-x-T92-K	UZ0107G-x-T92-K	TO-92	MT1	GATE	MT2	Bulk

<p>UZ0107G-x-AA3-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Peak Voltage</p> <p>(4) Green Package</p>	<p>(1) R: Tape Reel, B: Tape Box, K: Bulk</p> <p>(2) AA3: SOT-223, AB3: SOT-89, T92: TO-92</p> <p>(3) 6: 600V, 8: 800V</p> <p>(4) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING

PACKAGE	MARKING
SOT-223	 <p>UZ0107 □ □ □ □ □ 1</p> <p>L: Lead Free G: Halogen Free Date Code</p>
SOT-89	 <p>□ □ □ □ UZ0107 □ 1</p> <p>Date Code L: Lead Free G: Halogen Free</p>
TO-92	 <p>UTC UZ0107 □ □ □ □ □ 1</p> <p>L: Lead Free G: Halogen Free Date Code</p>

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
Repetitive Peak Off-State Voltage	V_{DRM}/V_{RRM}	Full Sine Wave, $T_{SP} \leq 103^{\circ}\text{C}$			600	V		
					800	V		
Non-Repetitive Peak On-State Current	I_{TSM}	Full Sine Wave, $T_{J(\text{init})}=25^{\circ}\text{C}$, $t_p=20\text{ms}$			12.5	A		
					13.8	A		
RMS On-State Current	$I_{T(\text{RMS})}$	Full Sine Wave, $T_{SP} \leq 103^{\circ}\text{C}$			1	A		
Peak Gate Current	I_{GM}				1	A		
Peak Gate Power	P_{GM}				2	W		
Average Gate Power	$P_{G(\text{AV})}$	Over Any 20ms Period			0.1	W		
Junction Temperature	T_J				125	$^{\circ}\text{C}$		
Storage Temperature	T_{STG}		-40		+150	$^{\circ}\text{C}$		
I^2t for Fusing	I^2t	$t_p=10\text{ms}$, Sine-Wave Pulse			0.78	A^2s		
Rate of Rise Of On-State Current	di_T/dt	$I_T=1\text{A}$, $I_G=20\text{mA}$, $di_G/dt=100\text{mA}/\mu\text{s}$, T2+ G+			50	$\text{A}/\mu\text{s}$		
			$I_T=1\text{A}$, $I_G=20\text{mA}$, $di_G/dt=100\text{mA}/\mu\text{s}$, T2+ G-			50	$\text{A}/\mu\text{s}$	
				$I_T=1\text{A}$, $I_G=20\text{mA}$, $di_G/dt=100\text{mA}/\mu\text{s}$, T2- G-			50	$\text{A}/\mu\text{s}$
					$I_T=1\text{A}$, $I_G=20\text{mA}$, $di_G/dt=100\text{mA}/\mu\text{s}$, T2- G+			20

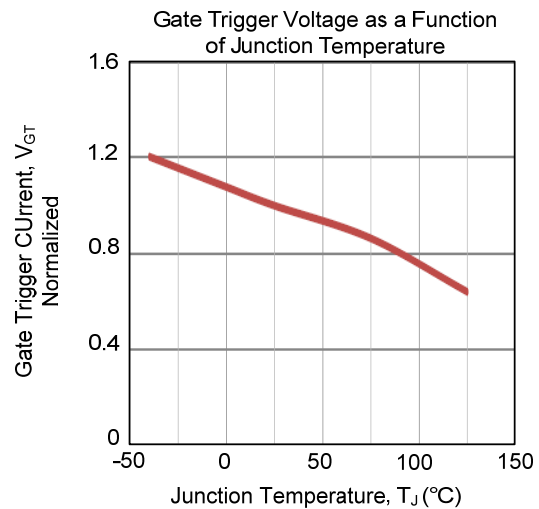
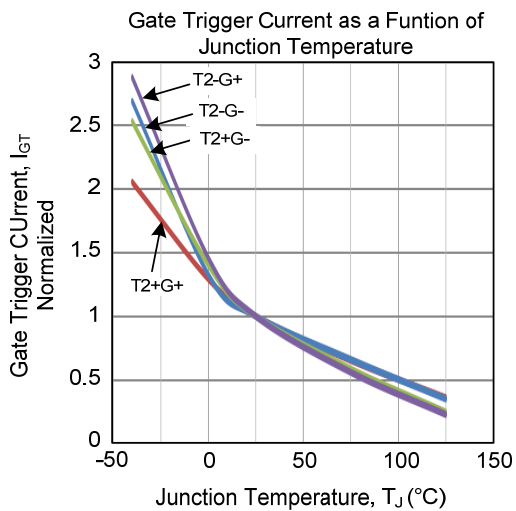
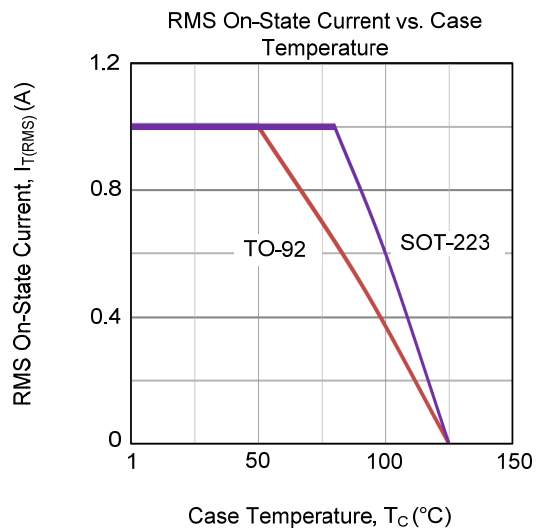
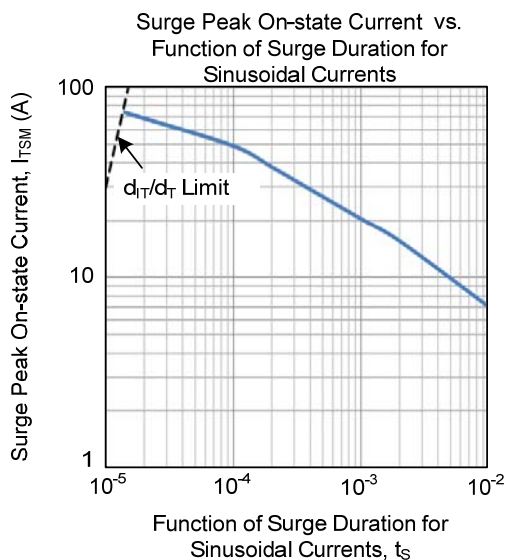
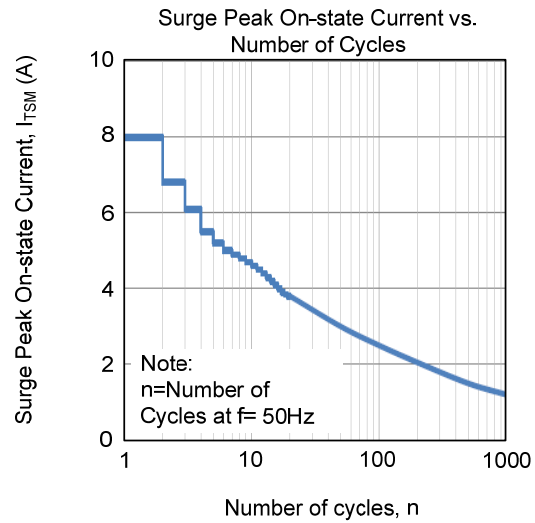
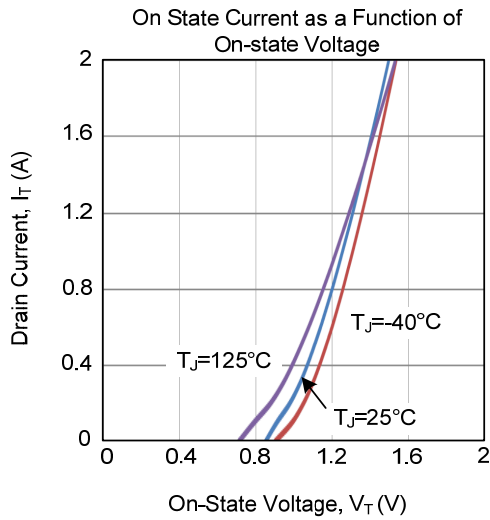
■ THERMAL DATA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal Resistance from Junction to Solder Point	θ_{J-SP}	Full Cycle			15	K/W
Thermal resistance from junction to lead	θ_{J-Lead}				6	K/W
Thermal Resistance from Junction to Ambient	SOT-223	θ_{JA}	Minimum Footprint, Printed-Circuit Board Mounted, in Free Air		156	K/W
				Pad Area, Printed-Circuit Board Mounted, in Free Air		70
	SOT-89	θ_{JA}	Minimum Footprint, Printed-Circuit Board Mounted, in Free Air		200	K/W
	TO-92			Vertical in Free Air		150

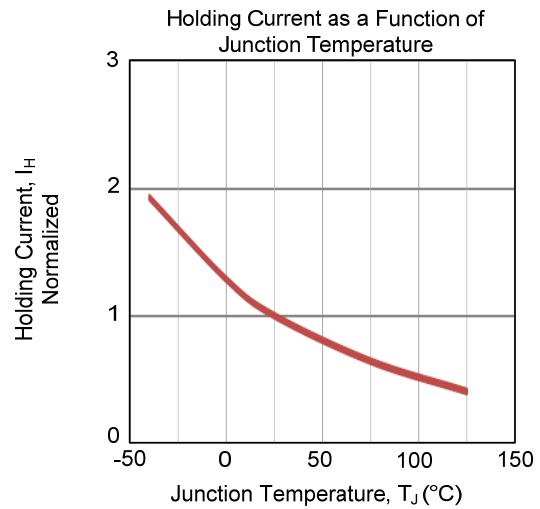
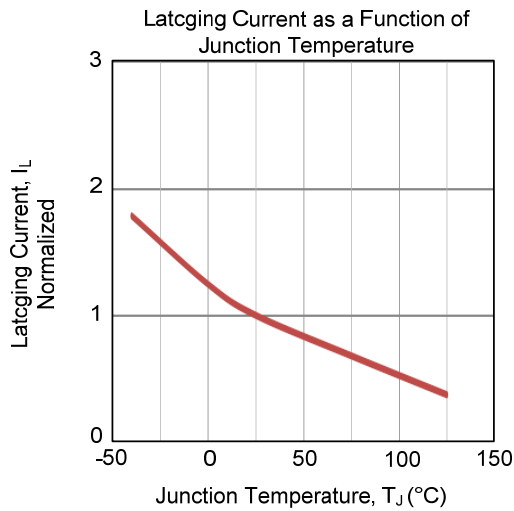
■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gate Trigger Current ($T_J=25^\circ\text{C}$)	I_{GT}	$V_D=12\text{V}$, $I_T=0.1\text{A}$, T2+ G+	0.3		5	mA
		$V_D=12\text{V}$, $I_T=0.1\text{A}$, T2+ G-	0.3		5	mA
		$V_D=12\text{V}$, $I_T=0.1\text{A}$, T2- G-	0.3		5	mA
		$V_D=12\text{V}$, $I_T=0.1\text{A}$, T2- G+	0.3		10	mA
Latching Current ($T_J=25^\circ\text{C}$)	I_L	$V_D=12\text{V}$, $I_G=0.1\text{A}$, T2+ G+			10	mA
		$V_D=12\text{V}$, $I_G=0.1\text{A}$, T2+ G-			25	mA
		$V_D=12\text{V}$, $I_G=0.1\text{A}$, T2- G-			10	mA
		$V_D=12\text{V}$, $I_G=0.1\text{A}$, T2- G+			10	mA
Holding Current	I_H	$V_D=12\text{V}$, $T_J=25^\circ\text{C}$			10	mA
On-State Voltage	V_T	$I_T=1\text{A}$, $T_J=25^\circ\text{C}$		1.3	1.6	V
Gate Trigger Voltage	V_{GT}	$V_D=12\text{V}$, $I_T=0.1\text{A}$, $T_J=25^\circ\text{C}$			1.3	V
		$V_D=V_{DRM}=\text{Rated } V_{DRM} \text{ and } V_{RRM}$ $I_T=0.1\text{A}$, $T_J=125^\circ\text{C}$	0.2			V
Off-State Current	I_D	$V_D=V_{DRM}=\text{Rated } V_{DRM} \text{ and } V_{RRM}$ $R_{GK}=1\text{k}\Omega$, $T_J=125^\circ\text{C}$			0.5	mA
Rate of Rise of Off-State Voltage	dV_D/dt	$V_{DM}=402\text{V}$, $T_J=110^\circ\text{C}$, Gate Open Circuit	100			V/ μs
Rate of Change of Commutating Voltage	dV_{com}/dt	$V_{DM}=400\text{V}$, $T_J=110^\circ\text{C}$, $dI_{com}/dt=0.44\text{A/ms}$, Gate Open Circuit	0.5			V/ μs

■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



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