



## UB209A

Preliminary

CMOS IC

### BATTERY PROTECTION IC WITH CELL-BALANCE FUNCTION

#### DESCRIPTION

The UTC **UB209A** Series is a protection IC for lithium-ion/lithium polymer rechargeable batteries, including a high precision voltage detection circuit and a delay circuit.

The UTC **UB209A** Series has a transmission function and two types of cell-balance function so that users are also able to configure a protection circuit with series multi-cell.

#### FEATURES

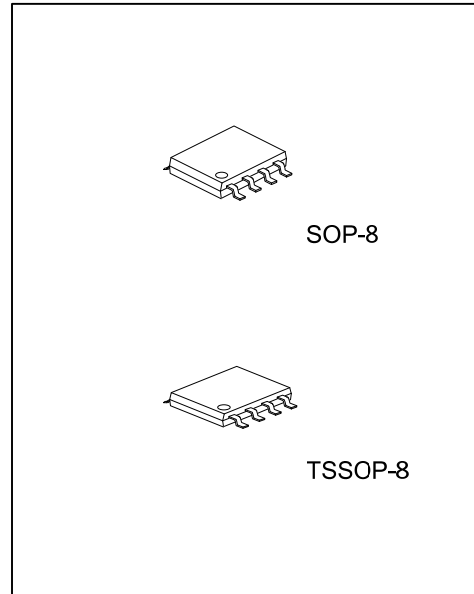
- \* Settable delay time by external capacitor for output pin
- \* High-accuracy voltage detection circuit
- \* Two types of cell-balance function: charge/discharge
- \* Control charging, discharging, cell-balance by CTLC, CTLD pins
- \* Low current consumption: 8.0μA max
- \* Wide range of operation temperature (-40°C ~ +85°C)

#### ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UB209AL-xx-S08-R	UB209AG-xx-S08-R	SOP-8	Tape Reel
UB209AL-xx-P08-R	UB209AG-xx-P08-R	TSSOP-8	Tape Reel

Note: xx: Output Voltage, refer SERIAL CODE LIST.

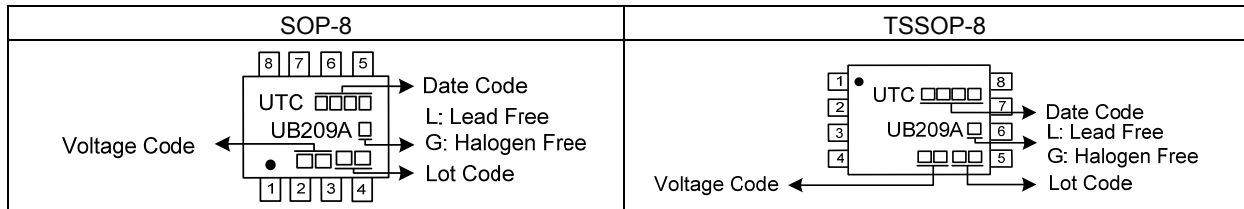
UB209AG-xx-S08-R	(1)Packing Type (2)Package Type (3)Output Voltage Code (4)Green Package	(1) R: Tape Reel (2) S08: SOP-8, P08: TSSOP-8 (3) xx: Refer to SERIAL CODE LIST (4) G: Halogen Free and Lead Free, L: Lead Free
------------------	--	--



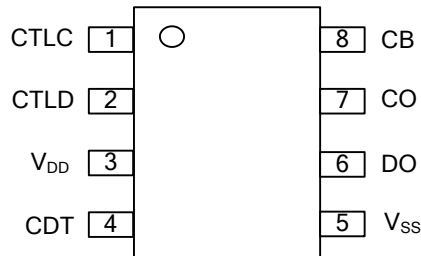
### ■ SERIAL CODE LIST

Model	Code	Overcharge Detection Voltage [V <sub>CU</sub> ](V)	Overcharge Release Voltage [V <sub>CL</sub> ](V)	Cell-balance Detection Voltage [V <sub>BU</sub> ](V)	Cell-balance Release Voltage [V <sub>BL</sub> ](V)	Overdischarge Detection Voltage [V <sub>DL</sub> ](V)	Overdischarge Release Voltage [V <sub>DU</sub> ](V)	Discharge Cell-balance Function
UB209A	AA	4.100	4.000	4.050	4.000	2.50	2.70	Yes
	AB	3.800	3.750	3.650	3.600	2.00	2.50	Yes
	AC	3.900	3.500	3.550	3.550	2.50	2.70	Yes
	AD	4.250	4.100	4.200	4.100	2.50	3.00	Yes
	AE	4.000	3.900	3.950	3.900	2.50	2.70	Yes
	AF	4.250	4.100	4.100	4.000	2.75	3.05	Yes
	AG	3.900	3.600	3.550	3.500	2.00	2.40	Yes
	AH	3.900	3.700	3.600	3.600	2.50	2.80	No
	AI	4.150	4.050	3.900	3.900	3.00	3.30	Yes
	AJ	4.250	4.150	4.100	4.050	2.50	2.80	Yes
AK	4.300	4.200	4.225	4.225	2.00	2.50	Yes	

### ■ MARKING



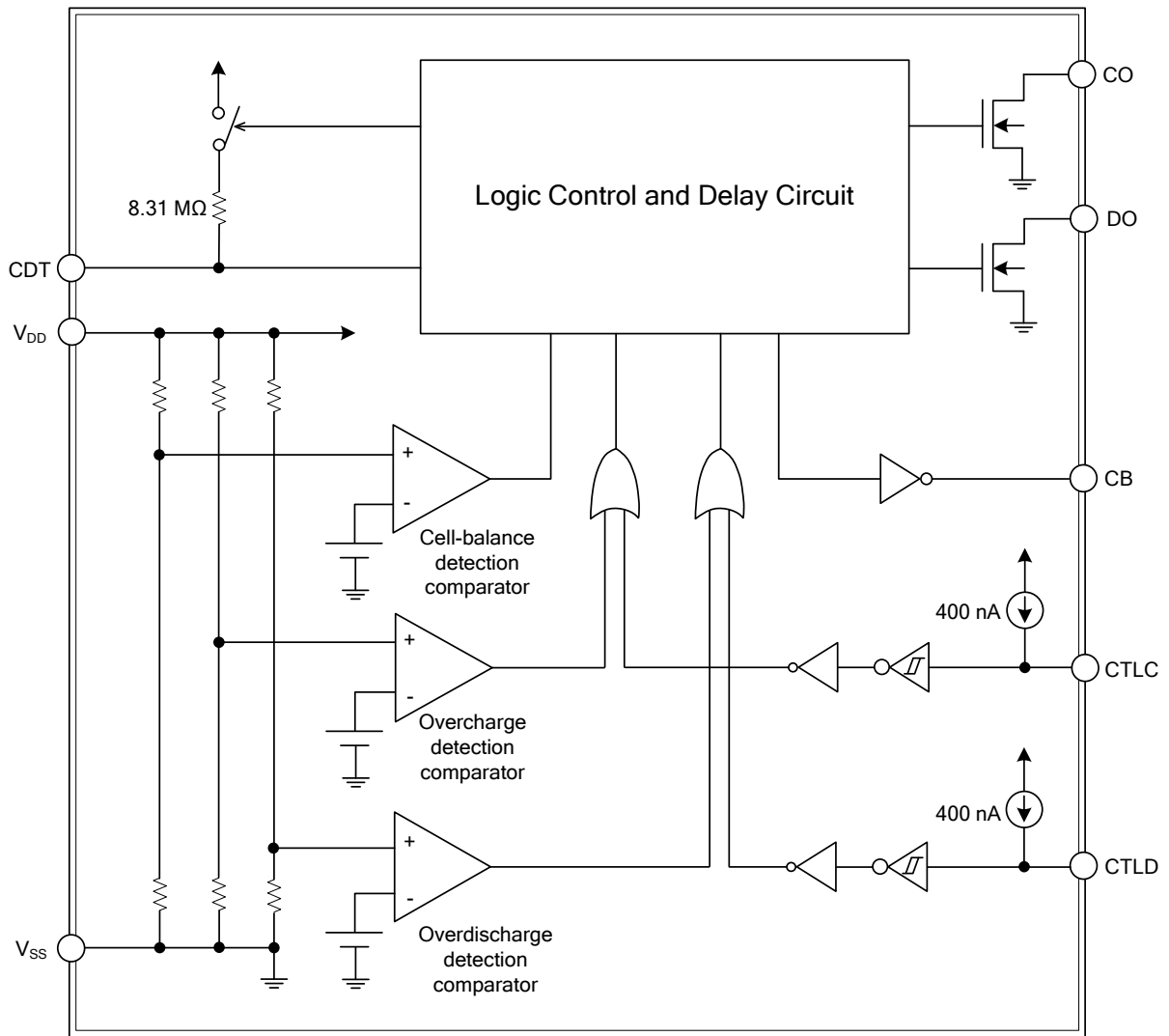
### ■ PIN CONFIGURATION



### ■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	CTLC	Pin for charge control
2	CTLD	Pin for discharge control
3	V <sub>DD</sub>	Connection pin for input positive power supply, for battery's positive voltage
4	CDT	Connection pin to capacitor for overcharge detection delay, for over discharge detection delay
5	V <sub>SS</sub>	Input pin for negative power supply, Connection pin for battery's negative voltage
6	DO	Output pin for discharge control (Nch open drain output)
7	CO	Output pin for charge control (Nch open drain output)
8	CB	Output pin for cell-balance control (CMOS output)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T<sub>A</sub>=25°C unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Input Voltage Between V <sub>DD</sub> and V <sub>SS</sub>		V <sub>DS</sub>	V <sub>SS</sub> -0.3 ~ V <sub>SS</sub> +9.0	V
CB Pin Output Voltage		V <sub>CB</sub>	V <sub>SS</sub> -0.3 ~ V <sub>DD</sub> +0.3	V
CDT Pin Voltage		V <sub>CDT</sub>	V <sub>SS</sub> -0.3 ~ V <sub>DD</sub> +0.3	V
DO Pin Output Voltage		V <sub>DO</sub>	V <sub>SS</sub> -0.3 ~ V <sub>SS</sub> +18	V
CO Pin Output Voltage		V <sub>CO</sub>	V <sub>SS</sub> -0.3 ~ V <sub>SS</sub> +18	V
CTLIC Pin Input Voltage		V <sub>CTLIC</sub>	V <sub>DD</sub> -18 ~ V <sub>DD</sub> +0.3	V
CTLD Pin Input Voltage		V <sub>CTLD</sub>	V <sub>DD</sub> -18 ~ V <sub>DD</sub> +0.3	V
Power Dissipation (Note 2)	SOP-8	P <sub>D</sub>	700	mW
	TSSOP-8		666	mW
Operating Ambient Temperature		T <sub>OPR</sub>	-40 ~ +85	°C
Storage Temperature		T <sub>STG</sub>	-55 ~ +125	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. When mounted on board Size: 114.3mm×76.2mm×1.6mm.

■ ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test circuit
Overcharge Detection Voltage	V <sub>CU</sub>		V <sub>CU</sub> -0.05	V <sub>CU</sub>	V <sub>CU</sub> +0.05	V	1
Overcharge Release Voltage	V <sub>CL</sub>		V <sub>CL</sub> -0.05	V <sub>CL</sub>	V <sub>CL</sub> +0.05	V	1
Cell-balance Detection Voltage	V <sub>BU</sub>		V <sub>BU</sub> -0.05	V <sub>BU</sub>	V <sub>BU</sub> +0.05	V	1
Cell-balance Release Voltage	V <sub>BL</sub>		V <sub>BL</sub> -0.05	V <sub>BL</sub>	V <sub>BL</sub> +0.05	V	1
Over Discharge Detection Voltage	V <sub>DL</sub>		V <sub>DL</sub> -0.10	V <sub>DL</sub>	V <sub>DL</sub> +0.10	V	1
Over Discharge Release Voltage	V <sub>DU</sub>		V <sub>DU</sub> -0.10	V <sub>DU</sub>	V <sub>DU</sub> +0.10	V	1
Detection Delay Time (Note 1)	t <sub>DET</sub>	C <sub>CDT</sub> =0.01μF	50	100	150	ms	2
Release Delay Time	t <sub>REL</sub>	C <sub>CDT</sub> =0.01μF	5	10	15	ms	2
CDT Pin Detection Voltage	V <sub>CDET</sub>	V <sub>DS</sub> =3.5V	V <sub>DS</sub> ×0.65	V <sub>DS</sub> ×0.70	V <sub>DS</sub> ×0.75	V	3
Operating Voltage Between V <sub>DD</sub> and V <sub>SS</sub>	V <sub>DSOP</sub>	Output Voltage of CO, DO, CB Fixed	1.5		8.0	V	
CTLC Pin H Voltage	V <sub>CTLCH</sub>	V <sub>DS</sub> =3.5V	V <sub>DS</sub> ×0.55		V <sub>DS</sub> ×0.90	V	4
CTLD Pin H Voltage	V <sub>CTLDH</sub>	V <sub>DS</sub> =3.5V	V <sub>DS</sub> ×0.55		V <sub>DS</sub> ×0.90	V	4
CTLC Pin L Voltage	V <sub>CTLCL</sub>	V <sub>DS</sub> =3.5V	V <sub>DS</sub> ×0.10		V <sub>DS</sub> ×0.45	V	4
CTLD Pin L Voltage	V <sub>CTLDL</sub>	V <sub>DS</sub> =3.5V	V <sub>DS</sub> ×0.10		V <sub>DS</sub> ×0.45	V	4
Current Consumption During Operation (Note 2)	I <sub>OPE</sub>	V <sub>DS</sub> =3.5V		3.5	8.0	μA	5
Source Current CTLC (Note 2)	I <sub>CTLCH</sub>	V <sub>DS</sub> =3.5V, V <sub>CTLC</sub> =0V	200	400	600	nA	6
Source Current CTLD (Note 2)	I <sub>CTLDH</sub>	V <sub>DS</sub> =3.5V, V <sub>CTLD</sub> =0V	200	400	600	nA	6
Source Current CB	I <sub>CBH</sub>	V <sub>CB</sub> =4.0V, V <sub>DS</sub> =4.5V	30			μA	7
Sink Current CB	I <sub>CBL</sub>	V <sub>CB</sub> =0.5V, V <sub>DS</sub> =3.5V	30			μA	7
Sink Current CO	I <sub>COL</sub>	V <sub>CO</sub> =0.5V, V <sub>DS</sub> =3.5V	30			μA	7
Leakage Current CO	I <sub>COH</sub>	V <sub>CO</sub> =18V, V <sub>DS</sub> =4.5V			0.2	μA	8
Sink Current DO	I <sub>DOL</sub>	V <sub>DO</sub> =0.5V, V <sub>DS</sub> =3.5V	30			μA	7
Leakage Current DO	I <sub>DOH</sub>	V <sub>DO</sub> =18V, V <sub>DS</sub> =1.8V			0.2	μA	8

Notes: 1. In the UTC **UB209A** Series, users are able to set delay time for the output pins. By using the following formula, delay time is calculated with the value of CDT pin's resistance in the IC (R<sub>CDT</sub>) and the value of capacitor set externally at the CDT pin (C<sub>CDT</sub>).

$$t_D [s] = -\ln(1 - V_{CDET}/V_{DS}) \times C_{CDT} [\mu F] \times R_{CDT} [M\Omega]$$

$$= -\ln(1 - 0.7(\text{Typ.})) \times C_{CDT} [\mu F] \times 8.31M\Omega (\text{Typ.})$$

$$= 10.0M\Omega(\text{Typ.}) \times C_{CDT} [\mu F]$$

In case of the capacitance of CDT pin C<sub>CDT</sub>=0.01μF, the output pin delay time t<sub>D</sub> is calculated by using the above formula and as follows.

$$t_D [s] = 10.0M\Omega(\text{Typ.}) \times 0.01\mu F = 0.1s(\text{Typ.})$$

Test the CDT pin detection voltage (V<sub>CDET</sub>) by test circuits shown in this datasheet after applying the power supply while pulling-down the CTLC, CTLD pins to the level of V<sub>SS</sub> pin outside the IC.

2. In case of using CTLC, CTLD pins pulled-down to the level of V<sub>SS</sub> pin externally, the current flows into the V<sub>DD</sub> pin (I<sub>DD</sub>) is calculated by the following formula.

$$I_{DD} = I_{OPE} + I_{CTLCH} + I_{CTLDH}$$

■ TEST CIRCUIT

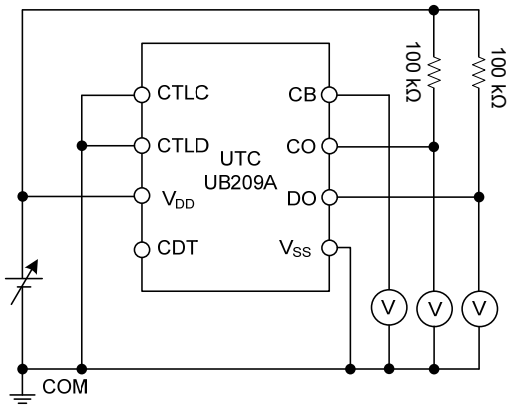


Figure 1. Test Circuit 1

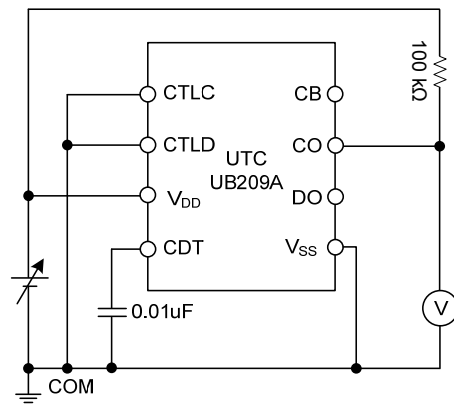


Figure 2. Test Circuit 2

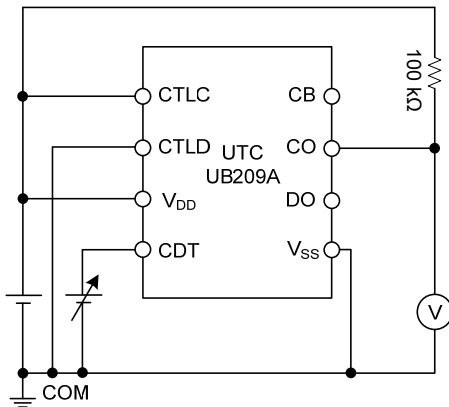


Figure 3. Test Circuit 3

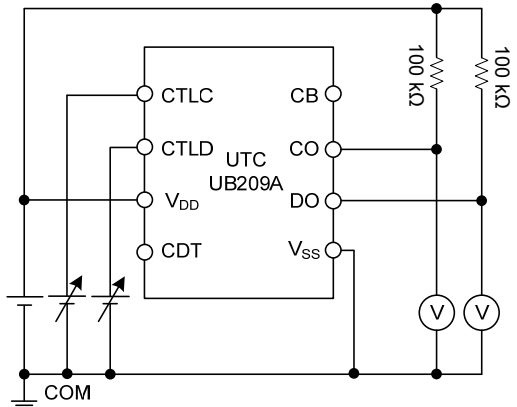


Figure 4. Test Circuit 4

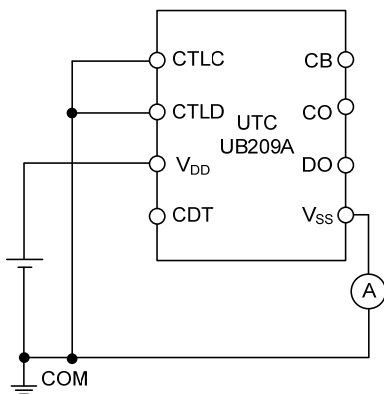


Figure 5. Test Circuit 5

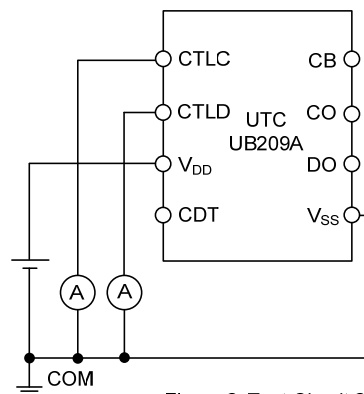


Figure 6. Test Circuit 6

■ TEST CIRCUIT(Cont.)

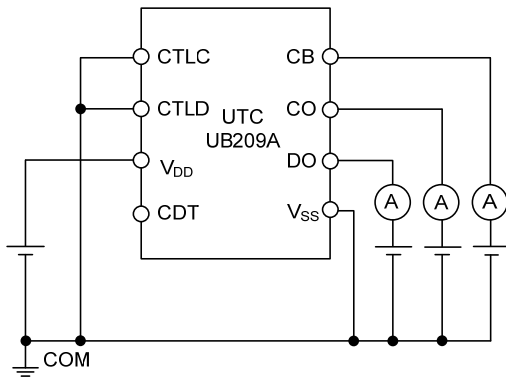


Figure 7. Test Circuit 7

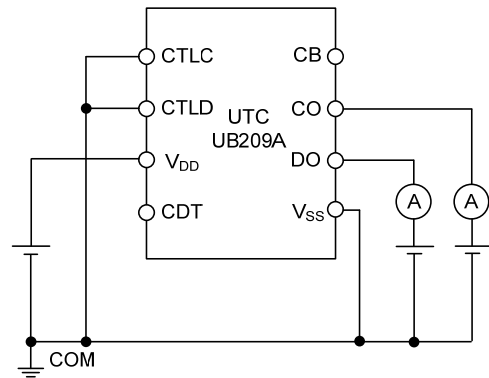


Figure 8. Test Circuit 8

■ OPERATION

Figure 9 shows the operation transition of UTC UB209A.

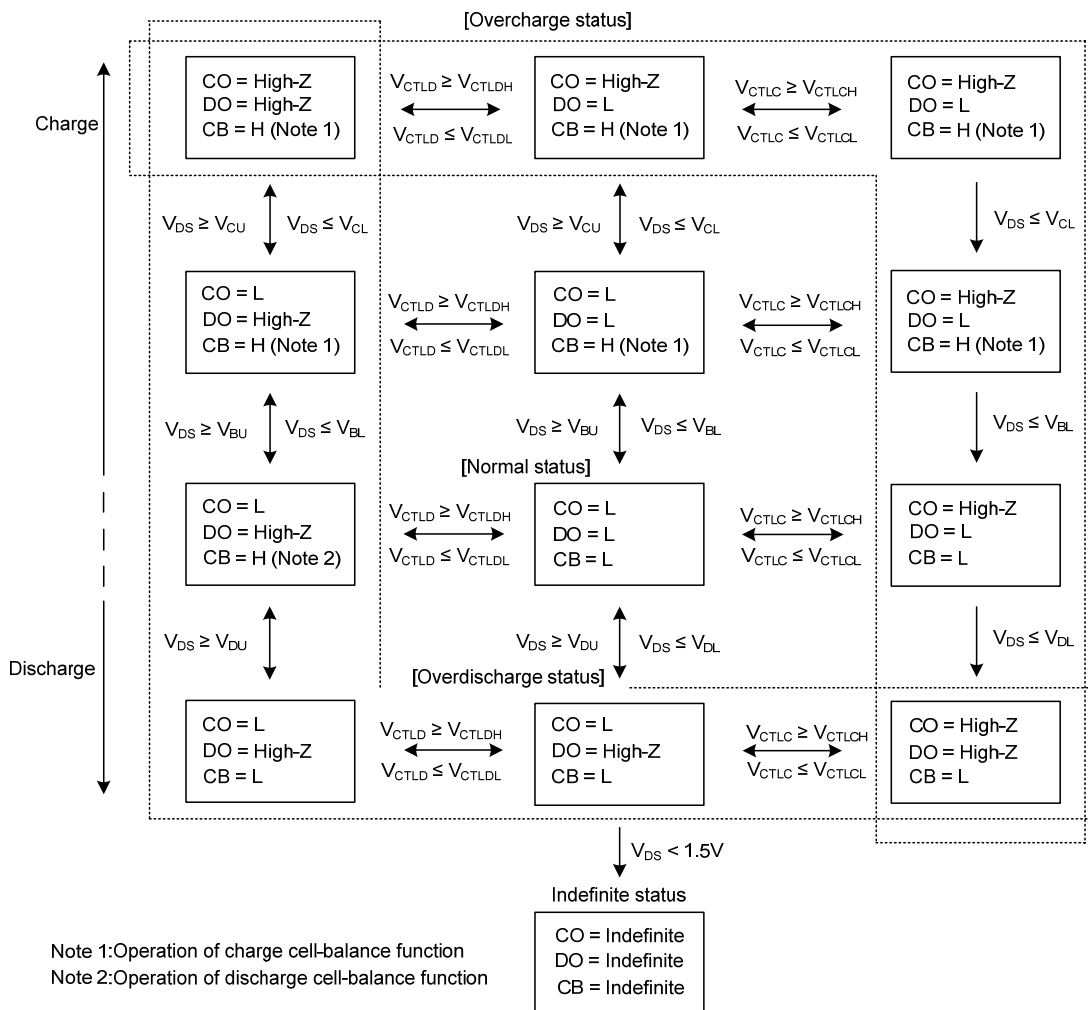


Figure 9. Operation Transition

## ■ OPERATION

### 1. Normal Status

In the UTC **UB209A**, both of CO and DO pin get the  $V_{SS}$  level; the voltage between  $V_{DD}$  and  $V_{SS}$  ( $V_{DS}$ ) is more than the overdischarge detection voltage ( $V_{DL}$ ), and is less than the overcharge detection voltage ( $V_{CU}$ ) and respectively, the CTLC pin input voltage ( $V_{CTLC}$ ) < the CTLC pin voltage "H" ( $V_{CTLCH}$ ), the CTLD pin input voltage ( $V_{CTLD}$ ) < the CTLD pin voltage "H" ( $V_{CTLDH}$ ). This is the normal status.

### 2. Overcharge Status

In the UTC **UB209A**, the CO pin is in high impedance; when  $V_{DS}$  gets  $V_{CU}$  or more, or  $V_{CTLC}$  gets  $V_{CTLCH}$  or more. This is the overcharge status.

If  $V_{DS}$  gets the overcharge release voltage ( $V_{CL}$ ) or less, and  $V_{CTLC}$  gets the CTLC pin voltage "L" ( $V_{CTLCL}$ ) or less, the UTC **UB209A** releases the overcharge status to return to the normal status.

### 3. Overdischarge Status

In the UTC **UB209A**, the DO pin is in high impedance; when  $V_{DS}$  gets  $V_{DL}$  or less, or  $V_{CTLD}$  gets  $V_{CTLDH}$  or more. This is the overdischarge status.

If  $V_{DS}$  gets the overdischarge release voltage ( $V_{DU}$ ) or more, and  $V_{CTLD}$  gets the CTLD pin voltage "L" ( $V_{CTLDL}$ ) or less, the UTC **UB209A** releases the overdischarge status to return to the normal status.

### 4. Cell-balance Function

In the UTC **UB209A**, the CB pin gets the level of  $V_{DD}$  pin; when  $V_{DS}$  gets the cell-balance detection voltage ( $V_{BU}$ ) or more. This is the charge cell-balance function.

If  $V_{DS}$  gets the cell-balance release voltage ( $V_{BL}$ ) or less again, the UTC **UB209A** sets the CB pin the level of  $V_{SS}$  pin.

In addition, the CB pin gets the level of  $V_{DD}$  pin; when  $V_{DS}$  is more than  $V_{DL}$ , and  $V_{CTLD}$  is  $V_{CTLDH}$  or more. This is the discharge cell-balance function.

If  $V_{CTLD}$  gets  $V_{CTLDL}$  or less, or  $V_{DS}$  is  $V_{DL}$  or less again, the UTC **UB209A** sets the CB pin the level of  $V_{SS}$ .

### 5. Delay Circuit

In the UTC **UB209A**, users are able to set delay time which is from detection of changes in  $V_{DS}$ ,  $V_{CTLC}$ ,  $V_{CTLD}$  to output to the CO, DO, CB pin.

For example in the detection of overcharge status, when  $V_{DS}$  exceeds  $V_{CU}$ , or  $V_{CTLC}$  gets  $V_{CTLCH}$  or more, charging to  $C_{CDT}$  starts via  $R_{CDT}$ . If the voltage between CDT and  $V_{SS}$  ( $V_{CDT}$ ) reaches the CDT pin detection voltage ( $V_{CDET}$ ), the CO pin is in high impedance. The output pin delay time  $t_D$  is calculated by the following formula.

$$t_D [s] = 10.0M\Omega (\text{Typ.}) \times C_{CDT} [\mu F]$$

The electric charge in  $C_{CDT}$  starts to be discharged when the delay time has finished.

The delay time that users have set for the CO pin, as seen above, is settable for each output pin DO, CB.



■ TYPICAL APPLICATION CIRCUIT

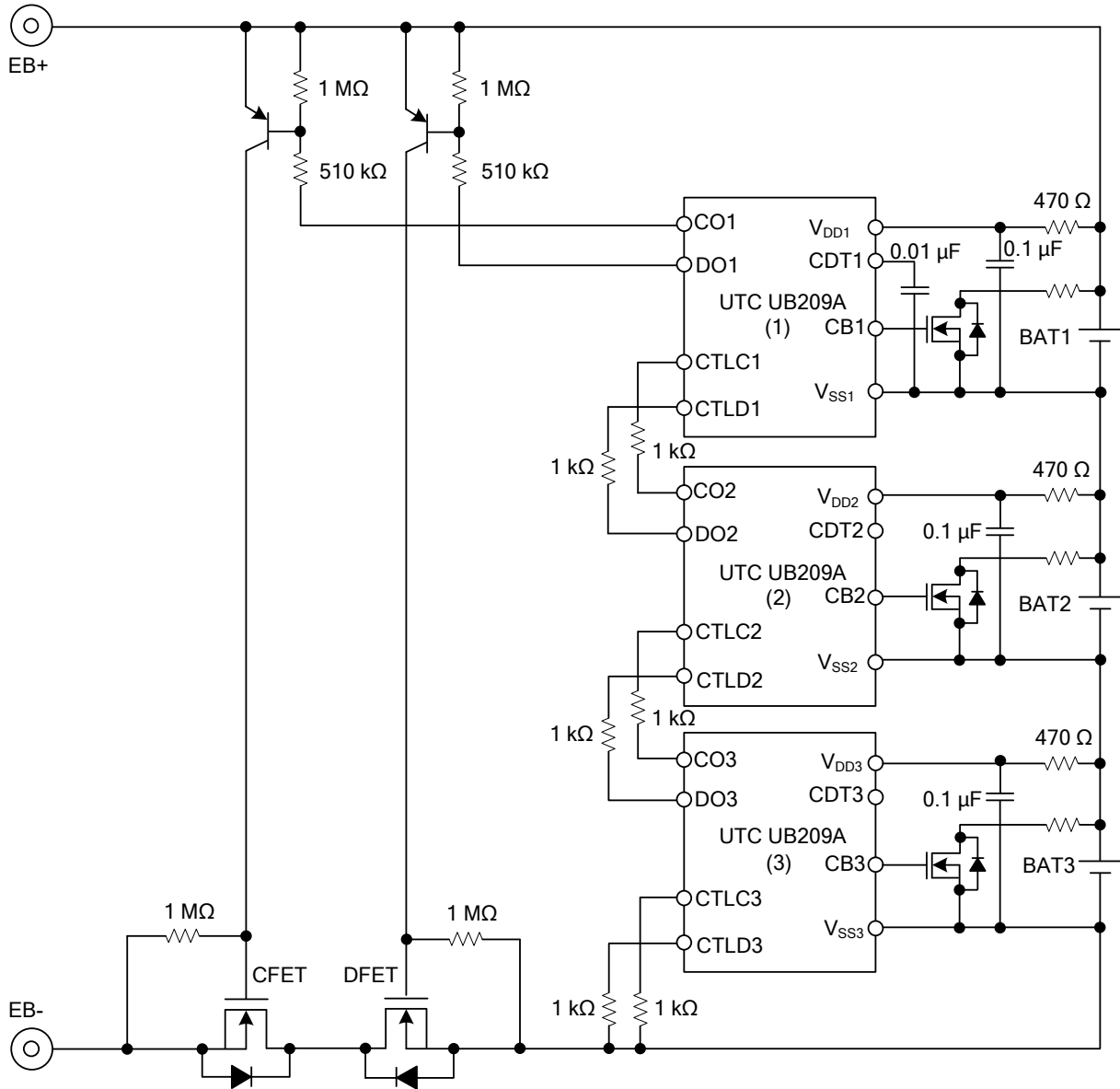


Figure 10

Caution ▮

1. The above constants may be changed without notice.
2. The example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. UTC reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.