



U74ACT125

CMOS IC

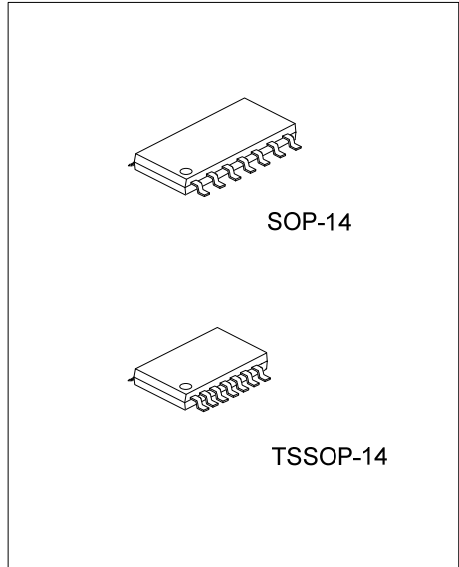
QUAD BUFFER WITH 3-STATE OUTPUTS

DESCRIPTION

The **U74ACT125** contains four independent non-inverting buffers with 3-STATE outputs.

FEATURES

- * Outputs source/sink 24mA
- *ACT125 has TTL-compatible outputs

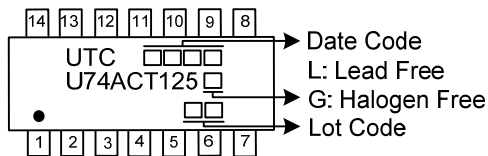


ORDERING INFORMATION

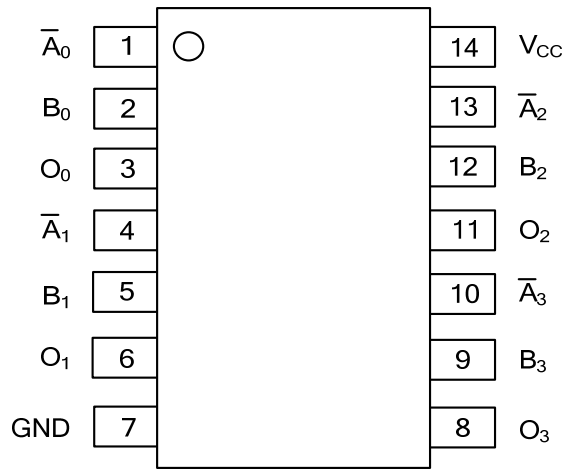
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74ACT125L-UEA-R	U74ACT125G-UEA-R	SOP-14U	Tape Reel
U74ACT125L-UEB-R	U74ACT125G-UEB-R	TSSOP-14U	Tape Reel

<p>U74ACT125G-UEA-R</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) R: Tape Reel (2) UEA: SOP-14U, UEB: TSSOP-14U (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ PIN CONFIGURATION

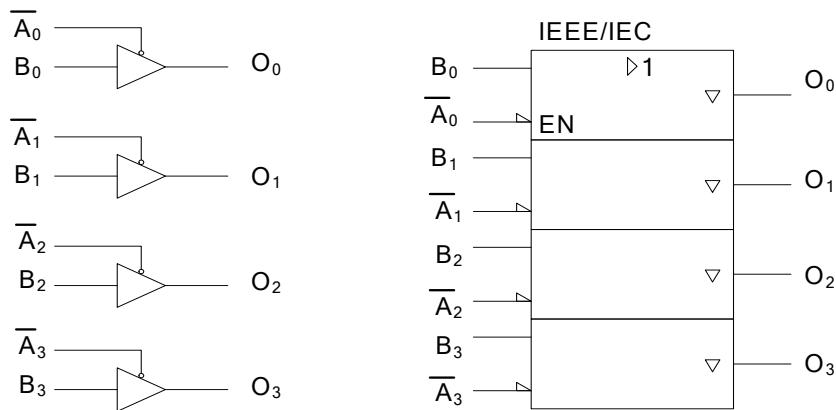


■ FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A_n	B_n	O_n
L	L	L
L	H	H
H	X	Z

H=HIGH Voltage Level; L=LOW Voltage Level
Z=HIGH Impedance; X=Immaterial

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified) (Note 2)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	-0.5 ~ 7.0	V
Input Voltage	V _{IN}	-0.5 ~ V _{CC} +0.5	V
Output Voltage	V _{OUT}	-0.5 ~ V _{CC} +0.5	V
Input Clamp Current (V _{IN} < 0 or V _{IN} > V _{CC})	I _{IK}	±20	mA
Output Clamp Current (V _{OUT} < 0 or V _{OUT} > V _{CC})	I _{OK}	±20	mA
Output Current	I _{OUT}	±50	mA
V _{CC} or GND Current	I _{CC}	±200	mA
Storage Temperature	T _{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	4.5 ~ 5.5	V
Input Voltage	V _{IN}	0 ~ V _{CC}	V
Output Voltage	V _{OUT}	0 ~ V _{CC}	V
Input Transition Rise or Fall Rate	Δt/Δv	8	ns/V
Operating Temperature	T _A	-40 ~ +125	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
High-Level Input Voltage	V _{IH}	V _{CC} =4.5V~5.5V	2			V	
Low-Level Input Voltage	V _{IL}	V _{CC} =4.5V~5.5V			0.8	V	
High-Level Output Voltage	V _{OH}	V _{CC} =4.5V	I _{OH} =-24mA	3.86			V
			I _{OH} =-50μA	4.4	4.49		V
		V _{CC} =5.5V	I _{OH} =-24mA	4.86			V
			I _{OH} =-50μA	5.4	5.49		V
Low-Level Output Voltage	V _{OL}	V _{CC} =4.5V	I _{OL} =24mA			0.36	V
			I _{OL} =50μA		0.001	0.1	V
		V _{CC} =5.5V	I _{OL} =24mA			0.36	V
			I _{OL} =50μA		0.001	0.1	V
Input Leakage Current	I _{I(LEAK)}	V _{CC} = 5.5V, V _{IN} =V _{CC} or GND			±0.1	μA	
Quiescent Supply Current	I _Q	V _{CC} = 5.5V, V _{IN} =5.5V or GND, I _{OUT} =0			4	μA	
Additional Quiescent Supply Current	ΔI _Q	V _{CC} = 5.5V, V _I =V _{CC} -2.1V		0.6		mA	
Input Capacitance	C _{IN}	V _{CC} = OPEN		4.5		pF	
3-STATE Current	I _{OZ}	V _{CC} =5.5V, V _I =V _{IL} , V _{IH} V _O =V _{CC} , GND			±0.5	μA	

■ DYNAMIC CHARACTERISTICS (T_A=25°C, unless otherwise specified)

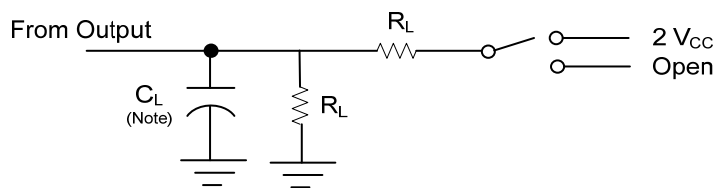
See Fig. 1 and Fig. 2 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Data to Output	t _{PLH}	V _{CC} =5V, t _r = t _r =3ns, C _L =50pF, R _L =500Ω, f=1MHz	1	6.5	9	ns
	t _{PHL}		1	7	9	ns
Output Enable Time	t _{PZH}		1	6.0	8.5	ns
	t _{PZL}		1	7.0	9.5	ns
Output disable Time	t _{PHZ}		1	7.0	9.5	ns
	t _{PLZ}		1	7.5	10	ns

■ OPERATING CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	$V_{CC}=5V$		45		pF

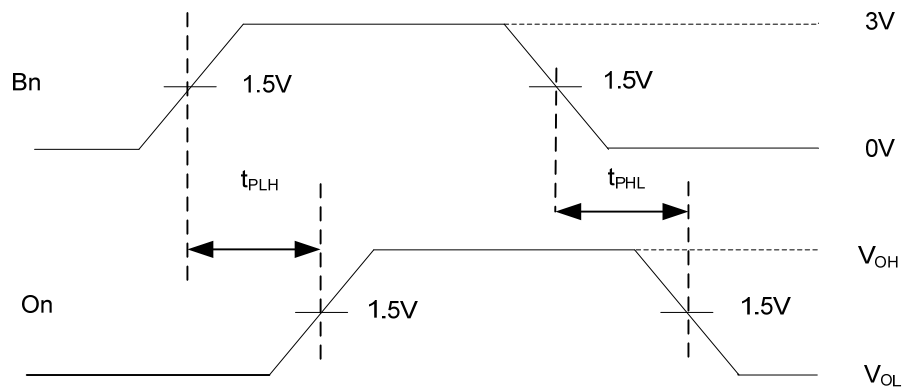
■ TEST CIRCUIT AND WAVEFORMS



Note: C_L includes probe and jig capacitance.

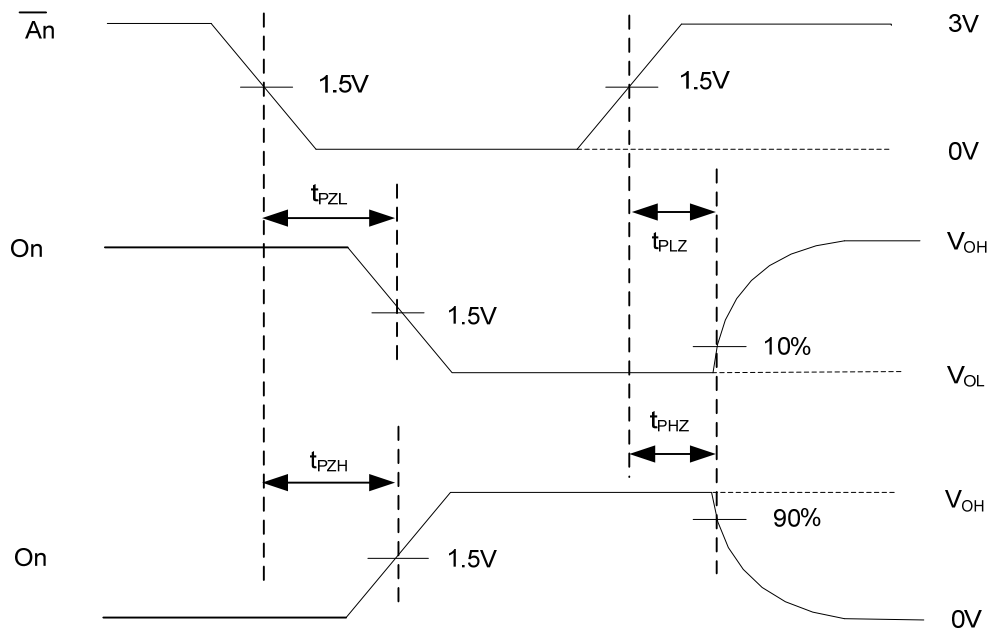
TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PLZ} , t_{PZL}	$2V_{CC}$
t_{PZH} , t_{PHZ}	Open

Fig. 1 Load circuitry for switching times.



PROPAGATION DELAY TIMES

■ TEST CIRCUIT AND WAVEFORMS (Cont.)



ENABLE AND DISABLE TIMES

Fig. 2 Propagation delay from input to output and Output transition time

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