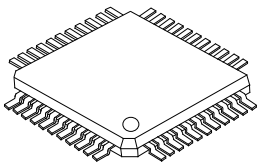
M7206 **CMOS IC**

3 1/2 LCD DISPLAY DRIVER, A/D CONVERTERS



LQFP-44

■ DESCRIPTION

The UTC **M7206** is a 3 1/2 A/D converter IC with low power supply and excellent performance, which also can greatly refrain form interfering. The M7206 combines seven -phase decoder, display driver, reference source, clock system and back light polarity driver, so it can directly drive LCD. Compared with other products, the M7206 adds a new function that can detect on-off state and then alarm.

The **M7206** covers high-precision, good compatibility and low-cost in all. It can achieve auto-zero adjustment error less than 10uV, zero drift within 1uV/°C, input current below 10pA and converter error under 1 count.

■ FEATURES

* On-off state detecting and alarming
* Zero auto-adjustment, guaranteed zero reading with zero input.
* True polarity indication for precision null detection.
* Differential inputs and differential reference.
* Triplex LCD display.
* Convenient 9V battery operation
* CMOS differential inputs for high impedance and null attenuation
* Low noise and A/D converter,
* Low noise A/D converter, stable display.
* Inner clock circuit , can form astable multi-vibrator by connecting passive electronic component.
* Optional exterior clock signal input
* Has triggered buttons that keep and low voltage alarm function that power
* On-chip voltage reference, 60ppm/°C drift.

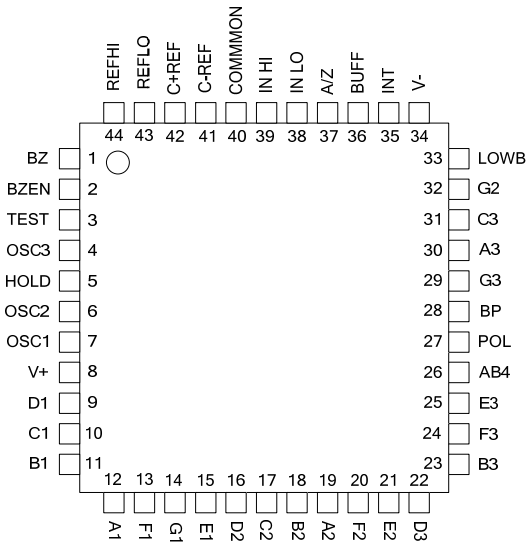
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
M7206L-QL1-Y	M7206G-QL1-Y	LQFP-44	Tray

M7206L-QL1-Y
(1)Packing Type
(2)Package Type
(3)Lead Free

(1) Y: Tray
(2) QL1: LQFP-44
(3) L: Lead Free, G: Halogen Free

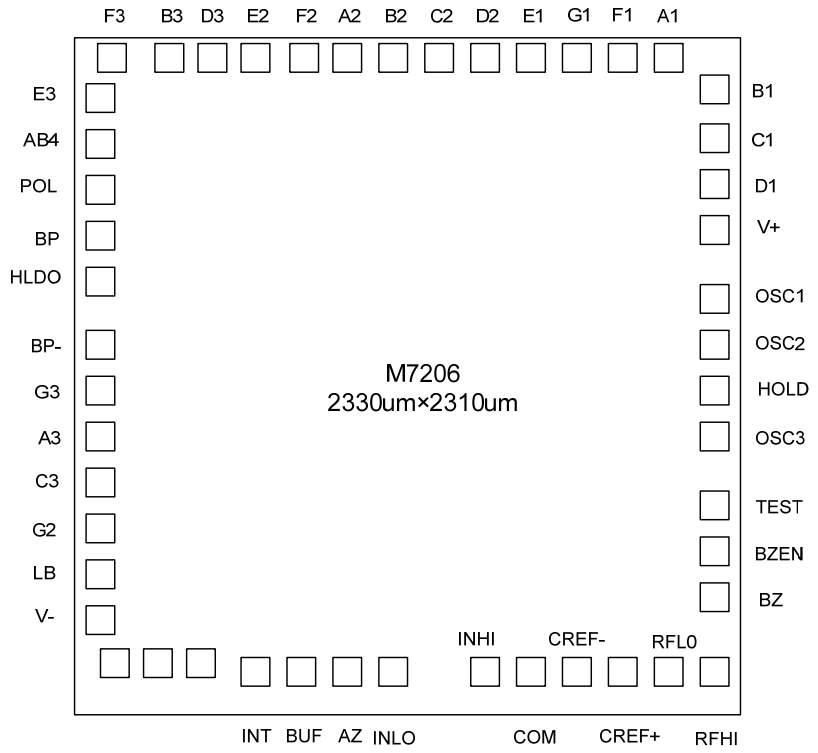
■ PIN CONFIGURATIONS



■ PIN DESCRIPTION

PIN	NAME	TYPE	PIN DESCRIPTION
1	BZ	O	Piezo buzzer output. Whenever BZEN is connected to V+ and differential inputs are tied together, BZ will generate a 5KHz sound output.
2	BZEN	I	Buzzer control slave input. This pin is internally pulled-down to TEST.See BZ
3	TEST	-	Digital GND. Pull high to V+ all LCD segments will be activated.
4	OSC3	-	Crystal oscillator connection. (RC)
5	HOLD	O	Hold control pin. When it receives a negative mud pulse, display hold; Receive again then function disabled.
6	OSC2	-	Crystal oscillator connection. (output)
7	OSC1	-	Crystal oscillator connection. (input)
8	V+	P	Positive supply voltage
9～15	A1~G1	O	LCD segment drive (unit)
16～21、32	A2~G2	O	LCD segment drive (decade)
22~25, 29~31	A3~G3	O	LCD segment drive (hundred)
26	AB4	O	LCD segment drive (thousand). When the readout exceeds 1999, AB4 drive the segment of thousand to display ‘1’ for showing excess.
27	POL	O	LCD segment drive. (minus ‘-‘)
28	BP	O	LCD common drive.
33	LOWB	O	LCD segment drive. (low battery)
34	V-	P	Negative supply voltage. Connecting to battery negative terminal.
35	INT	-	Integrator output.
36	BUFF	-	Integration register connection
37	A/Z	-	Auto-zero capacitor connection
38	IN LO	I	Analog low input signal
39	IN HI	I	Analog high input signal
40	COMMON	O	Set the common-mode voltage for the system
41	C-REF-	-	Negative capacitor connection for on-chip A/D converter
42	C-REF+	-	Positive capacitor connection for on-chip A/D converter
43	REF LO	I	Low differential reference input connection.
44	REF HI	I	High differential reference input connection

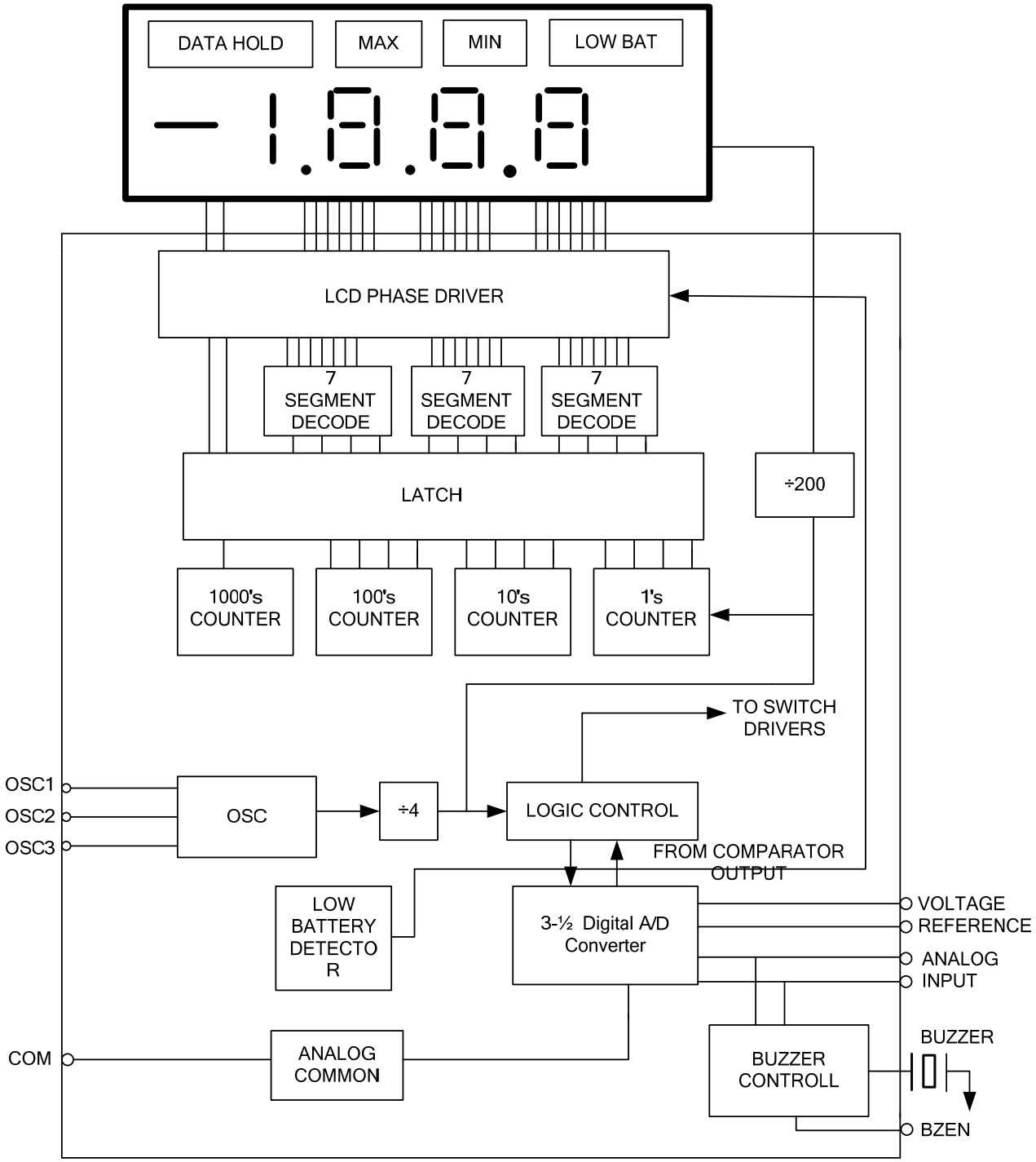
■ PIN FIGURE



■ PIN COORDINATES

PIN	Name	Coordinate		PIN	Name	Coordinate	
		X	Y			X	Y
1	BZ	2135	325	24	F3	130	2115
2	BZEN	2135	475	25	E3	95	1965
3	TEST	2135	625	26	AB4	95	1815
4	OSC3	2135	885	27	POL	95	1665
5	HOLD	2135	1035	28	BP	95	1515
6	OSC2	2135	1185	29	HLDO	95	1365
7	OSC1	2135	1335	30	BP-	95	1165
8	V+	2135	1550	31	G3	95	1015
9	D1	2135	1710	32	A3	95	865
10	C1	2135	1860	33	C3	95	715
11	B1	2135	2010	34	G2	95	565
12	A1	1970	2115	35	LB	95	415
13	F1	1820	2115	36	V-	95	265
14	G1	1670	2115	37	INT	570	95
15	E1	1520	2115	38	BUF	725	95
16	D2	1370	2115	39	AZ	880	95
17	C2	1220	2115	40	IN LO	1030	95
18	B2	1070	2115	41	IN HI	1350	95
19	A2	920	2115	42	COM	1510	95
20	F2	770	2115	43	CREF-	1670	95
21	E2	620	2115	44	CREF+	1820	95
22	D3	470	2115	45	RF LO	1970	95
23	B3	320	2115	46	RF HI	2120	95

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Voltage（V+～V-）	V_{CC}	12	V
Analog input voltage	V_{IANG}	V+~V-	V
Reference Input Voltage	V_{IREF}	V+~V-	V
Operating Temperature Range	T_{OPR}	0 ~ 70	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS

(V_{CC}＝9V, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} Range	V_{CC}			9		V
Supply Current(Does not conclude COMMON current)	I_{CC}	V_{IN}=0V		0.6	1.2	mA
DC characteristics Zero Input Reading		V_{IN}=0V, full-scale=200mV	-000.0	±000.0	+000.0	Digital Reading
Ratio metric Reading		V_{IN}=V_{REF}, V_{REF}=100mV	999	999/ 1000	1001	Digital Reading
Linearity (MAX. deviation form best straight line fit)		full-scale=200.0mV or full-scale=2.0V	-1	± 0.2	+1	Counts
Roll-over Error		-V_{IN}=+V_{IN} ~ 200mV	-1	± 0.2	+1	Counts
Input Leakage Current		V_{IH}=0V		1	10	PA
Low battery flag		V+ to V-	6.6	6.9	7.2	V
Analog Common Voltage (with respect to V+)		25kΩ Between Common and Positive Supply	2.80	3.00	3.20	V

■ TYPICAL APPLICATIONS CIRCUITS

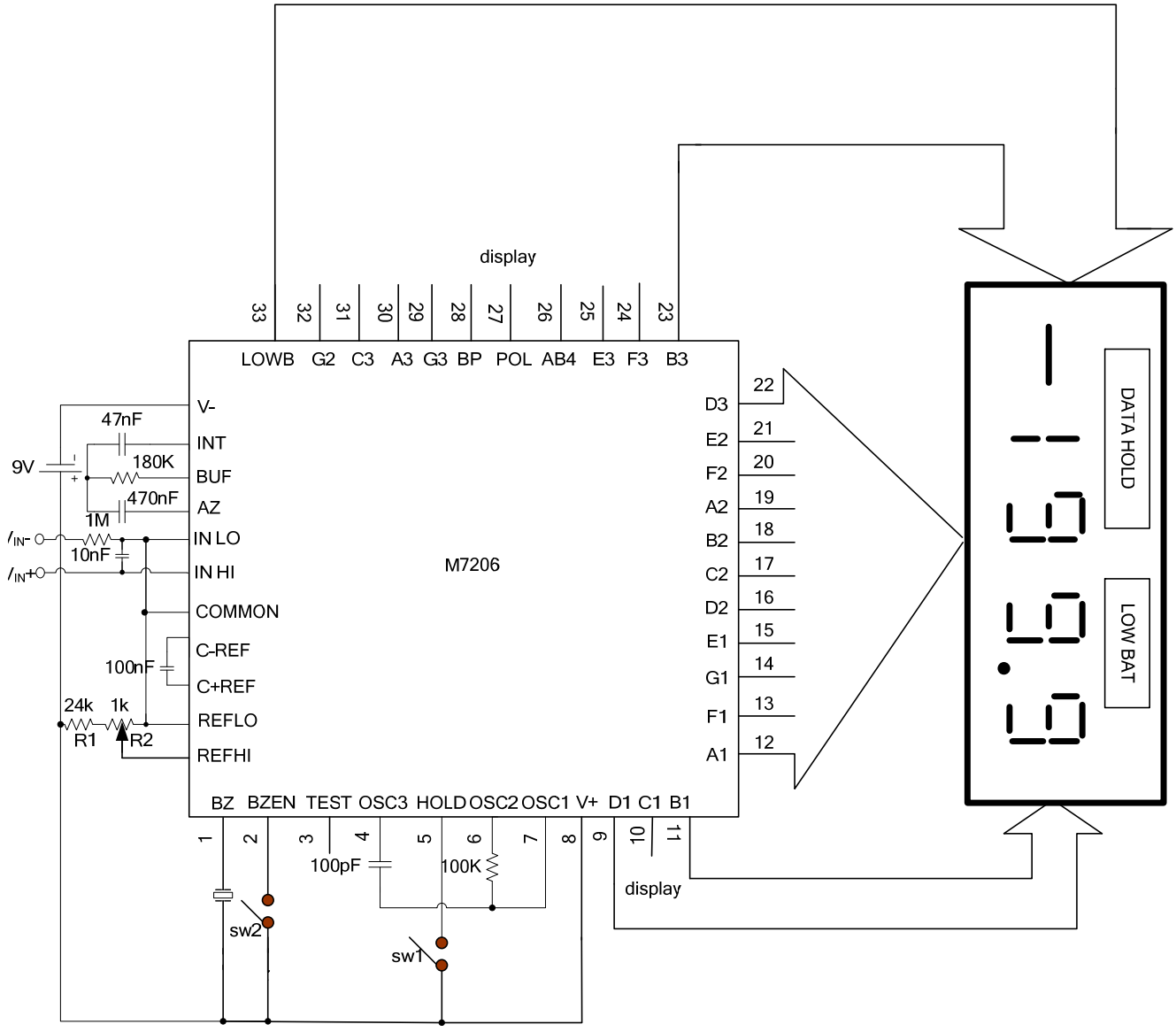


Figure 1

■ Detailed Description

Analog Section

The measurement cycle of analog section is divided into three phases. They are (1)auto-zero(A-Z),(2) signal integrate(INT)and (3) de-integrate(DE).

Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to Analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10uV.

Signal Integrate Phase

During signal integrate the auto-zero loops are opened, the internal short is removed, and the internal inputs high and low are connected to the external pins. The converter then integrates the differential voltage between INHI and INLO for a fixed time. This differential voltage can be within a wide common mode range: up to 1V from either supply. On the other hand, if the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

De-Integrate Phase

The final phase is de-integrated, or reference integrates. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is:

DISPLAY COUNT=1000(V_{IN}/V_{REF})

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 0.5V below the positive supply to 1V above the negative supply. In this range, the system has a CMRR of 86dB typical. However, we must make sure that the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mod e voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain change when called up to de-integrate a positive signal but lose charge when called up to de-integrate a negative input signal. This difference in reference for positive or negative input voltage will give a roll-over error. However, by selecting the reference capacitor such that it is large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count worst case.

Analog Common

The COM pin is used to set the common-mod voltage for the system where the input signals are floating with respect to the power supply. It sets a voltage that is approximately 2.8V lower than the positive supply. In most of the applications, IN LO, RF LO and COM pins are tied to the same point, so that the common mode voltage can be removed from the reference system and the converter.

Within the IC, analog COMMON is tied to an N-Channel FET that can sink approximately 30mA of current to hold the voltage 2.8V below the positive supply (when a load is trying to pull the common voltage toward the positive supply). However, there is only 10μA of source current, so COM voltage is easily tied to a more negative voltage with respect to the positive supply.

■ Detailed Description(Cont.)

TEST

The TEST pin serves two functions. Within IC it is coupled to the internally generated digital supply through an NMOS. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. The second function is a “lamp test”. When TEST is pulled high(to V+)all segment will be turned on and output should be “1888”.

Component Value Selection

Integrating Resistor

Both the buffer amplifier and the integrator have an output stage with 100μA of quiescent current. They can supply 4μA of drive current with negligible nonlinearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full scale, 470kΩ is near optimum and similarly a 47kΩ for a 200mV scale.

Integrating Capacitor

The integrating capacitor should give the maximum voltage swing that ensures tolerance buildup will not saturate the integrator swing (approximately. 0.3V from either supply). When the analog COMMON is used as a reference, a nominal +2V full-scale integrator swing is fine. For three readings /second (48 kHz clock) nominal values for CINT are 0.22μF and 0.10μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is that it must have a low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give the best choice.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.47μF capacitor is recommended. On the 2V scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Oscillator Components

For all ranges of frequency a 100kΩ resistor is recommended and the capacitor is selected from the equation:
$f = 0.45/RC$ For 48kHz clock(3 Reading/sec),
C=100pF.

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1μF will hold the roll-over error to 0.5 count in this instance.

Reference Voltage

The analog input required to generate full scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200mV and 2V scale, V_{REF} should equal 100mV and 1V, respectively. However, in some applications the full-scale input voltage may be other than 200mV or 2V, but 600mV. For example, the reference voltage should be set to 300mV and the input signal can be used directly without being divided.

The differential reference can be used during the measurement of resistor by the ratio metric method and when a digital reading of zero is desired for V_{IN}≠0. A compensating offset voltage can be applied between COM and IN LO and the voltage of being measured is connected between COM and IN HI.