



UNISONIC TECHNOLOGIES CO., LTD

UD6604-H

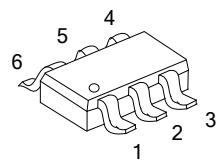
Power MOSFET

20V COMPLEMENTARY MOSFET

■ DESCRIPTION

The UTC **UD6604-H** is a 20V complementary MOSFET, it uses UTC's advanced technology to provide the customers a minimum on state resistance, etc.

The UTC **UD6604-H** is suitable for load switch and battery protection applications.



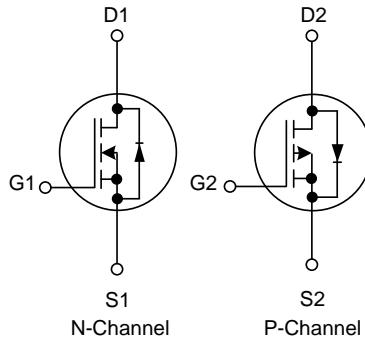
SOT-26

■ FEATURES

- * 3.4A, 20V, $R_{DS(ON)} \leq 40 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=3.4\text{A}$
- $R_{DS(ON)} \leq 55 \text{ m}\Omega$ @ $V_{GS}=2.5\text{V}$, $I_D=3.0\text{A}$
- $R_{DS(ON)} \leq 80 \text{ m}\Omega$ @ $V_{GS}=1.8\text{V}$, $I_D=2.0\text{A}$
- 2.5A, -20V, $R_{DS(ON)} \leq 66\text{m}\Omega$ @ $V_{GS}=-4.5\text{V}$, $I_D=-2.5\text{A}$
- $R_{DS(ON)} \leq 83 \text{ m}\Omega$ @ $V_{GS}=-2.5\text{V}$, $I_D=-2.0\text{A}$
- $R_{DS(ON)} \leq 93 \text{ m}\Omega$ @ $V_{GS}=-1.8\text{V}$, $I_D=-1.0\text{A}$

* Low $R_{DS(ON)}$

■ SYMBOL



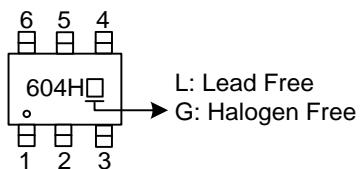
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment						Packing
Lead Free	Halogen Free		1	2	3	4	5	6	
UD6604G-AG6-R	UD6604G-AG6-R	SOT-26	G1	S2	G2	D2	S1	D1	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UD6604G-AG6-R	(1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) AG6: SOT-26 (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING



■ **ABSOLUTE MAXIMUM RATINGS** ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	RATINGS		UNIT
		N-CHANNEL	P-CHANNEL	
Drain-Source Voltage	V_{DSS}	20	-20	V
Gate-Source Voltage	V_{GSS}	± 8	± 8	V
Continuous Drain Current	I_D	3.4	-2.5	A
		2.5	-2	A
Pulsed Drain Current (Note 3)	I_{DM}	13	-13	A
Power Dissipation (Note 2)	P_D	1.1	1.1	W
		0.7	0.7	W
Operating Temperature Range	T_J	-55 ~ +150		°C
Storage Temperature Range	T_{STG}	-55 ~ +150		°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **THERMAL CHARACTERISTICS**

PARAMETER	SYMBOL	TYP	MAX	UNIT
Junction-to-Ambient (Note 1)	θ_{JA}	78	110	°C/W
Junction-to-Ambient (Note 1, 4)		106	150	°C/W

■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^\circ\text{C}$ unless otherwise noted)

N-CHANNEL

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	20			V
Zero Gate Voltage Drain Current	$I_{\text{DS}}^{\text{SS}}$	$V_{DS}=20\text{V}, V_{GS}=0\text{V}$			1	μA
		$V_{DS}=20\text{V}, V_{GS}=0\text{V}, T_J=55^\circ\text{C}$			5	μA
Gate-Source Leakage Current	Forward Reverse	$V_{GS}=+8\text{V}, V_{DS}=0\text{V}$ $V_{GS}=-8\text{V}, V_{DS}=0\text{V}$			+100 -100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(\text{TH})}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.4	0.7	1	V
On State Drain Current	$I_{D(\text{ON})}$	$V_{GS}=4.5\text{V}, V_{DS}=5\text{V}$	13			A
		$V_{GS}=4.5\text{V}, I_D=3.4\text{A}$			40	$\text{m}\Omega$
Static Drain-Source On-State Resistance		$V_{GS}=4.5\text{V}, I_D=3.4\text{A}, T_J=125^\circ\text{C}$			85	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_D=3.0\text{A}$			55	$\text{m}\Omega$
		$V_{GS}=1.8\text{V}, I_D=2.0\text{A}$			80	$\text{m}\Omega$
Forward Transconductance	g_{FS}	$V_{DS}=5\text{V}, I_D=3.4\text{A}$		16		S
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f=1.0\text{MHz}$		290		pF
Output Capacitance	C_{OSS}			45		pF
Reverse Transfer Capacitance	C_{RSS}			40		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{GS}=4.5\text{V}, V_{DS}=10\text{V}, I_D=4\text{A}$		5.5		nC
Gate to Source Charge	Q_{GS}			1		nC
Gate to Drain Charge	Q_{GD}			0.6		nC
Turn-ON Delay Time	$t_{D(\text{ON})}$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=1\text{A}$ $R_G=25\Omega$		2.9		ns
Turn-ON Rise Time	t_R			8.4		ns
Turn-OFF Delay Time	$t_{D(\text{OFF})}$			19.2		ns
Turn-OFF Fall-Time	t_F			5.6		ns
SOURCE TO DRAIN DIODE SPECIFICATIONS						
Diode Forward Voltage	V_{SD}	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.7	1	V
Maximum Body-Diode Continuous Current	I_S				1.5	A
Body Diode Reverse Recovery Time	t_{rr}	$I_F=3.4\text{A}, dI/dt=100\text{A}/\mu\text{s}$		14	19	ns
Body Diode Reverse Recovery Charge	Q_{rr}			3.8		nC

- Notes:
1. The value of θ_{JA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design.
 2. The power dissipation P_D is based on $T_{J(\text{MAX})}=150^\circ\text{C}$, using $\leq 10\text{s}$ junction-to-ambient thermal resistance.
 3. Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})}=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.
 4. The θ_{JA} is the sum of the thermal impedance from junction to lead θ_{JL} and lead to ambient.

■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^\circ\text{C}$ unless otherwise noted)

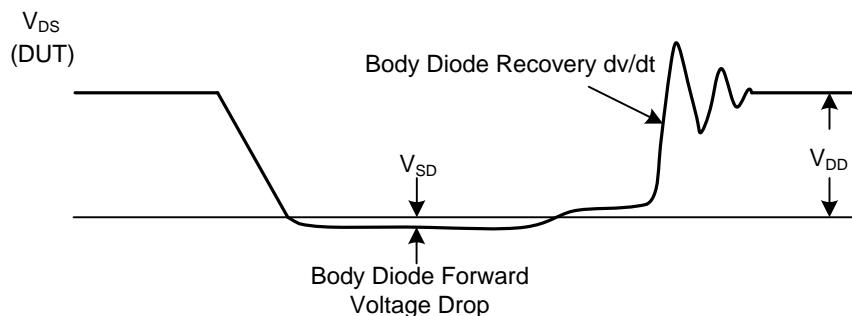
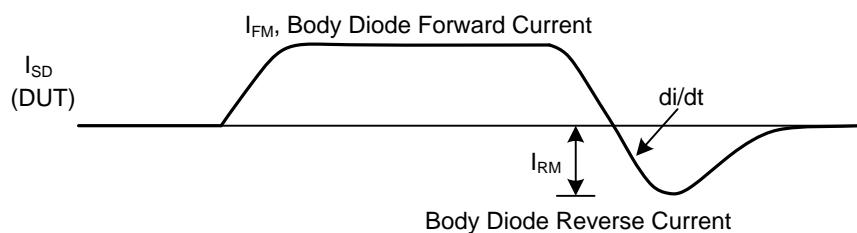
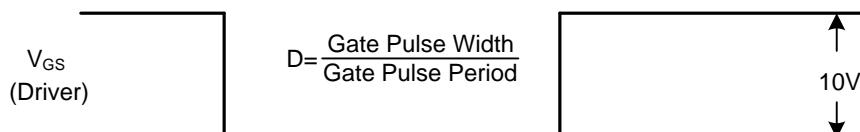
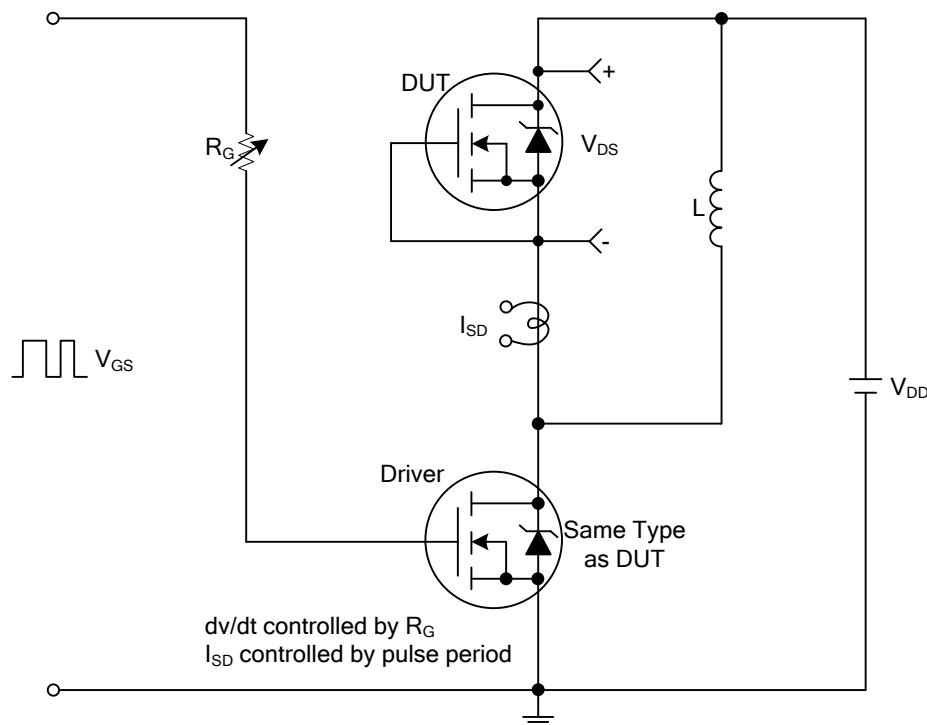
P-CHANNEL

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=-250\mu\text{A}, V_{GS}=0\text{V}$	-20			V
Zero Gate Voltage Drain Current	$I_{\text{DS}S}$	$V_{DS}=-20\text{V}, V_{GS}=0\text{V}$			-1	μA
		$V_{DS}=-20\text{V}, V_{GS}=0\text{V}, T_J=55^\circ\text{C}$			-5	μA
Gate-Source Leakage Current	I_{GSS}	Forward $V_{GS}=+8\text{V}, V_{DS}=0\text{V}$			+100	nA
Reverse $V_{GS}=-8\text{V}, V_{DS}=0\text{V}$					-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(\text{TH})}$	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-0.4	-0.65	-1	V
On State Drain Current	$I_{\text{D}(\text{ON})}$	$V_{GS}=-4.5\text{V}, V_{DS}=-5\text{V}$	-13			A
	$R_{\text{DS}(\text{ON})}$	$V_{GS}=-4.5\text{V}, I_D=-2.5\text{A}$			66	$\text{m}\Omega$
		$V_{GS}=-4.5\text{V}, I_D=-2.5\text{A}, T_J=125^\circ\text{C}$			105	$\text{m}\Omega$
		$V_{GS}=-2.5\text{V}, I_D=-2.0\text{A}$			83	$\text{m}\Omega$
		$V_{GS}=-1.8\text{V}, I_D=-1.0\text{A}$			93	$\text{m}\Omega$
Forward Transconductance	g_{FS}	$V_{DS}=-5\text{V}, I_D=-2.5\text{A}$		13		S
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}, V_{DS}=-15\text{V}, f=1.0\text{MHz}$		290		pF
Output Capacitance	C_{OSS}			45		pF
Reverse Transfer Capacitance	C_{RSS}			40		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{GS}=-4.5\text{V}, V_{DS}=-10\text{V}, I_D=-3\text{A}$		5.5		nC
Gate to Source Charge	Q_{GS}			1		nC
Gate to Drain Charge	Q_{GD}			0.6		nC
Turn-ON Delay Time	$t_{\text{D}(\text{ON})}$	$V_{DS}=-10\text{V}, V_{GS}=-4.5\text{V}, I_D=1\text{A}$ $R_G=25\Omega$		5		ns
Turn-ON Rise Time	t_R			17.4		ns
Turn-OFF Delay Time	$t_{\text{D}(\text{OFF})}$			40.7		ns
Turn-OFF Fall-Time	t_F			11.4		ns
SOURCE TO DRAIN DIODE SPECIFICATIONS						
Diode Forward Voltage	V_{SD}	$I_S=-1\text{A}, V_{GS}=0\text{V}$		-0.7	-1	V
Maximum Body-Diode Continuous Current	I_S				-1.5	A
Body Diode Reverse Recovery Time	t_{rr}	$I_F=-2.5\text{A}, dI/dt=100\text{A}/\mu\text{s}$		37	49	ns
Body Diode Reverse Recovery Charge	Q_{rr}			27		nC

- Notes:
1. The value of θ_{JA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design.
 2. The power dissipation P_D is based on $T_{J(\text{MAX})}=150^\circ\text{C}$, using $\leq 10\text{s}$ junction-to-ambient thermal resistance.
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 4. The θ_{JA} is the sum of the thermal impedance from junction to lead θ_{JL} and lead to ambient.

■ TEST CIRCUITS AND WAVEFORMS

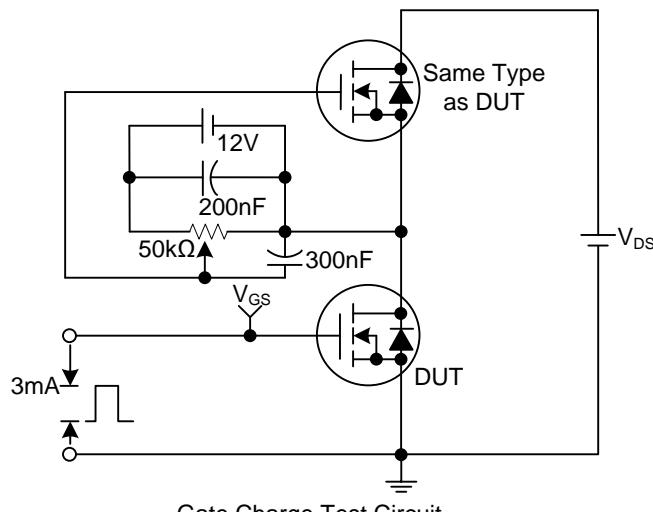
N-CHANNEL



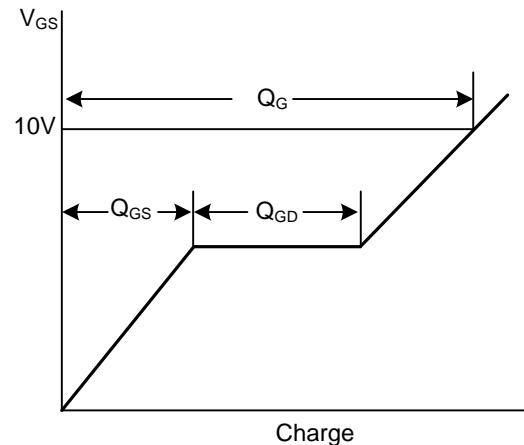
Peak Diode Recovery dv/dt Test Circuit and Waveforms

■ TEST CIRCUITS AND WAVEFORMS

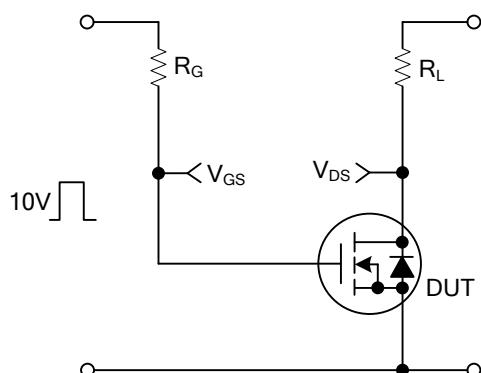
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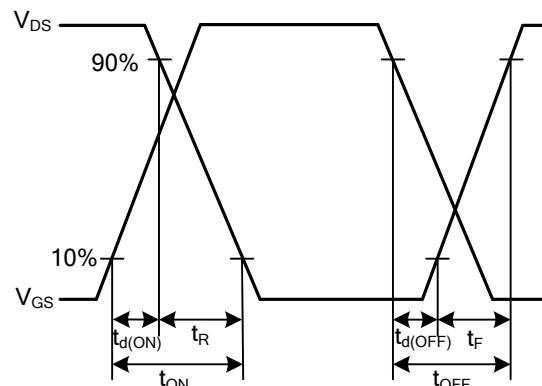
Gate Charge Test Circuit



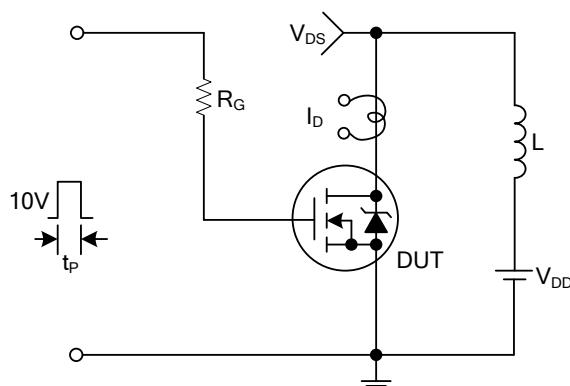
Gate Charge Waveforms



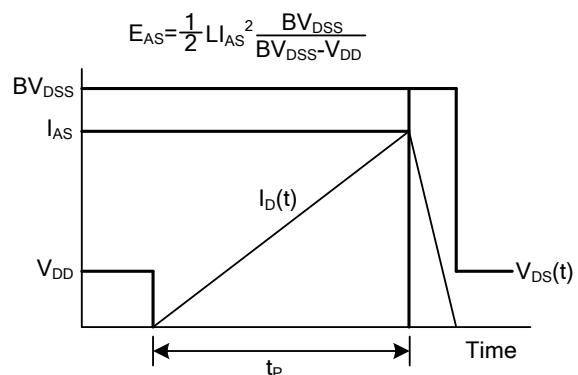
Resistive Switching Test Circuit



Resistive Switching Waveforms



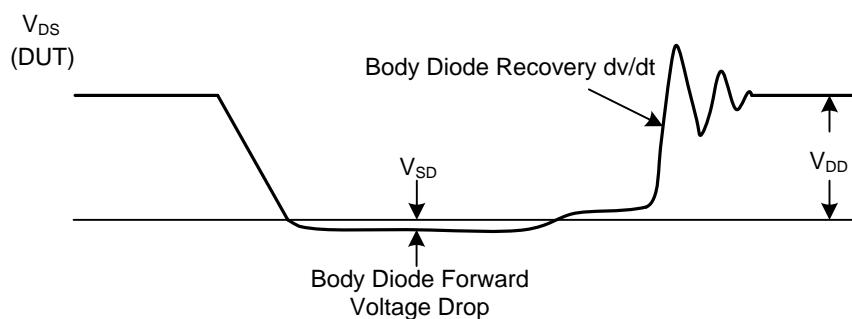
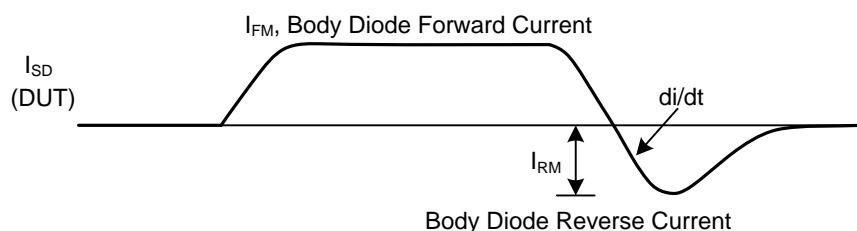
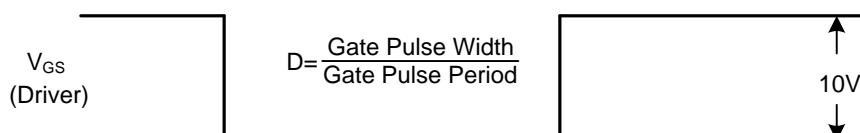
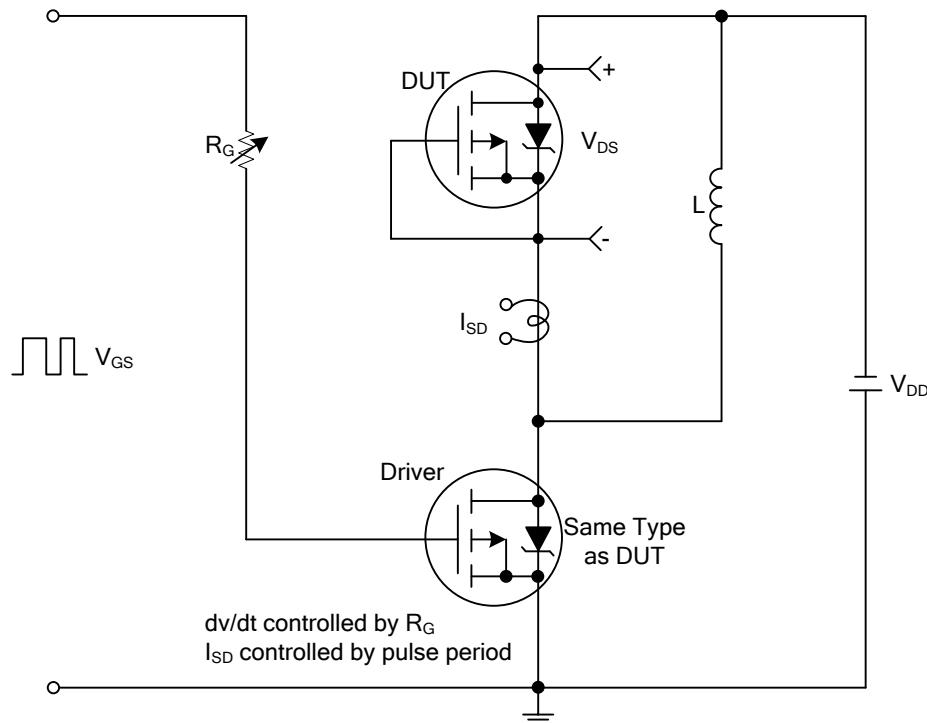
Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

■ TEST CIRCUITS AND WAVEFORMS

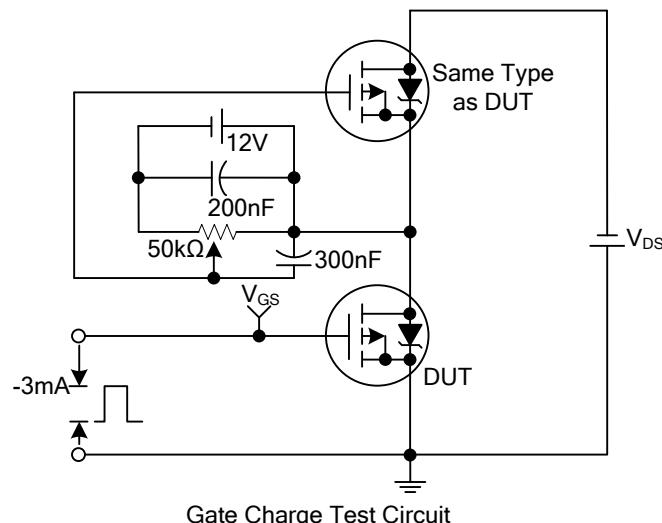
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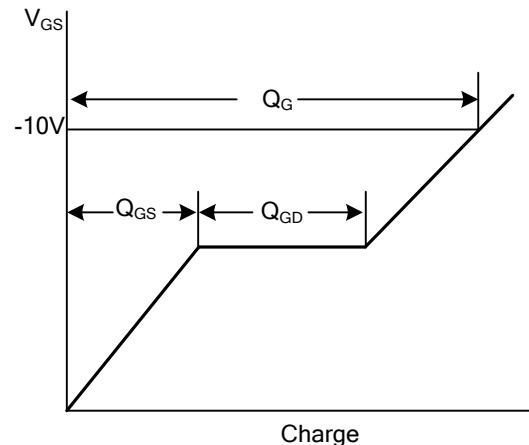
Peak Diode Recovery dv/dt Test Circuit and Waveforms

■ TEST CIRCUITS AND WAVEFORMS

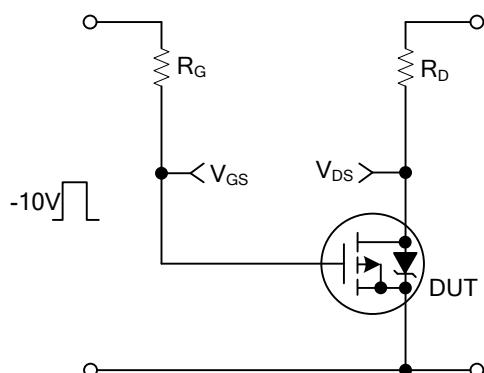
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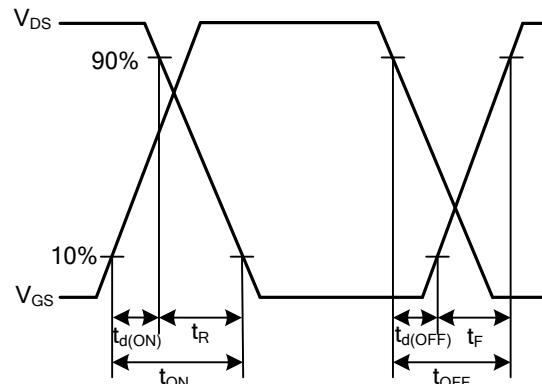
Gate Charge Test Circuit



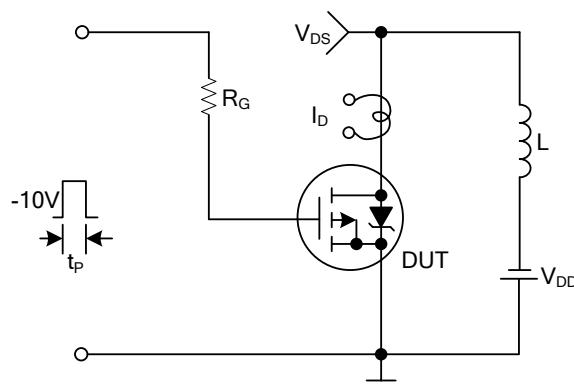
Gate Charge Waveforms



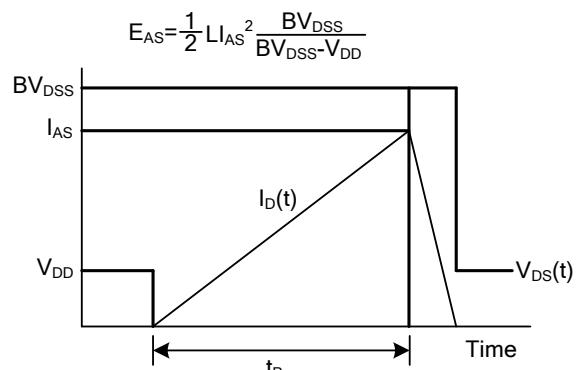
Resistive Switching Test Circuit



Resistive Switching Waveforms



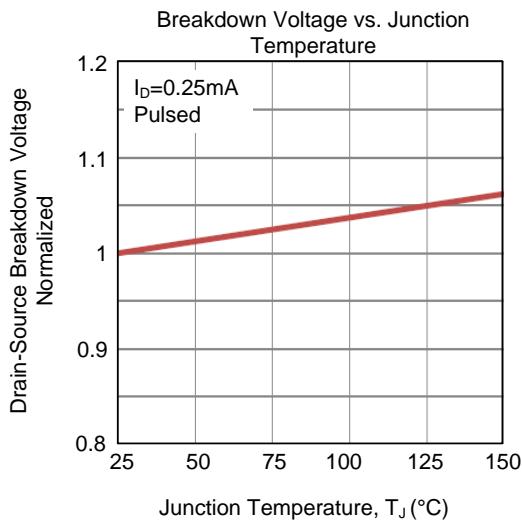
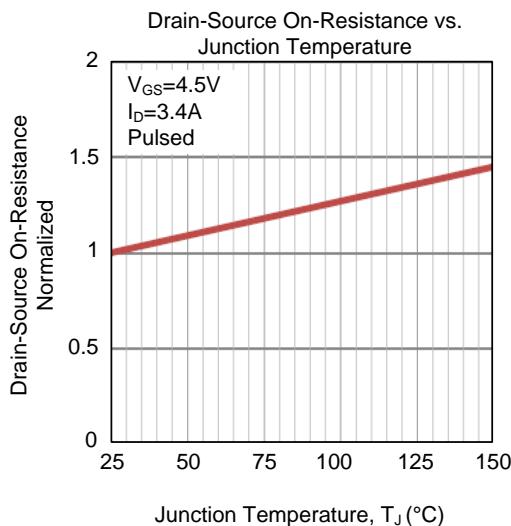
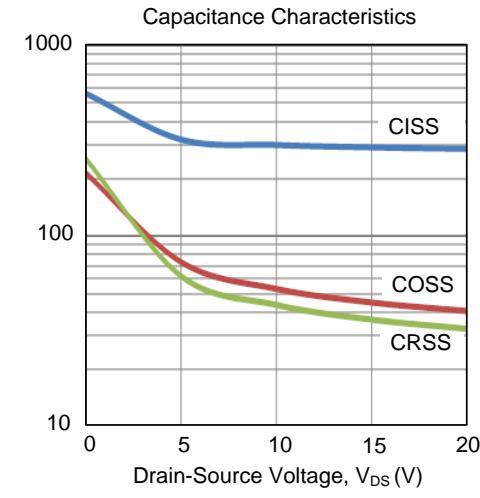
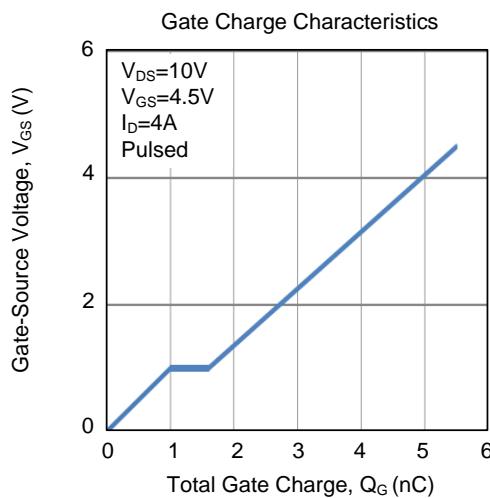
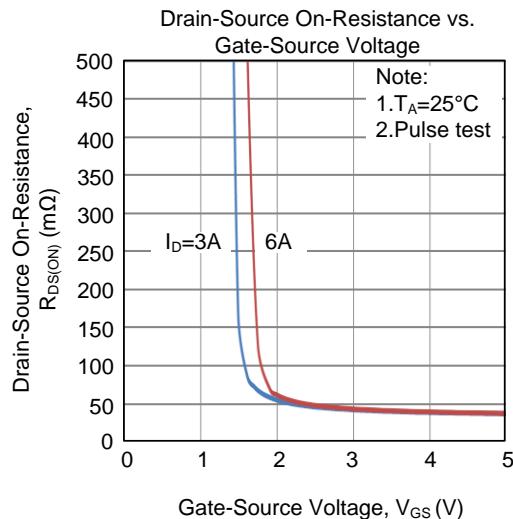
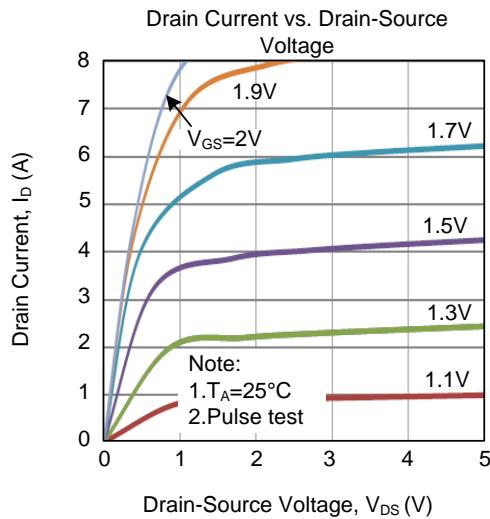
Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

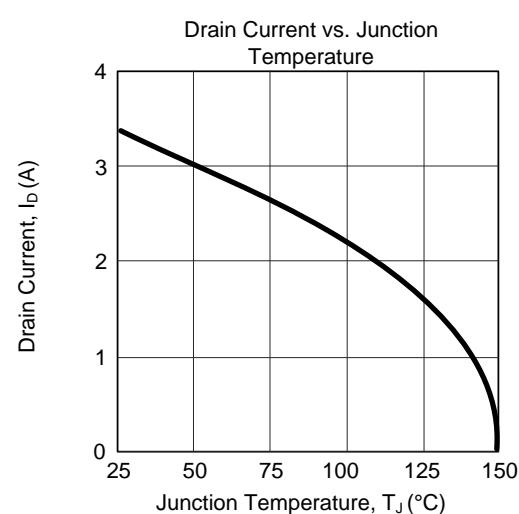
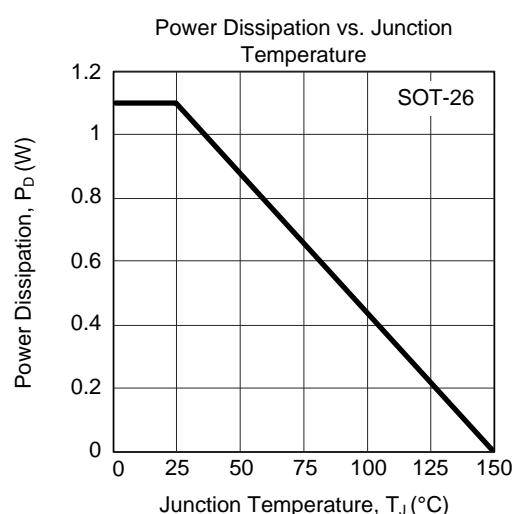
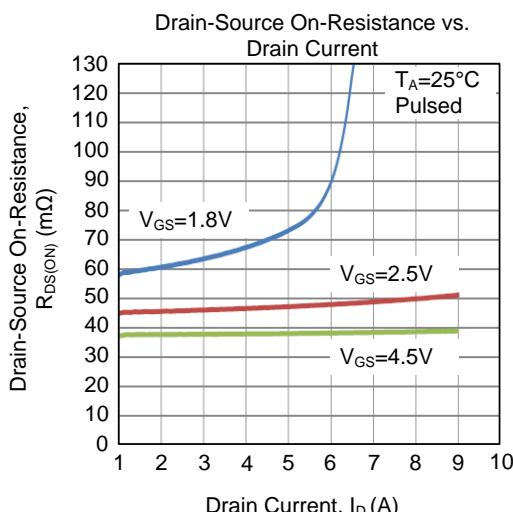
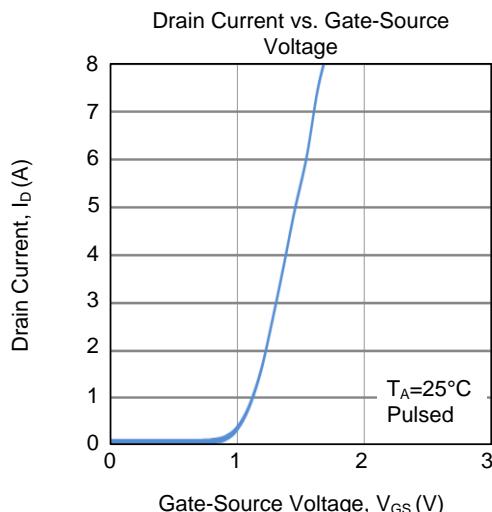
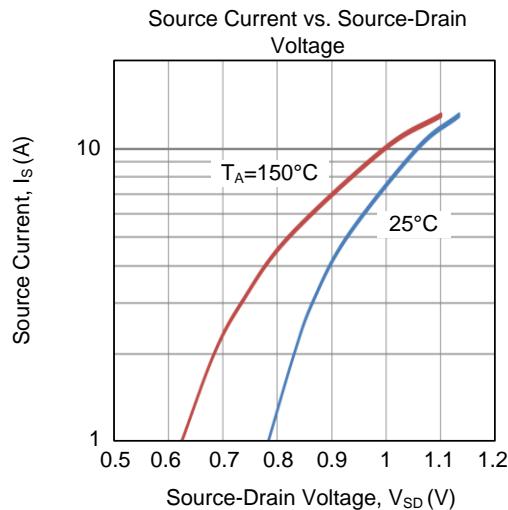
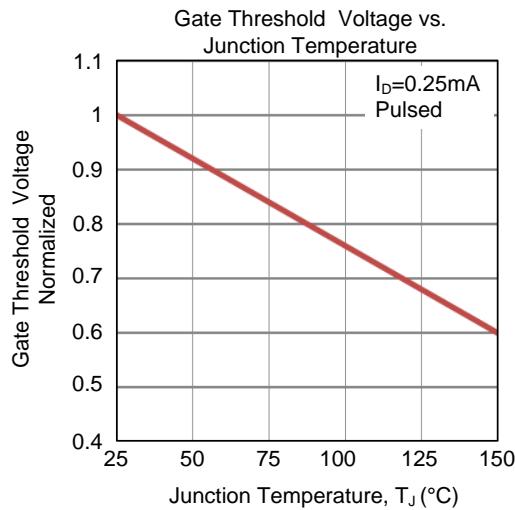
■ TYPICAL CHARACTERISTICS

N-CHANNEL



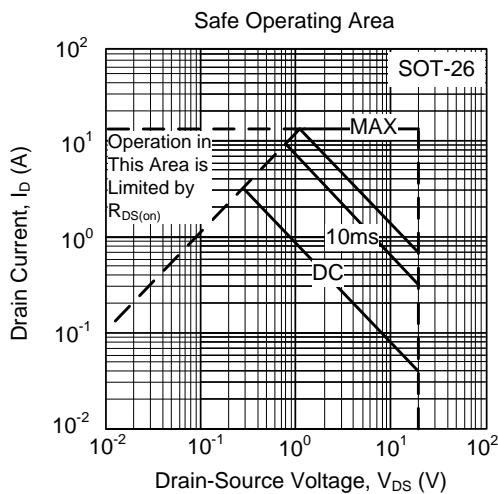
■ TYPICAL CHARACTERISTICS (Cont.)

N-CHANNEL

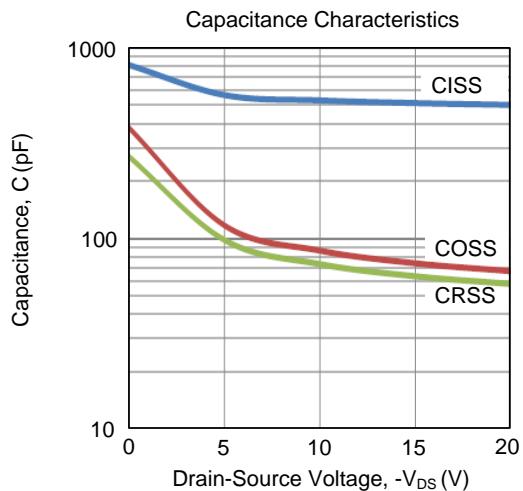
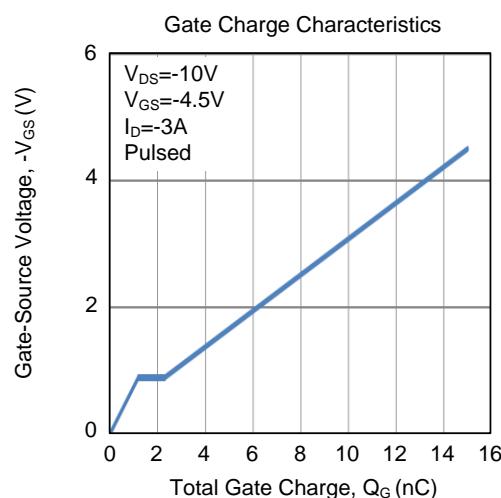
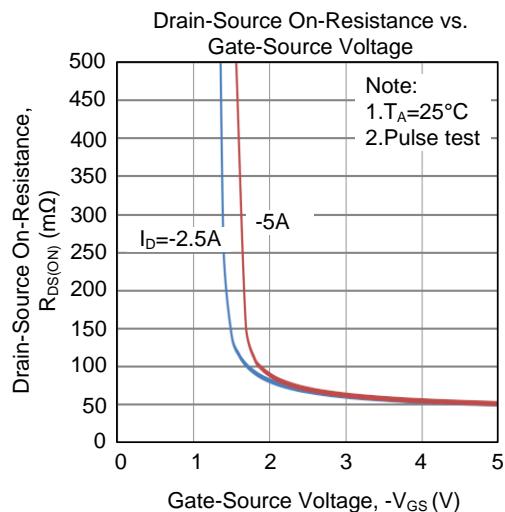
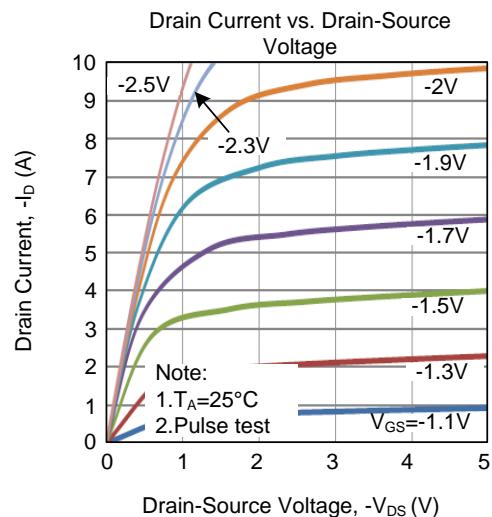


■ TYPICAL CHARACTERISTICS (Cont.)

N-CHANNEL

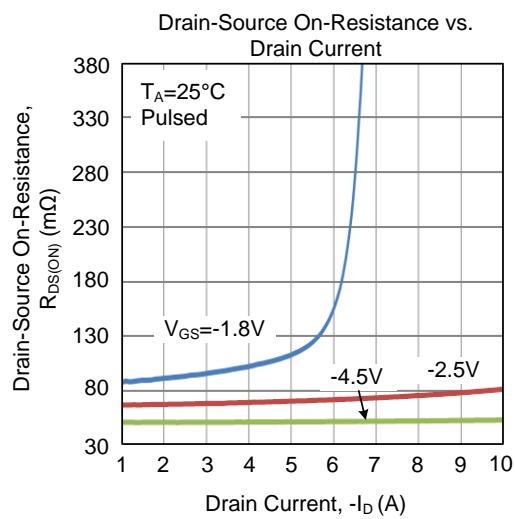
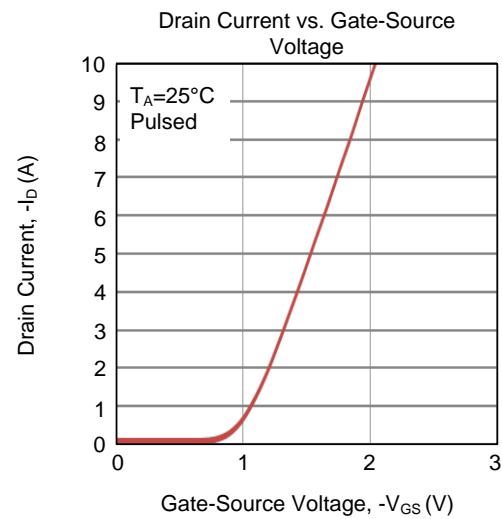
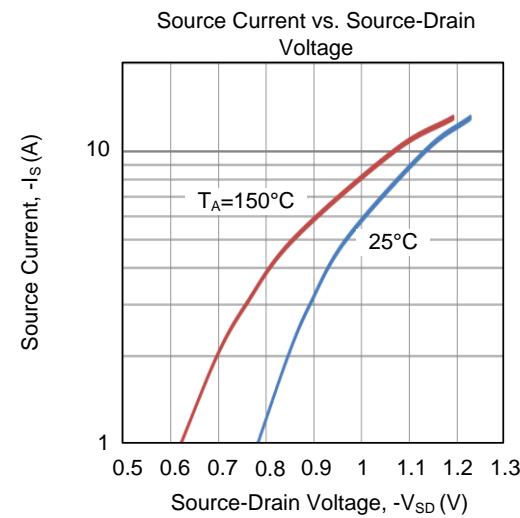
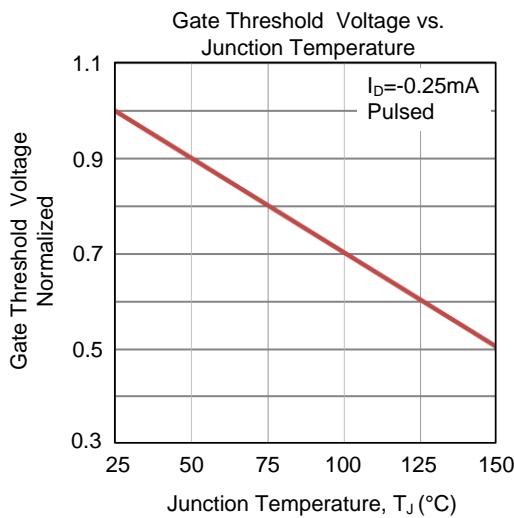
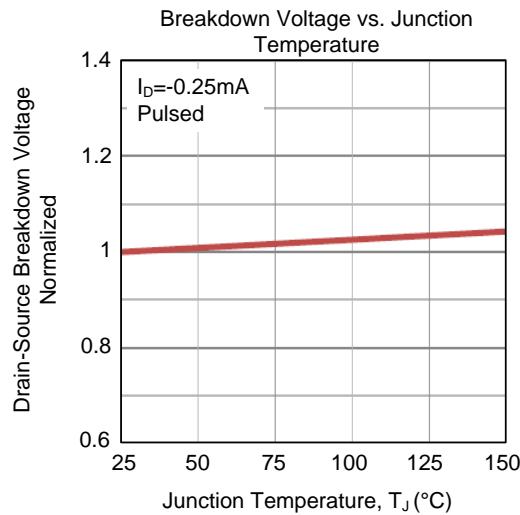
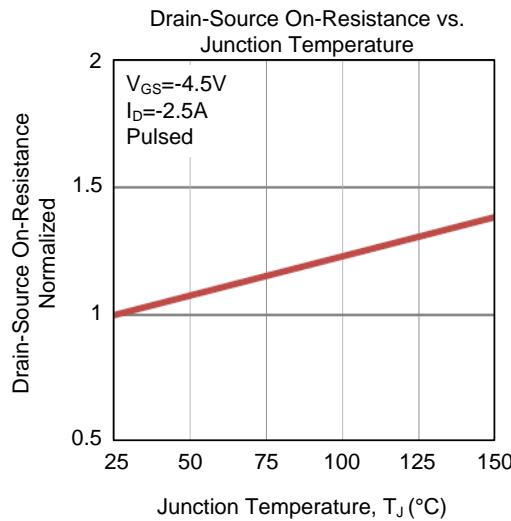


P-CHANNEL



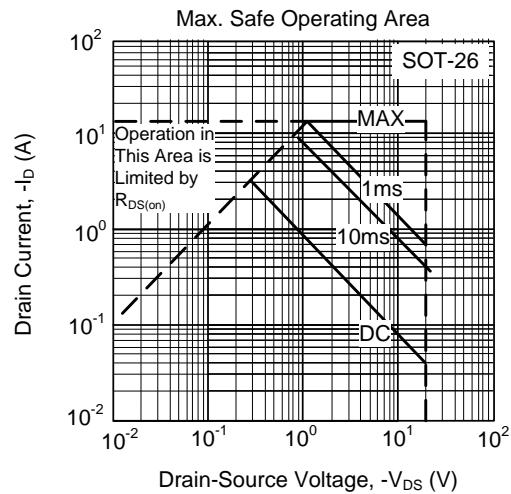
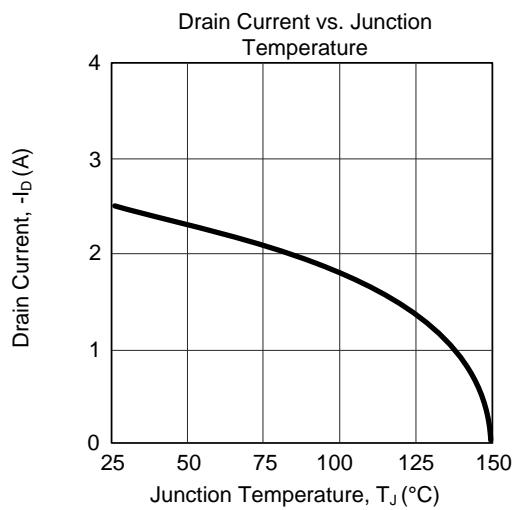
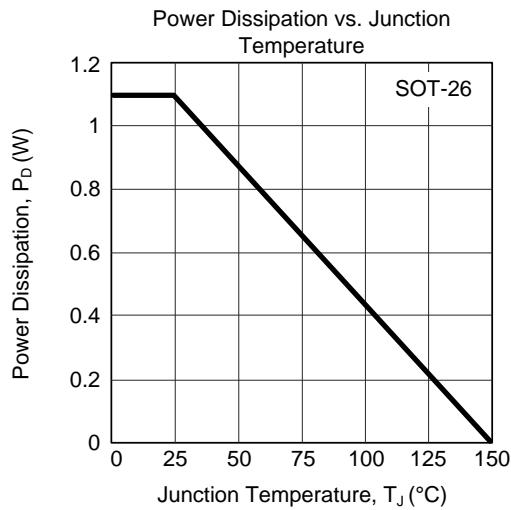
■ TYPICAL CHARACTERISTICS (Cont.)

P-CHANNEL



■ TYPICAL CHARACTERISTICS (Cont.)

P-CHANNEL



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