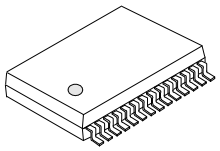
IC CARD INTERFACE



TSSOP-28

■ DESCRIPTION

The UTC **UTDA8024** is analog interface IC for 3V or 5V smart cards. It is placed between the card and the microcontroller to perform communication, control function, all supply and protection functions. It requires very few external components for application. It can be applied in many fields, such as IC card readers for banking, pay TV, Identification, Electronic payment, etc.

■ FEATURES

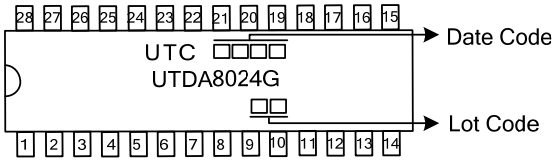
* Three specifically protected half-duplex bidirectional buffered I/O lines to card contacts C4, C7 and C8
* Automatic activation and deactivation sequences; initiated by software or by hardware in the event of a short-circuit, card take-off, overheating, V_{DD} or V_{DDP} drop-out
* 26MHz integrated crystal oscillator
* DC/DC converter for V_{CC} generation separately powered from a 5 V ± 20% supply (V_{DDP} and PGND)
* 3V or 5V ± 5% regulated card supply voltage (V_{CC}) with appropriate decoupling has the following capabilities:
  - I_{CC}<80mA at V_{DDP}=4~6.5V
  - Handles current spikes of 40nAs up to 20MHz
  - Controls rise and fall times
  - Filtered overload detection at approximately 120mA
* Built-in debounce on card presence contacts
* Supply supervisor for spike-killing during power-on and power-off and Power-on reset (threshold fixed internally or externally by a resistor bridge)
* Thermal and short-circuit protection on all card contacts
* Clock generation for cards up to 20MHz (divided by 1, 2, 4 or 8 through CLKDIV1 and CLKDIV2 signals) with synchronous frequency changes
* Non-inverted control of RST via pin RSTIN
* ISO 7816, GSM11.11 and EMV (payment systems) Compatibility
* Enhanced ESD protection on card side (>6kV)
* One multiplexed status signal $\overline{OFF}$

■ ORDERING INFORMATION

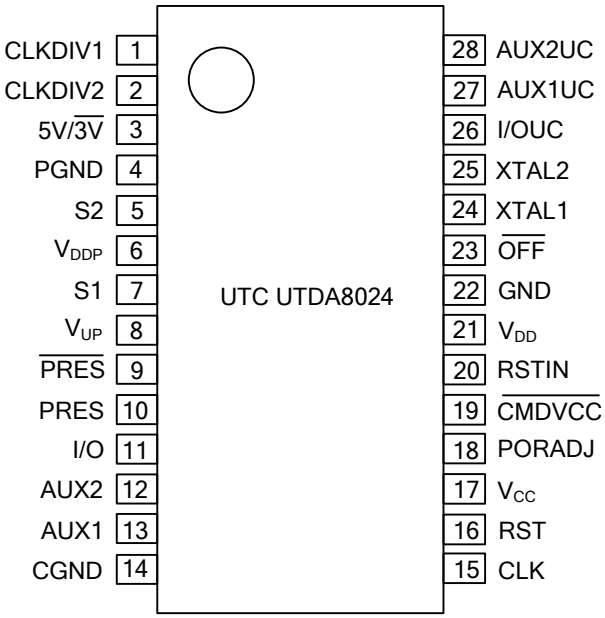
Ordering Number	Package	Packing
UTDA8024G-P28-R	TSSOP-28	Tape Reel

UTDA8024G-P28-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) P28: TSSOP-28 (3) G: Halogen Free and Lead Free

■ MARKING



■ PIN CONFIGURATION

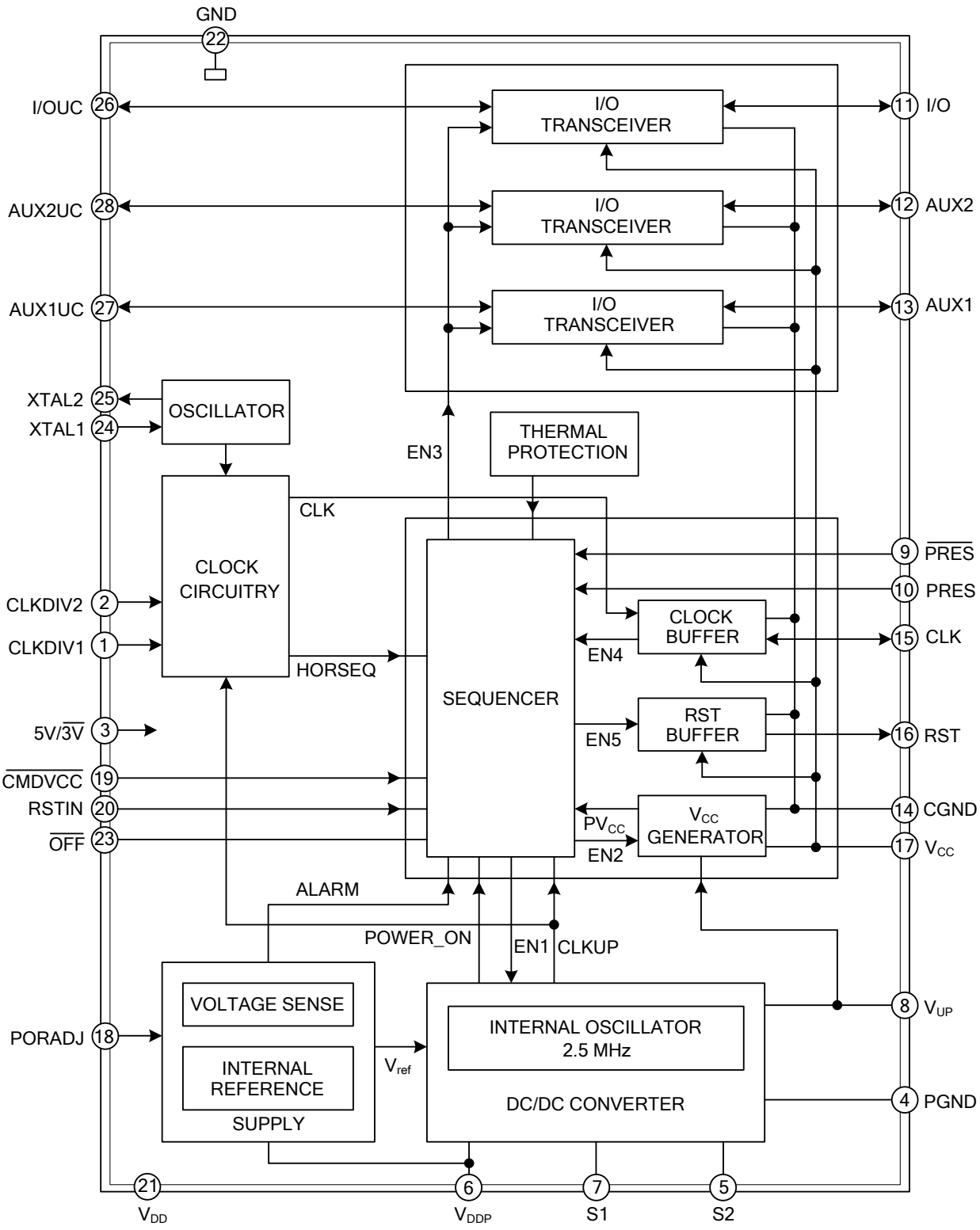


■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	CLKDIV1	CLK frequency selection input 1
2	CLKDIV2	CLK frequency selection input 2
3	5V/ $\overline{3V}$	Card supply voltage selection input; V_{CC}=5V (HIGH) or V_{CC}=3V (LOW)
4	PGND	DC/DC converter power supply ground
5	S2	DC/DC converter capacitor; connected between pins S1 and S2; C=100nF with ESR<100mΩ
6	V_{DDP}	DC/DC converter power supply voltage
7	S1	DC/DC converter capacitor; connected between pins S1 and S2; C=100nF with ESR<100mΩ
8	V_{UP}	DC/DC converter output decoupling capacitor connection; C=100nF with ESR<100mW must be connected between VUP and PGND
9	$\overline{PRES}$	Card presence contact input (active LOW); if PRES or $\overline{PRES}$ is active, the card is considered 'present' and a built-in debounce feature of 8 ms (typ.) is activated
10	PRES	Card presence contact input (active HIGH); if PRES or $\overline{PRES}$ is active, the card is considered 'present' and a built-in debounce feature of 8 ms (typ.) is activated
11	I/O	Data line to/from card reader contact C7; integrated 11kΩ pull-up resistor to V_{CC}
12	AUX2	Data line to/from card reader contact C8; integrated 11kΩ pull-up resistor to V_{CC}
13	AUX1	Data line to/from card reader contact C4; integrated 11kΩ pull-up resistor to V_{CC}
14	CGND	Card signal ground
15	CLK	Card clock to/from card reader contact C3
16	RST	Card reset output from card reader contact C2
17	V_{CC}	Card supply voltage to card reader contact C1; decoupled to CGND via 2 × 100nF or 100+220nF capacitors with ESR<100mΩ; Note 1
18	PORADJ	Power-on reset threshold adjustment input for changing the reset threshold with an external resistor bridge; doubles the width of the POR pulse when used
19	$\overline{CMDVCC}$	Input from the host to start activation sequence (active LOW)
20	RSTIN	Card reset input from the host
21	V_{DD}	Supply voltage
22	GND	Ground
23	$\overline{OFF}$	NMOS interrupt output to the host (active LOW); 20kΩ integrated pull-up resistor to V_{DD}
24	XTAL1	Crystal connection or input for external clock
25	XTAL2	Crystal connection (leave open-circuit if external clock source is used)
26	I/OUC	Host data I/O line; integrated 11kΩ pull-up resistor to V_{DD}
27	AUX1UC	Auxiliary data line to/from the host; integrated 11kΩ pull-up resistor to V_{DD}
28	AUX2UC	Auxiliary data line to/from the host; integrated 11 kΩ pull-up resistor to V_{DD}

Note 1. The noise margin on V_{CC} will be higher with the 220nF capacitor

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER			SYMBOL	RATINGS	UNIT
Supply Voltage			V_{DD}	-0.3~+6.5	V
DC/DC Converter Supply Voltage			V_{DDP}	-0.3~+6.5	V
Voltage On Input and Output Pins	Pins XTAL1, XTAL2, 5V/$\overline{3V}$, RSTIN, AUX1UC, AUX2UC, I/OUC, CLKDIV1, CLKDIV2, $\overline{CMDVCC}$, $\overline{OFF}$ and PORADJ		V_I, V_O	-0.3~+6.5	V
Voltage On Card Pins	Pins PRES, $\overline{PRES}$, I/O, RST, AUX1, AUX2 and CLK		V_{CARD}	-0.3~+6.5	V
Voltage On Other Pins	Pins V_{UP}, S1 and S2		V_N	-0.3~+6.5	V
Electrostatic Discharge Voltage	Card Contacts in Typical Application (Note 2) Pins I/O, RST, V_{CC}, AUX1, AUX2, CLK, PRES and $\overline{PRES}$		V_{ESD}	-6~+6	kV
	All Pins (Note 2)	Human Body Model		-2~+2	kV
		Machine Model		-200~+200	V
Maximum Junction Temperature			$T_{J(MAX)}$	150	°C
Storage Temperature			T_{STG}	-55~+150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. All card contacts are protected against any short-circuit with any other card contact.

■ THERMAL RESISTANCES CHARACTERISTICS

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	in Free Air	θ_{JA}	100	K/W

■ ELECTRICAL CHARACTERISTICS

V_{DD}=3.3V; V_{DDP}=5V; T_{AMB}=25°C; f_{XTAL}=10MHz; all currents flowing into the IC are positive; see Note 1; unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Temperature						
Ambient Temperature	T_{AMB}		-25		+85	°C
Supplies						
Supply Voltage	V_{DD}		2.7		6.5	V
DC/DC Converter Supply Voltage	V_{DDP}	V_{CC}=5V, $\|I_{CC}\|$ <50mA	4.0	5.0	6.5	V
		V_{CC}=5V, $\|I_{CC}\|$ <20mA	2.5		6.5	V
Supply Current	I_{DD}	Card Inactive			1.2	mA
		Card Active, $f_{CLK}=f_{XTAL}$, C_L=30pF			1.5	mA
DC/DC Converter Supply Current	I_{DDP}	Inactive Mode			0.1	mA
		active mode, $f_{CLK}=f_{XTAL}$, C_L=30Pf, $\|I_{CC}\|$ =0			10	mA
		V_{CC}=5V, $\|I_{CC}\|$ =80mA			200	mA
		V_{CC}=3V, $\|I_{CC}\|$ =65mA			100	mA
Falling Threshold Voltage on V_{DD}	V_{th2}	No External Resistors at Pin PORADJ, V_{DD} Level Falling	2.35	2.45	2.55	V
Hysteresis of Threshold Voltage V_{th2}	V_{hys2}	No External Resistors at Pin PORADJ	50	100	150	mV
Pin PORADJ (Note 2)						
External Rising Threshold Voltage on V_{DD}	$V_{th(ext)(rise)}$	External Resistor Bridge at Pin PORADJ, V_{DD} Level Rising	1.240	1.28	1.310	V
External Falling Threshold Voltage on V_{DD}	$V_{th(ext)(fall)}$	External Resistor Bridge at Pin POR ADJ, V_{DD} Level Falling	1.190	1.22	1.26	V
Hysteresis of Threshold Voltage $V_{th(ext)}$	$V_{hys(ext)}$	External Resistor Bridge at Pin POR ADJ	30	60	90	mV
Hysteresis of Threshold Voltage $V_{th(ext)}$ Variation with Temperature	$\Delta V_{hys(ext)}$	External Resistor Bridge at Pin PORADJ			0.25	mV/K
Width of Internal Power-On Reset Pulse	t_w	No External Resistors at Pin PORADJ	4	8	12	ms
		External Resistor Bridge at Pin PORADJ	8	16	24	ms
Leakage Current On Pin PORADJ	$I_{L(PORADJ)}$	V_{PORADJ}<0.5V	-0.1	4	10	μA
		V_{PORADJ}>1V	-1		+1	μA
Total Power Dissipation	P_{tot}	Continuous Operation, T_{AMB}=-25~+85°C			0.56	W
DC/DC converter						
Clock Frequency	f_{CLK}	Card Active	2.2		3.2	MHz
Threshold Voltage for Voltage Doubler to Change to Voltage Follower	$V_{th(vd-vf)}$	5V Card	5.2	5.8	6.2	V
		3V Card	3.8	4.1	4.4	V
Output Voltage On Pin V_{UP} (Average Value)	$V_{UP(av)}$	V_{CC}=5V	5.2	5.7	6.2	V
		V_{CC}=3V, V_{DDP}=3.3V	3.5	3.9	4.3	V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Card supply voltage (pin V_{CC}) (Note 3)							
External Capacitance On Pin V_{CC}	C_{VCC}	Note 4		80		400	nF
Card Supply Voltage (Including Ripple Voltage)	V_{CC}	5V Card	Card Inactive, $\|I_{CC}\|$ =0mA	-0.1	0	+0.1	V
			Card Inactive, $\|I_{CC}\|$ =1mA	-0.1	0	+0.3	V
			Card Active, $\|I_{CC}\|$ <50mA	4.75	5.0	5.25	V
			Card Active, Single Current Pulse, I_p=-100mA, t_p=2ms	4.65	5.0	5.25	V
			Card Active, Current Pulses, I_p=40nA	4.65	5.0	5.25	V
			Card Active, Current Pulses, I_p=40nA with $\|I_{CC}\|$ <200mA, t_p<400ns	4.65	5.0	5.25	V
		3V Card	Card Inactive, $\|I_{CC}\|$ =0mA	-0.1	0	+0.1	V
			Card Inactive, $\|I_{CC}\|$ =1mA	-0.1	0	+0.3	V
			Card Active, $\|I_{CC}\|$ <50mA	2.85	3.0	3.15	V
			Card Active, Single Current Pulse, I_p=-100mA, t_p=2ms	2.76	3.0	3.20	V
			Card Active, Current Pulses, I_p=40nA	2.76	3.0	3.20	V
			Card Active, Current Pulses, I_p=40nA with $\|I_{CC}\|$ <200mA, t_p<400ns	2.76	3.0	3.20	V
Ripple Voltage on V_{CC} (Peak to Peak Value)	$V_{CC(ripple)(p-p)}$	f_{ripple}=20kHz~200MHz				350	mV
Card Supply Current	$\|I_{CC}\|$	V_{CC}=0~5V				80	mA
		V_{CC}=0~3V				65	mA
		V_{CC} Short-Circuit to GND		100	120	150	mA
Slew Rate	SR	Slew Up or Down		0.08	0.15	0.22	V/μs
Crystal oscillator (pins XTAL1 and XTAL2)							
External Capacitance On Pins XTAL1 and XTAL2	C_{XTAL1}, C_{XTAL2}	Depends On Type of Crystal or Resonator Used				15	pF
Crystal Frequency	f_{XTAL}			2		26	MHz
Frequency Applied on Pin XTAL1	f_{XTAL1}			0		26	MHz
LOW-Level Input Voltage On Pin XTAL1	V_{IL}			-0.3		+0.3V_{DD}	V
HIGH-Level Input Voltage On Pin XTAL1	V_{IH}			0.7V_{DD}		V_{DD}+0.3	V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Data lines (pins I/O, I/OUC, AUX1, AUX2, AUX1UC and AUX2UC)							
I/O to I/OUC, I/OUC to I/O Falling Edge Delay	$t_{d(I/O-I/OUC)}$, $t_{d(I/OUC-I/O)}$					200	ns
Active Pull-Up Pulse Width	t_{pu}					100	ns
Maximum Frequency On Data Lines	$f_{I/O(max)}$					1	MHz
Input Capacitance On Data Lines	C_i					10	pF
Data lines to card reader (pins I/O, AUX1 and AUX2; with integrated 11kΩ pull-up resistors to V_{CC})							
Output Voltage	$V_{o(inactive)}$	Inactive Mode	No Load	0		0.1	V
			$I_{o(inactive)}$=1mA			0.3	V
Output Current	$I_{o(inactive)}$	Inactive Mode, Pin Grounded				-1	mA
LOW-Level Output Voltage	V_{OL}	I_{OL}=1mA		0		0.3	V
		I_{OL}≥15mA		V_{CC}-0.4		V_{CC}	V
HIGH-Level Output Voltage	V_{OH}	No DC Load		$0.9V_{CC}$		V_{CC}+0.1	V
		5 and 3V Cards, I_{OH}<-40μA		$0.75V_{CC}$		V_{CC}+0.1	V
		$\lvert I_{OH} \rvert$ ≥10mA		0		0.4	V
LOW-Level Input Voltage	V_{IL}			0.3		0.8	V
HIGH-Level Input Voltage	V_{IH}			1.5		V_{CC}+0.3	V
LOW-Level Input Current	$\lvert I_{IL} \rvert$	V_{IL}=0V				600	μA
HIGH-Level Input Leakage Current	$\lvert I_{LIH} \rvert$	V_{IH}=V_{CC}				10	μA
Data Input Transition Time	$t_{t(DI)}$	$V_{IL(max)}$ to $V_{IH(min)}$				1.2	μs
Data Output Transition Time	$t_{t(DO)}$	V_o=0~V_{CC}, C_L≤80pF, 10% to 90%				0.1	μs
Integrated Pull-Up Resistor	R_{pu}	Pull-Up Resistor to V_{CC}			18		kΩ
Current When Pull-Up Active	I_{pu}	V_{OH}=0.9V_{CC}, C=80pF		-1			mA
Data lines to microcontroller (pins I/OUC, AUX1UC and AUX2UC; with integrated 11kΩ pull-up resistors to V_{DD})							
LOW-Level Output Voltage	V_{OL}	I_{OL}=1mA		0		0.3	V
HIGH-Level Output Voltage	V_{OH}	No DC Load		$0.9V_{DD}$		V_{DD}+0.1	V
		5 and 3V Cards, I_{OH}<-40μA		$0.75V_{DD}$		V_{DD}+0.1	V
LOW-Level Input Voltage	V_{IL}			-0.3		+0.3V_{DD}	V
HIGH-Level Input Voltage	V_{IH}			$0.7V_{DD}$		V_{DD}+0.3	V
HIGH-Level Input Leakage Current	$\lvert I_{LIH} \rvert$	V_{IH}=V_{DD}				10	μA
LOW-Level Input Current	$\lvert I_L \rvert$	V_{IL}=0V				600	μA
Integrated Pull-Up Resistor	R_{pu}	Pull-Up Resistor to V_{CC}			18		kΩ
Data Input Transition Time	$t_{t(DI)}$	$V_{IL(max)}$ to $V_{IH(min)}$				1.2	μs
Data Output Transition Time	$t_{t(DO)}$	V_o=0~V_{DD}, C_L<30pF, 10% to 90%				0.1	μs
Current When Pull-Up Active	I_{pu}	V_{OH}=0.9V_{DD}, C=30pF		-1			mA
Internal oscillator							
Frequency of Internal Oscillator	$f_{OSC(int)}$	Inactive Mode		55	140	200	kHz
		Active Mode		2.2	2.7	3.2	MHz
Reset output to card reader (pin RST)							
Output Voltage	$V_{o(inactive)}$	Inactive Mode	No Load	0		0.1	V
			$I_{o(inactive)}$=1mA	0		0.3	V
Output Current	$I_{o(inactive)}$	Inactive Mode, Pin Grounded		0		-1	mA
RSTIN to RST Delay	$t_{d(RSTIN-RST)}$	RST Enabled				2	μs

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
LOW-Level Output Voltage	V_{OL}	I_{OL}=200μA		0		0.2	V
		I_{OL}=20mA (Current Limit)		V_{CC}-0.4		V_{CC}	V
HIGH-Level Output Voltage	V_{OH}	I_{OH}=-200μA		0.9V_{CC}		V_{CC}	V
		I_{OH}=-20mA (Current Limit)		0		0.4	V
Rise Time	t_r	C_L=100pF, V_{CC}=5 or 3V				0.1	μs
Fall Time	t_f	C_L=100pF, V_{CC}=5 or 3V				0.1	μs
Clock output to card reader (pin CLK)							
Output Voltage	$V_{o(inactive)}$	Inactive Mode	No Load	0		0.1	V
			$I_{o(inactive)}$=1mA	0		0.3	V
Output Current	$I_{o(inactive)}$	CLK Inactive, Pin Grounded		0		-1	mA
LOW-Level Output Voltage	V_{OL}	I_{OL}=200μA		0		0.3	V
		I_{OL}=70mA (Current Limit)		V_{CC}-0.4		V_{CC}	V
HIGH-Level Output Voltage	V_{OH}	I_{OH}=-200μA		0.9V_{CC}		V_{CC}	V
		I_{OLH}=-70mA (Current Limit)		0		0.4	V
Rise Time	t_r	C_L=30pF, Note 5				16	ns
Fall Time	t_f	C_L=30pF, Note 5				16	ns
Duty Factor (Except for f_{XTAL})	δ	C_L=30pF, Note 5		45		55	%
Slew Rate	SR	Slew Up or Down, C_L=30pF		0.2			V/ns
Control inputs (pins CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$, RSTIN and 5V/$\overline{\text{3V}}$) (Note 6)							
LOW-Level Input Voltage	V_{IL}			-0.3		+0.3V_{DD}	V
HIGH-Level Input Voltage	V_{IH}			0.7V_{DD}		V_{DD}+0.3	V
LOW-Level Input Leakage Current	$\lvert I_{LIL} \rvert$	0<V_{IL}<V_{DD}				1	μA
HIGH-Level Input Leakage Current	$\lvert I_{LIH} \rvert$	0<V_{IH}<V_{DD}				1	μA
Card presence inputs (pins PRES and $\overline{\text{PRES}}$) (Note 7)							
LOW-Level Input Voltage	V_{IL}			-0.3		+0.3V_{DD}	V
HIGH-Level Input Voltage	V_{IH}			0.7V_{DD}		V_{DD}+0.3	V
LOW-Level Input Leakage Current	$\lvert I_{LIL} \rvert$	0<V_{IL}<V_{DD}				5	μA
HIGH-Level Input Leakage Current	$\lvert I_{LIH} \rvert$	0<V_{IH}<V_{DD}				5	μA
Interrupt output (pin $\overline{\text{OFF}}$; NMOS drain with integrated 20kΩ pull-up resistor to V_{DD})							
LOW-Level Output Voltage	V_{OL}	I_{OL}=2mA		0		0.3	V
HIGH-Level Output Voltage	V_{OH}	I_{OH}=-15μA		0.75V_{DD}			V
Integrated Pull-Up Resistor	R_{pu}	20kΩ Pull-Up Resistor to V_{DD}		16	20	24	kΩ
Protection and limitation							
Shutdown and Limitation Current pin V_{CC}	$\lvert I_{CC(sd)} \rvert$				130	150	mA
Limitation Current Pins I/O, AUX1 and AUX2	$I_{I/O(lim)}$			-15		+15	mA
Limitation Current Pin CLK	$I_{CLK(lim)}$			-70		+70	mA
Limitation Current Pin RST	$I_{RST(lim)}$			-20		+20	mA
Shut-Down Temperature	T_{sd}				150		°C
Timing							
Activation Time	t_{act}	see Fig.1		50		220	μs
Deactivation Time	t_{de}	see Fig.3		50	80	100	μs
Start of the Window for Sending CLK to the Card	t_3	see Fig.1&2		50		130	μs
End of the Window for Sending CLK to the Card	t_5	see Fig.1&2		140		220	μs
Debounce Time Pins PRES And $\overline{\text{PRES}}$	$t_{debounce}$	see Fig.4		5	8	11	ms

■ ELECTRICAL CHARACTERISTICS (Cont.)

Notes: 1. All parameters remain within limits but are tested only statistically for the temperature range. When a parameter is specified as a function of V_{DD} or V_{CC} it means their actual value at the moment of measurement.

2. If no external bridge is used then, to avoid any disturbance, it is recommended to connect pin 18 to ground.
3. To meet these specifications, pin V_{CC} should be decoupled to CGND using two ceramic multilayer capacitors of low ESR both with values of 100nF, or one 100nF and one 220nF (see Fig. 6)
4. Permitted capacitor values are 100, or 100 + 100, or 220, or 220 + 100, or 330nF.
5. Transition time and duty factor definitions are shown in Fig.5, $\delta = \frac{t_1}{t_1 + t_2}$
6. Pin $\overline{\text{CMDVCC}}$ is active LOW; pin RSTIN is active HIGH; for CLKDIV1 and CLKDIV2 functions see Table 1.
7. Pin $\overline{\text{PRES}}$ is active LOW; pin PRES is active HIGH; PRES has an integrated 1.25μA current source to GND (PRES to V_{DD}); the card is considered present if at least one of the inputs $\overline{\text{PRES}}$ or PRES is active.

Table 1 Clock frequency selection (Note)

CLKDIV1	CLKDIV2	f_{CLK}
0	0	$\frac{f_{XTAL}}{8}$
0	1	$\frac{f_{XTAL}}{4}$
1	1	$\frac{f_{XTAL}}{2}$
1	0	f_{XTAL}

Note: The status of pins CLKDIV1 and CLKDIV2must not be changed simultaneously; a delay of 10ns minimum between changes is needed; the minimum duration of any state of CLK is eight periods of XTAL1.

■ TIMING WAVEFORMS

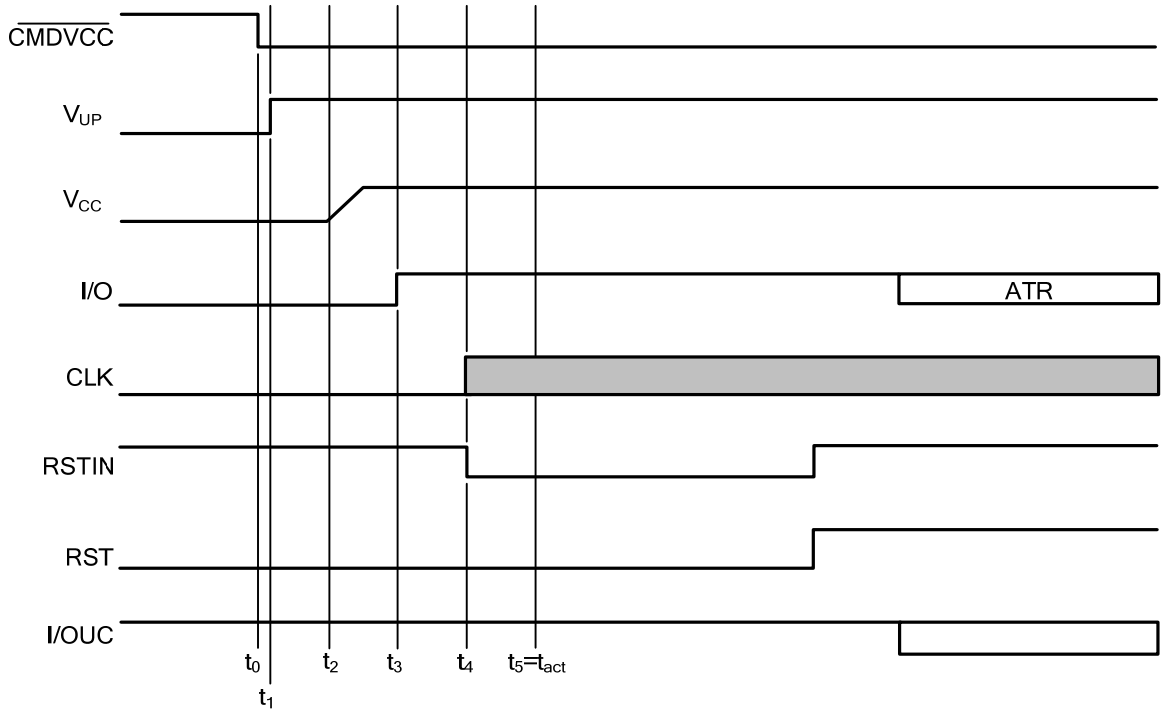


Fig. 1 Activation Sequence Using RSTIN and $\overline{\text{CMDVCC}}$.

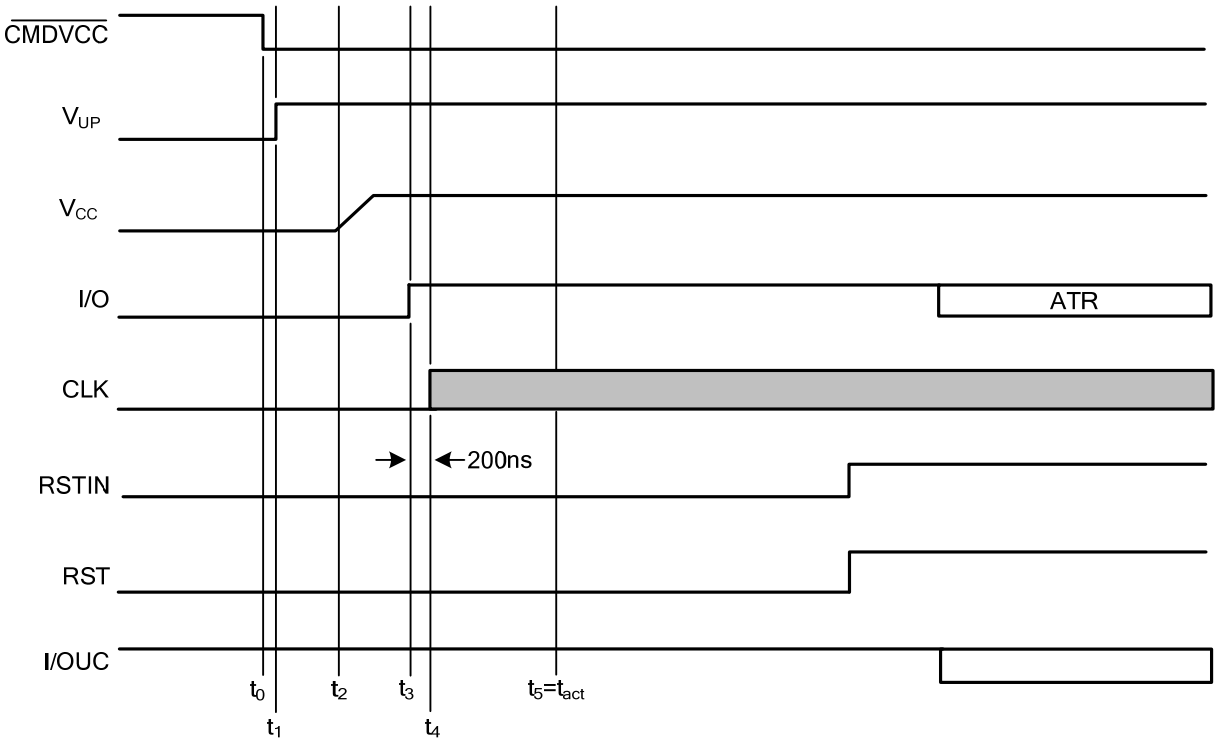


Fig. 2 Activation sequence at t_3.

■ TIMING WAVEFORMS (Cont.)

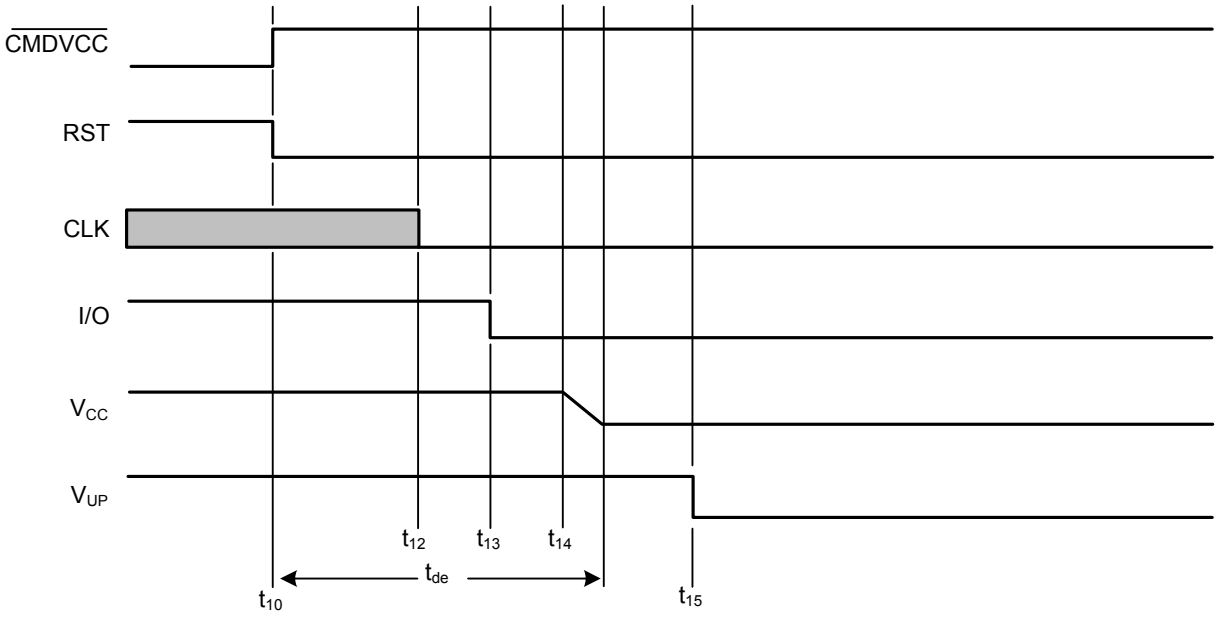


Fig.3 Deactivation Sequence

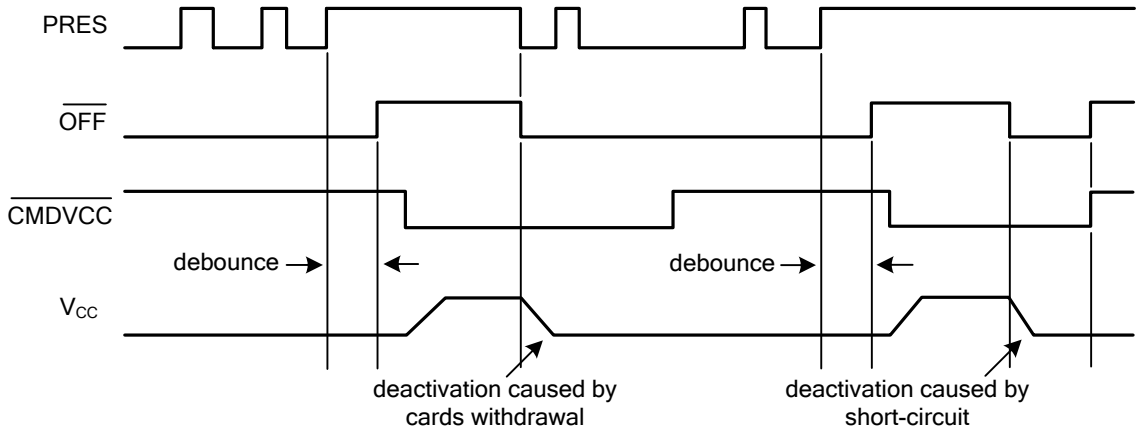


Fig. 4 Behaviour of $\overline{OFF}$, $\overline{CMDVCC}$, PRES and V_{CC}.

■ TIMING WAVEFORMS (Cont.)

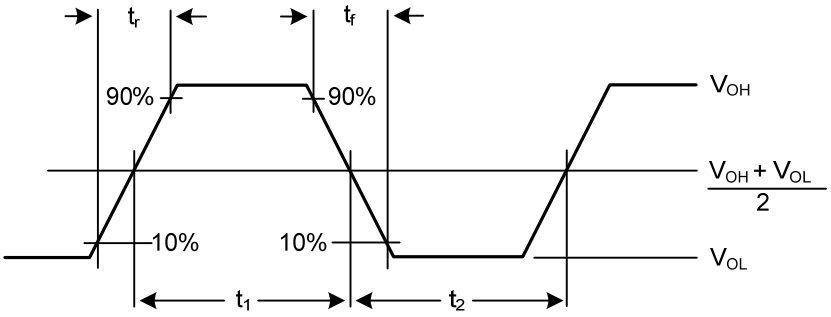


Fig. 5 Definition of output and input transition times.

■ TYPICAL APPLICATION CIRCUIT

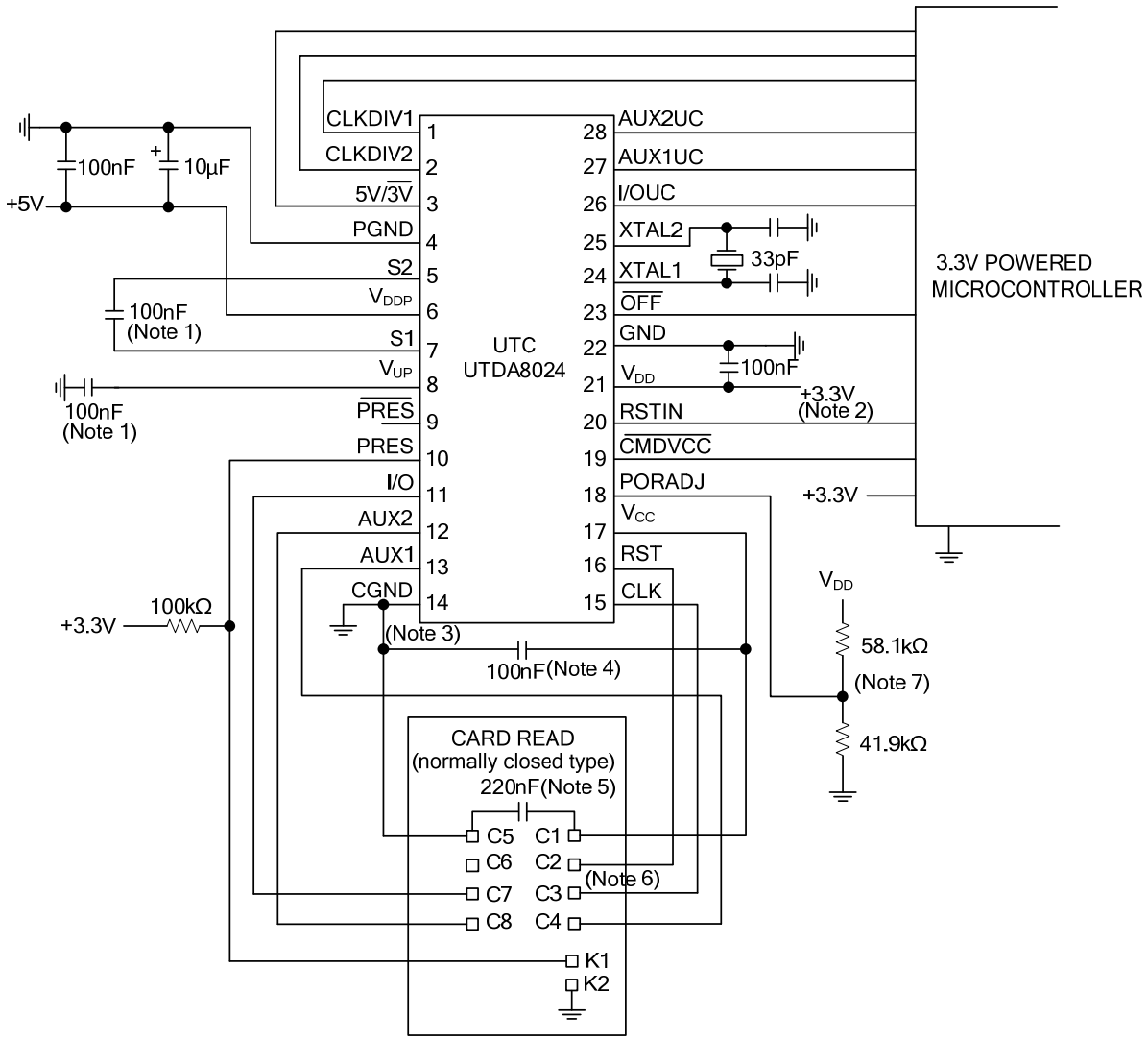


Fig. 6 Application Diagram.

Notes: 1. These capacitors must be of the low ESR-type and be placed near the IC (within 100mm).
2. UTC UTDA8024 and the microcontroller must use the same V_{DD} supply.
3. Make short, straight connections between CGND, C5 and the ground connection to the capacitor.
4. Mount one low ESR-type 100nF capacitor close to pin V_{CC}.
5. Mount one low ESR-type 100 or 220nF capacitor close to C1 contact (less than 100mm from it).
6. The connection to C3 should be routed as far from C2, C7, C4 and C8 and, if possible, surrounded by grounded tracks.
7. Optional resistor bridge for changing the threshold of V_{DD}. If this bridge is not required pin 18 should be connected to ground.