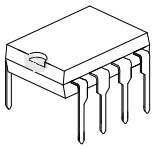
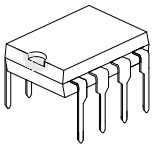
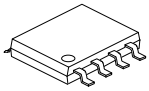
HIGH PERFORMANCE CURRENT MODE POWER SWITCH



DIP-7A



DIP-8



SOP-8

■ DESCRIPTION

The UTC **UCS1652S** is an integrated PWM controller and Power MOSFET specifically designed for switching operation with minimal external components. The UTC **UCS1652S** is designed to provide several special enhancements to satisfy the needs, for example, Power-Saving mode for low standby power, Frequency Hopping , Constant Output Power Limiting , Slope Compensation ,Over Current Protection (OCP), Over Voltage Protection (OVP), Over Load Protection (OLP), Under Voltage Lock Out (UVLO), Over Temperature Protection (OTP), etc. IC will be shutdown or can auto-restart in situations.

■ FEATURE

* Internal Power MOSFET (650V)
* Programming Gate Driver Capability
* Frequency hopping for Improved EMI Performance.
* Lower than 30mW Standby Power Design
* Linearly decreasing frequency to 20~35KHz during light load
* Internal Soft start
* Internal Slope Compensation
* Constant Power Limiting for universal AC input Range
* Gate Output Maximum Voltage Clamp(16V)
* Over temperature protection
* Overload protection
* Over voltage protection
* Leading edge blanking
* Cycle-by-Cycle current limiting
* Under Voltage Lock Out

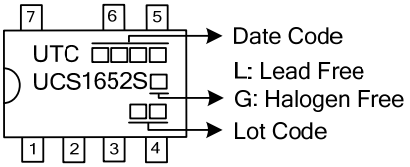
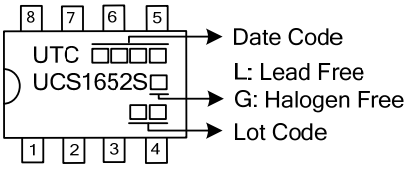
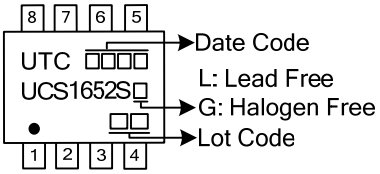
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCS1652SL-D07A-T	UCS1652SG-D07A-T	DIP-7A	Tube
UCS1652SL-D08-T	UCS1652SG-D08-T	DIP-8	Tube
UCS1652SL-S08-R	UCS1652SG-S08-R	SOP-8	Tape Reel

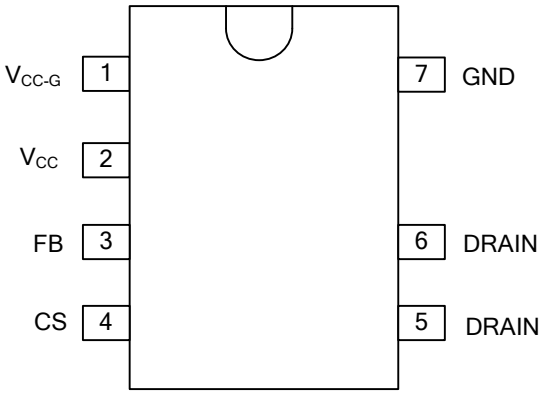
UCS1652SG-D07A-T
(1)Packing Type
(2)Package Type
(3)Green Package

(1) T: Tube, R: Tape Reel
(2) D07A: DIP-7A, D08: DIP-8, S08: SOP-8
(3) G: Halogen Free and Lead Free, L: Lead Free

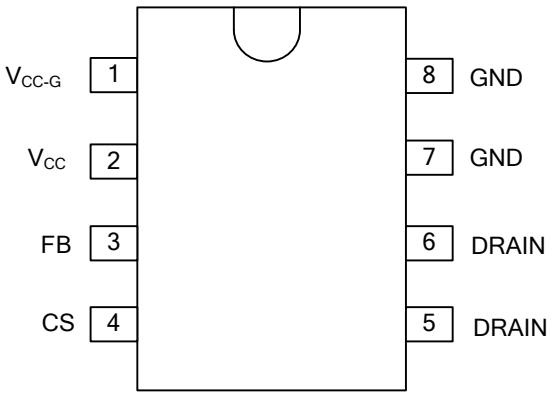
■ MARKING

PACKAGE	MARKING
DIP-7A	
DIP-8	
SOP-8	

■ PIN CONFIGURATION



DIP-7A

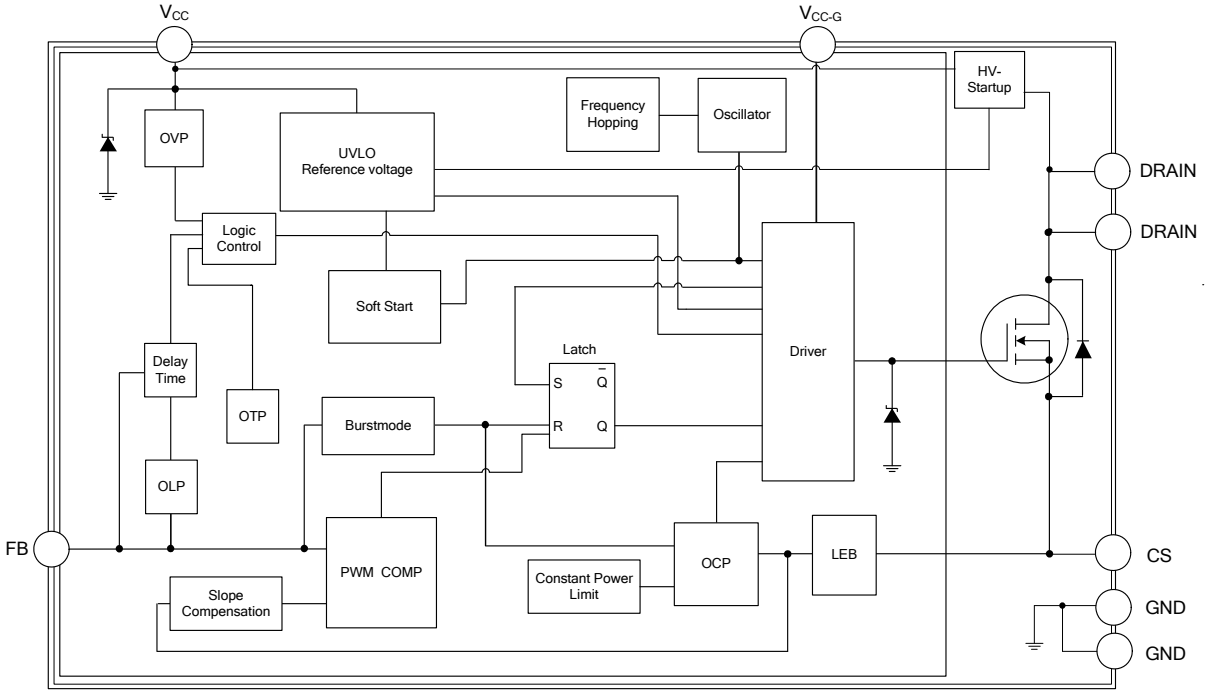


DIP-8 / SOP-8

■ PIN DESCRIPTION

PIN NO.		PIN NAME	DESCRIPTION
DIP-7A	DIP-8 / SOP-8		
1	1	V_{CC-G}	Supply voltage
2	2	V_{CC}	Supply voltage
3	3	FB	Feedback
4	4	CS	Current sense input
5	5	DRAIN	Power MOSFET drain
6	6	DRAIN	Power MOSFET drain
-	7	GND	Ground
7	8	GND	Ground

■ BLOCK DIAGRAM



Notes: OLP (Over Load Protection)
OVP (Over Voltage Protection)
OTP (Over Temperature Protection)
OCP (Over Current Protection)
UVLO (Under Voltage Latch-Out)
LEB (Led Edge Blanking)

■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	32	V
Input Voltage to FB Pin	V_{FB}	-0.3 ~ 6.5	V
Input Voltage to CS Pin	V_{CS}	-0.3 ~ 6.5	V
Junction Temperature	T_J	+150	°C
Operating Temperature	T_{OPR}	-40 ~ +125	°C
Storage Temperature	T_{STG}	-50 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ OPERATING RANGE

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	10 ~ 24	V
V_{CC-G} Pin Series Resistor	V_{CC_GR}	51 ~ 510	Ω
Open Frame Output Power for 85~264VAC	P_{O_MAX}	18	W

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, V_{CC}=15V, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY SECTION							
Start Up Current		I_{ST}	V_{CC} = $V_{THD(ON)}$-1V		2	15	μA
Supply Current with Switch		I_{OP}	V_{FB}= 3.5V		1.5	2.5	mA
V_{DD} Zener Clamp Voltage		V_{CLAMP}	I_{VDD}=20mA	29	30	32	V
UNDER-VOLTAGE LOCKOUT SECTION							
Start Threshold Voltage		$V_{THD(ON)}$		18	20	22	V
Min. Operating Voltage		$V_{CC(MIN)}$		6.5	8	9.5	V
CONTROL SECTION							
Feedback Source Current		I_{FB}	V_{FB}=0		240		uA
V_{FB} Open Loop Voltage Level		V_{FB_Open}			5.4		V
Burst-Mode Out FB Voltage		$V_{FB(OUT)}$	V_{CS} =0		1.42		V
Burst-Mode Enter FB Voltage		$V_{FB(IN)}$	V_{CS} =0		1.35		V
Switching Frequency	Normal Initial	$F_{(SW)}$	V_{FB} = 3.5V	60	65	70	kHz
	Burst mode Base Frequency			20			kHz
Duty Cycle		D_{MAX}	V_{FB}=3.5V, V_{CS}=0	70	80	90	%
Frequency Hopping		$F_{J(SW)}$		-9		+9	%
Frequency Variation VS V_{CC} Deviation		F_{DV}	V_{CC}=10 ~ 20V			10	%
Frequency Variation VS Temperature Deviation		F_{DT}	T=-40 ~ 110°C			10	%
Soft-Start Time		T_{SOFTS}			5		ms
PROTECTION SECTION							
OVP Threshold		V_{OVP}	V_{FB}=3.5V	25	26	27	V
OLP Threshold		$V_{FB(OLP)}$	V_{CS}=0		4.4		V
Delay Time Of OLP		T_{D-OLP}		60	88	120	ms
OTP Threshold		$T_{(THR)}$			140		°C
CURRENT LIMITING SECTION							
Leading Edge Blanking Time		t_{LEB}		200	450	700	nS
Peak Current Limitation		$V_{SENSE-H}$	V_{FB}=3.9V		0.92		V
Threshold Voltage For Valley		$V_{SENSE-L}$	V_{FB}=3.9V	0.73	0.79	0.85	V
POWER MOS-TRANSISTOR SECTION							
Drain-Source Breakdown Voltage		V_{DSS}	V_{GS}=0V, I_D=250μA	650			V
Drain-Source Diode Continuous Source Current		I_S				2.8	A
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=0.8A			2.5	Ω

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature.

■ FUNCTIONAL DESCRIPTION

The internal reference voltages and bias circuit work at V_{CC}> $V_{THD(ON)}$, and shutdown at V_{CC}<$V_{CC(MIN)}$.

(1) Soft-Start

When every IC power on, driver output duty cycle will be decided by inter-slope voltage V_{SOFTS} and V_{CS} on current sense resistor at beginning. After the whole soft-start phase end, and driver duty cycle depend on V_{FB} and V_{CS}. The relation among V_{SOFTS}, V_{FB} and V_{OUT} as followed Fig.3. Furthermore, soft-start phase should end before V_{CC} reach $V_{CC(MIN)}$ during V_{CC} power on. Otherwise, if soft-start phase remain not end before V_{CC} reach $V_{CC(MIN)}$ during V_{CC} power on, IC will enter auto-restart phase and not set up V_{OUT}.

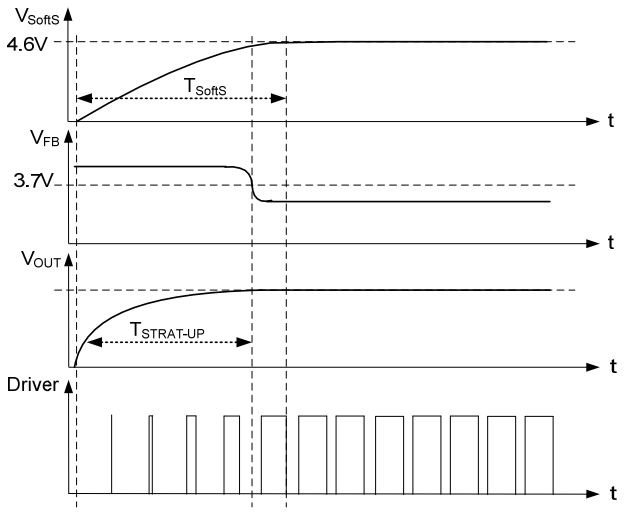


Fig.3 Soft-start phase

(2) Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation, this greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

(3) Frequency Hopping For EMI Improvement

The Frequency Hopping is implemented in the IC; there are two oscillators built-in the IC. The first oscillator is to set the normal switching frequency; the switching frequency is modulated with a period signal generated by the 2nd oscillator. The relation between the first oscillator and the 2nd oscillator as followed Fig.4. So the tone energy is evenly spread out, the spread spectrum minimizes the conduction band EMI and therefore eases the system design in meeting stringent EMI requirement.

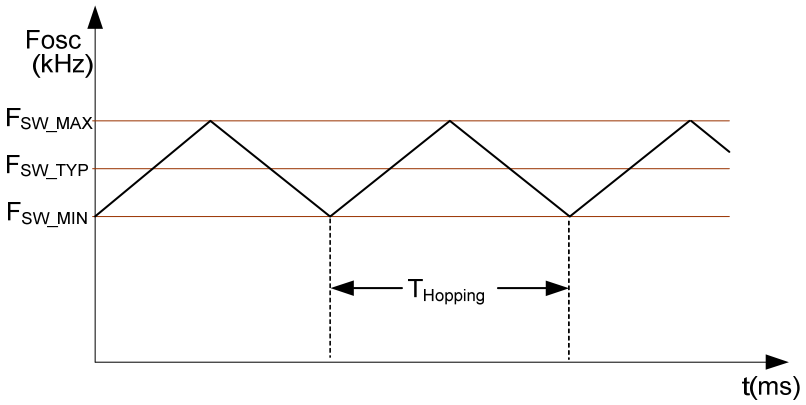


Fig.4 Frequency Hopping

■ FUNCTIONAL DESCRIPTION (Cont.)

(4) Constant Output Power Limit

When the primary current, across the primary wind of transformer, reaches the limit current, the output GATE driver will be turned off after a small propagation delay t_D. This propagation delay will introduce an additional current proportional to $t_D \times V_{IN}/Lp$. Since the propagation delay is nearly constant regardless of the input line voltage V_{IN}. Higher input line voltage will result in a larger additional current and hence the output power limit is also higher than that under low input line voltage. To compensate for this output power limit variation across a wide AC input range, the threshold voltage is adjusted by adding a positive ramp. This ramp signal rises from $V_{SENSE\text{-}L}$ to V_{SENSE_H}, and then flattens out at V_{SENSE_H}. A smaller threshold voltage forces the output GATE drive to terminate earlier. This reduces the total PWM turn-on time and makes the output power equal to that of low line input. This proprietary internal compensation ensures a constant output power limit for a wide AC input voltage range (90VAC to 264VAC).

(5) Protection section

The IC takes on more protection functions such as OLP, OVP and OTP etc. In case of those failure modes for continual blanking time, the driver is shut down. At the same time, IC enters auto-restart, V_{CC} power on and driver is reset after V_{CC} power on again.

OLP

After power on, IC will shutdown driver if over load state occurs for continual $T_{D\text{-}OLP}$. OLP case as followed Fig.5.

OVP

OVP will shutdown the sitching of the power MOSFET whenever $V_{CC} > V_{OVP}$. The OVP case as followed Fig.6.

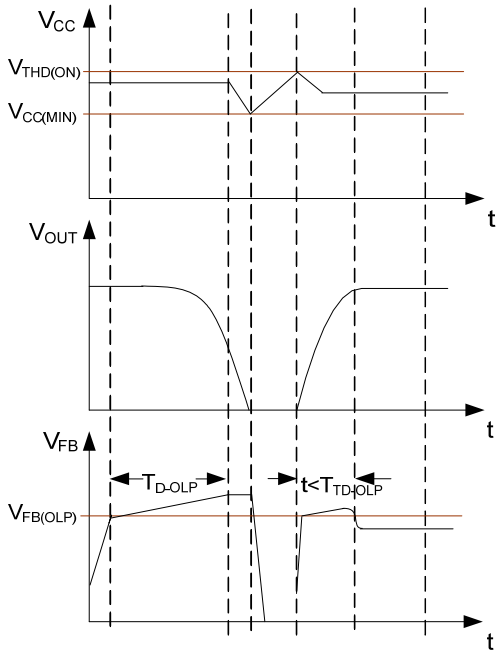


Fig.5 OLP case

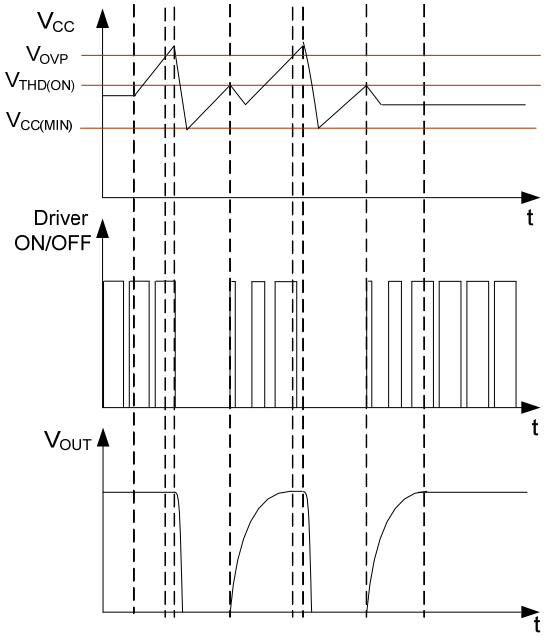


Fig.6 OVP case

OTP

OTP will shut down driver when junction temperature $T_J > T_{(THR)}$ for continual a blanking time.

■ FUNCTIONAL DESCRIPTION (Cont.)

(6) Driver Output Section

The driver-stage drives the gate of the MOSFET and is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch on slope when reaching the MOSFET threshold. This is achieved by a slope control of the rising edge at the driver's output. The output driver is clamped by an internal 16V Zener diode in order to protect power MOSFET transistors against undesirable gate over voltage.

In addition to the gate drive control scheme mentioned, the gate drive strength can also be adjusted externally by a resistor connected between V_{DD} and V_{DDG}, the falling edge of the Drain output can be well controlled. It provides great flexibility for system EMI design.

(7) Inside power switch MOS transistor

Specific power MOS transistor parameter is as "POWER MOS TRANSISTOR SECTION" in electrical characteristics table.

■ TYPICAL APPLICATION CIRCUIT

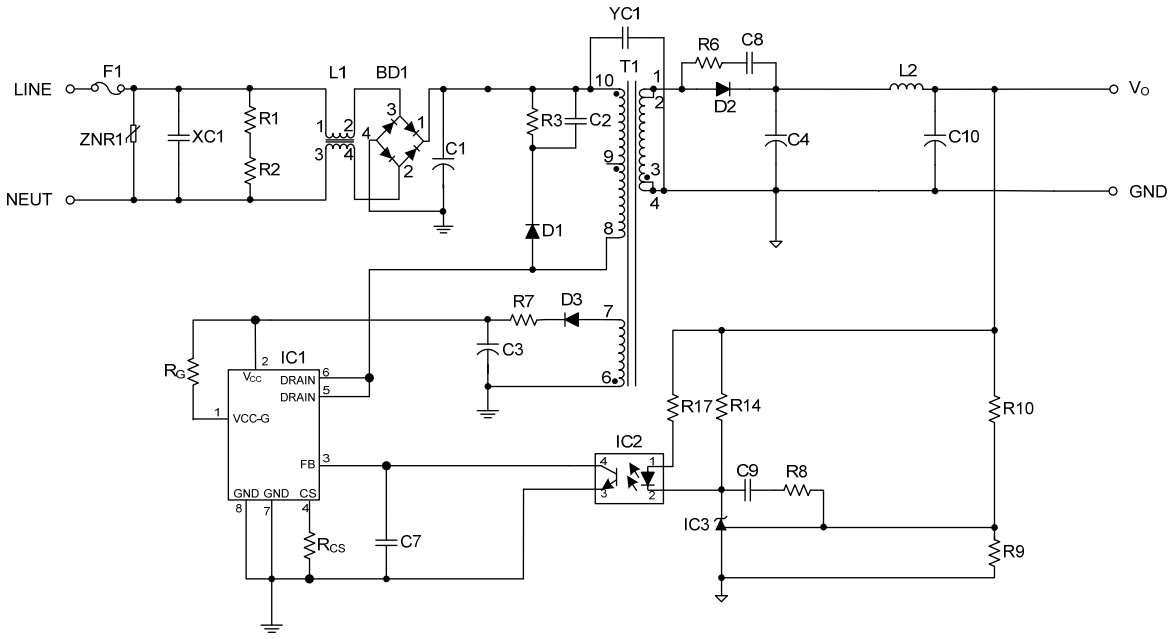
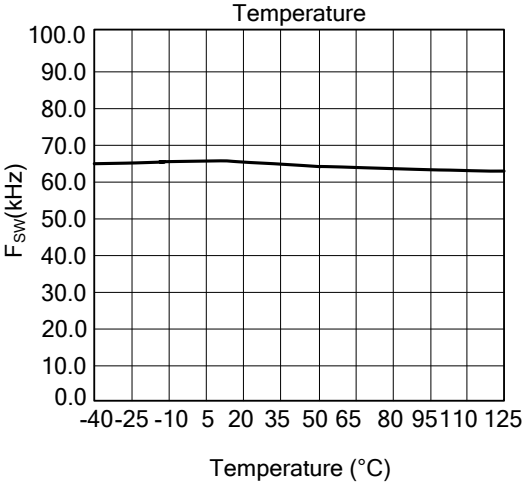


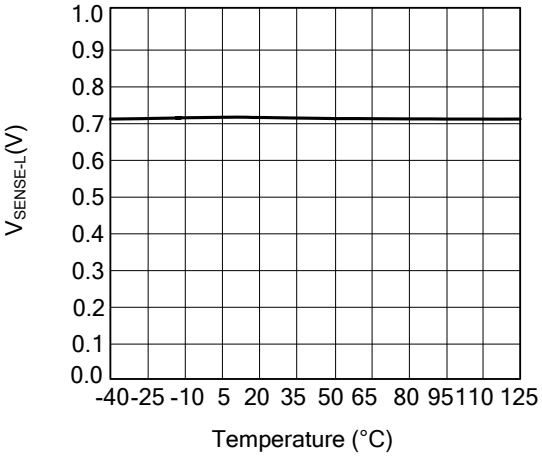
Fig.7 UTC **UCS1652S** Typical Application Circuit

■ TYPICAL CHARACTERISTICS

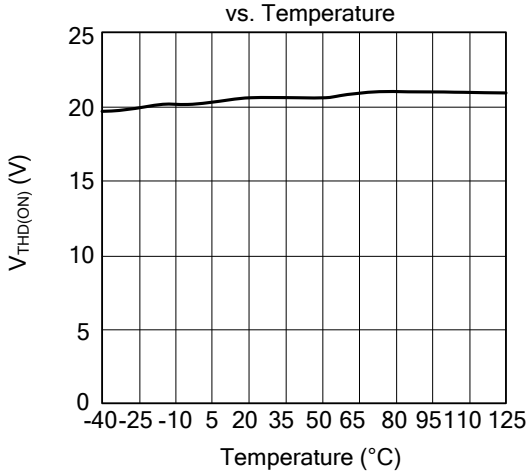
Switch Frequency (F_{SW}) vs. Temperature



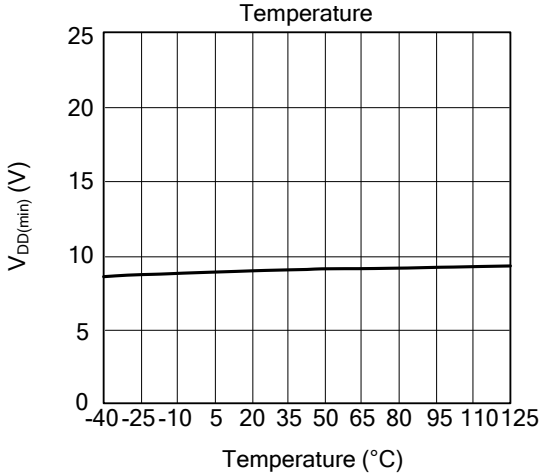
$V_{SENSE-L}$ vs. Temperature



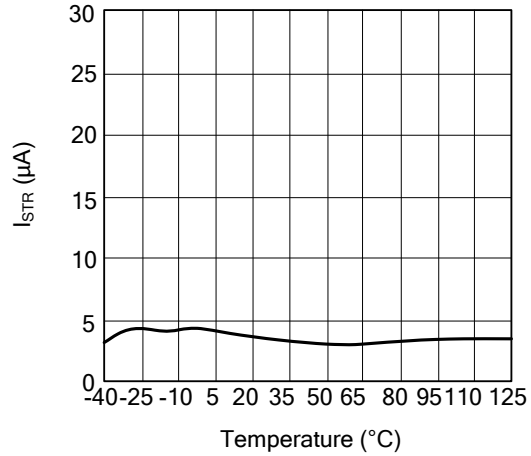
Start-up Threshold Voltage ($V_{THD(ON)}$) vs. Temperature



Min. Operating Voltage ($V_{DD\ (min)}$) vs. Temperature



Start-up Crrent (I_{STR}) vs. Temperature



Max. Duty Cycle (D_{MAX}) vs. Temperature