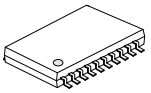
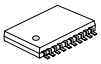
U74LVC241

CMOS IC

OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS



SOP-20



TSSOP-20U

■ DESCRIPTION

The **U74LVC241** contains two 4-bit line drivers with separate output-enable(1$\overline{OE}$ /2OE) inputs. When (1$\overline{OE}$ /2OE) is low and high, the device passes data from the A to the Y. When(1$\overline{OE}$ /2OE) is high and low, the outputs are in the high-impedance state.

The **U74LVC241** can be used in a mixed 3.3V/5V system environment. This device has power-down protective circuit, preventing device destruction when it is powered down.

■ FEATURES

* Operate From 1.65V to 3.6V
* Input Accept Voltages to 5.5V
* Partial-Power-Down Mode Operation
* Max t_{PD} is 6.1ns at 3.3V

■ ORDERING INFORMATION

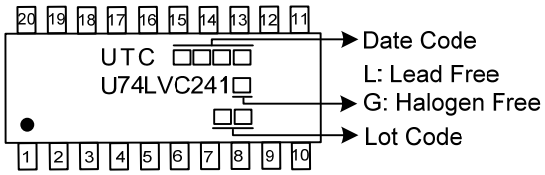
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC241L-S20-R	U74LVC241G-S20-R	SOP-20	Tape Reel
U74LVC241L-ULA-R	U74LVC241G-ULA-R	TSSOP-20U	Tape Reel

U74LVC241G-S20-R

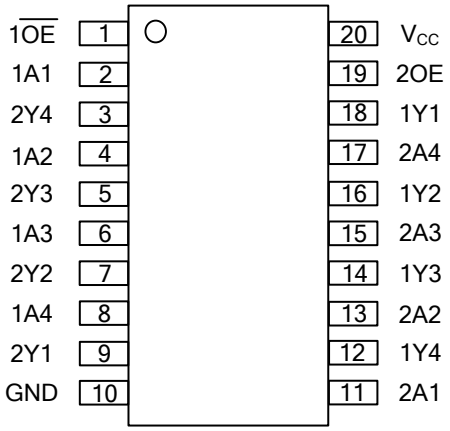
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) S20: SOP-20, ULA: TSSOP-20U
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

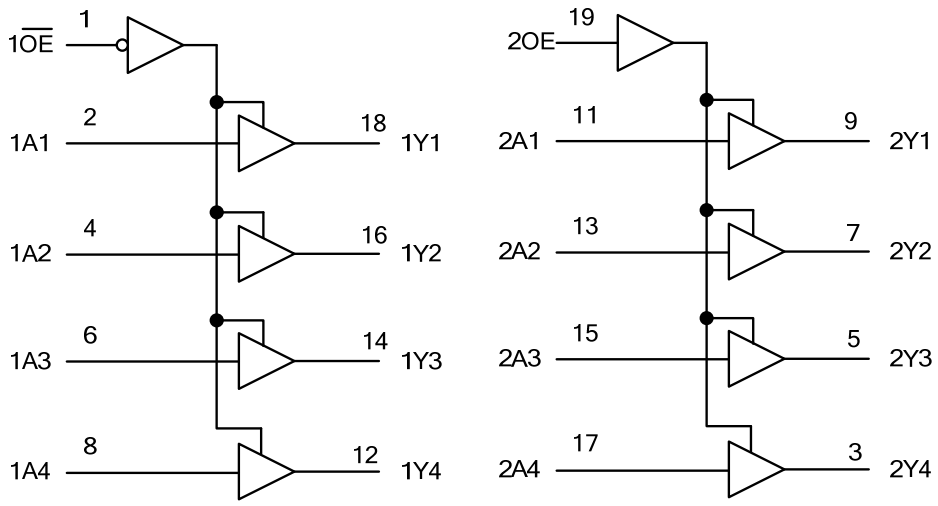


■ FUNCTION TABLE (each gate)

INPUT				OUTPUT	
1$\overline{OE}$	1An	2OE	2An	1Yn	2Yn
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level；L = Low voltage level
X = Don't care；Z = High-impedance OFF-state

■ LOGIC DIAGRAM (Positive Logic)



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +6.5	V
Input Voltage	V_{IN}		-0.5 ~ +6.5	V
Output Voltage	V_{OUT}	Output in the high or low state	-0.5 ~ V_{CC} +0.5	V
		Output in the power-off state	-0.5 ~ +6.5	V
Continuous V_{CC} or GND Current	I_{CC}		±100	mA
Continuous Output Current	I_{OUT}	V_{OUT}=0V ~ V_{CC}	±50	mA
Input Clamp Current	I_{IK}	V_{IN}<0V	-50	mA
Output Clamp Current	I_{OK}	V_{OUT}>V_{CC} or V_{OUT}<0V	-50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		3.6	V
		Data retention only	1.2			V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}	High or low state	0		V_{CC}	V
		Power-off state	0		5.5	V
Input Transition Rise or Fall Rate	Δt/Δv	V_{CC}=1.65V ~ 2.7V	0		20	ns/V
		V_{CC}=2.7V ~ 3.6V	0		10	ns/V
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	V_{CC}=1.8V±0.15V	0.65×V_{CC}			V
		V_{CC}=2.5V±0.2V	1.7			V
		V_{CC}=3.3V±0.3V	2			V
Low-level Input Voltage	V_{IL}	V_{CC}=1.8V±0.15V			0.35×V_{CC}	V
		V_{CC}=2.5V±0.2V			0.7	V
		V_{CC}=3.3V±0.3V			0.8	V
High-Level Output Voltage	V_{OH}	V_{CC}=1.65 ~ 3.6V, I_{OH}=-100μA	V_{CC}-0.2			V
		V_{CC}=1.65V, I_{OH}=-4mA	1.2			V
		V_{CC}=2.3V, I_{OH}=-8mA	1.7			V
		V_{CC}=2.7V, I_{OH}=-12mA	2.2			V
		V_{CC}=3.0V, I_{OH}=-18mA	2.4			V
		V_{CC}=3.0V, I_{OH}=-24mA	2.2			V
Low-Level Output Voltage	V_{OL}	V_{CC}=1.65 ~ 3.6V, I_{OL}=100μA			0.2	V
		V_{CC}=1.65V, I_{OL}=4mA			0.45	V
		V_{CC}=2.3V, I_{OL}=8mA			0.7	V
		V_{CC}=2.7V, I_{OL}=12mA			0.4	V
		V_{CC}=3.0V, I_{OL}=24mA			0.55	V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=3.6V, V_{IN}=5.5V or GND		±0.1	±5	μA
Power OFF Leakage Current	I_{off}	V_{CC}=0V, V_{IN} or V_{OUT}=5.5V		0.1	±10	μA
OFF-state output current	I_{OZ}	V_{CC}=3.6V, V_{IN} = V_{IH} or V_{IL}, V_{OUT}=5.5V or GND		0.1	±10	μA
Quiescent Supply Current	I_{CC}	V_{CC}=2.7 ~ 3.6V, V_{IN}=V_{CC} -0.6V, I_{OUT}=0A		0.1	10	μA
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	V_{CC}=3 ~ 5.5V, One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND		5	500	μA
Input Capacitance	C_I	V_{CC}=0 ~ 3.6V, V_{IN}=GND to V_{CC}		5.0		pF

■ SWITCHING CHARACTERISTICS (Unless otherwise specified)

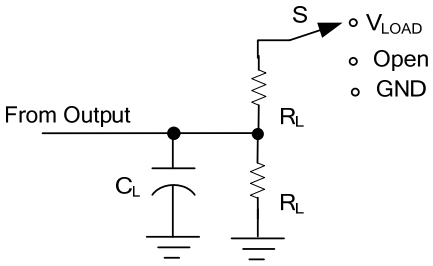
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (An) to output(Yn)	t_{PD}	V_{CC}=1.8V±0.15V	1.5	5.9	14.1	ns
		V_{CC}=2.5V±0.2V	1.0	3.2	7.3	ns
		V_{CC}=2.7V	1.5	3.2	7.1	ns
		V_{CC}=3.3V±0.3V	1.5	2.7	6.1	ns
Propagation delay from input (1 $\overline{OE}$) to output(1Yn)	t_{en}	V_{CC}=1.8V±0.15V	1.5	6.6	16.2	ns
		V_{CC}=2.5V±0.2V	1.5	3.7	8.9	ns
		V_{CC}=2.7V	1.5	3.8	8.1	ns
		V_{CC}=3.3V±0.3V	1.5	3.0	7.1	ns
Propagation delay from input (2OE) to output(2Yn)	t_{en}	V_{CC}=1.8V±0.15V	2.5	5.5	13.8	ns
		V_{CC}=2.5V±0.2V	2.1	4.2	7.4	ns
		V_{CC}=2.7V	1.5	3.7	8.1	ns
		V_{CC}=3.3V±0.3V	1.5	3.4	7.1	ns
Propagation delay from input (1 $\overline{OE}$) to output(1Yn)	t_{dis}	V_{CC}=1.8V±0.15V	2.5	4.3	10	ns
		V_{CC}=2.5V±0.2V	1.0	3.5	5.6	ns
		V_{CC}=2.7V	1.5	3.2	7.0	ns
		V_{CC}=3.3V±0.3V	1.5	3.0	6.0	ns
Propagation delay from input (2OE) to output(2Yn)	t_{dis}	V_{CC}=1.8V±0.15V	1.5	3.5	9.9	ns
		V_{CC}=2.5V±0.2V	0.5	3.1	5.6	ns
		V_{CC}=2.7V	1.5	3.4	7.0	ns
		V_{CC}=3.3V±0.3V	1.5	2.6	6.0	ns

■ OPERATING CHARACTERISTICS

(f=10MHz, V_{IN}=GND to V_{CC}, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	V_{CC}=1.8V±0.15V		14.4		pF
		V_{CC}=2.5V±0.2V		17.9		pF
		V_{CC}=3.3V±0.3V		21		pF

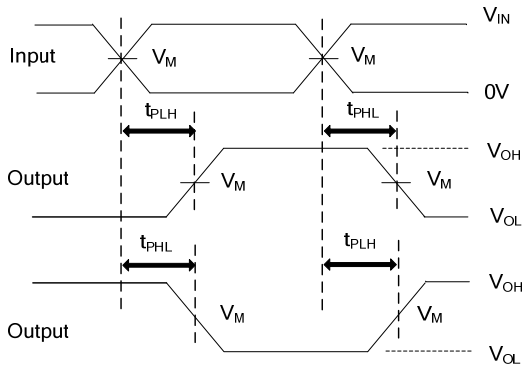
■ TEST CIRCUIT AND WAVEFORMS



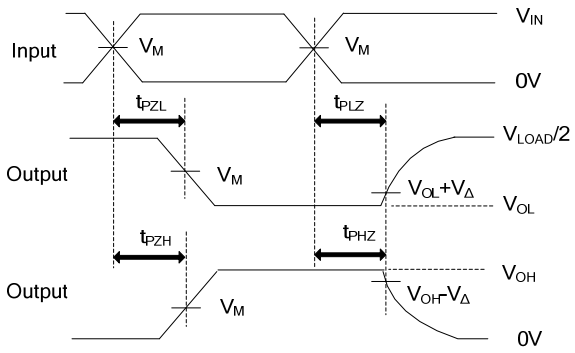
TEST CIRCUIT

TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{LOAD}

V_{CC}	V_{IN}	t_R/t_F	V_M	$V_\triangle$	C_L	R_L	V_{EXT}		
							t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	0.15V	30pF	1KΩ	OPEN	GND	$2\times V_{CC}$
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	0.15V	30pF	500Ω	OPEN	GND	$2\times V_{CC}$
2.7V	2.7V	≤2.5ns	1.5V	0.3V	50pF	500Ω	OPEN	GND	$2\times V_{CC}$
3.3V±0.3V	2.7V	≤2.5ns	1.5V	0.3V	50pF	500Ω	OPEN	GND	$2\times V_{CC}$



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω.