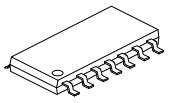
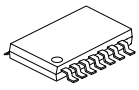
U74LVC32A

CMOS IC

QUAD 2-INPUT POSITIVE-OR GATE



SOP-14U



TSSOP-14U

QFN-14(2.5×3.0)

■ DESCRIPTION

The **U74LVC32A** is a quad 2-input positive-OR gate which performs the function Y=A+B or $Y=\overline{A}\bullet\overline{B}$. It is designed for 1.65V to 3.6V operation.

■ FEATURES

* Wide supply voltage range from 1.65V to 3.6V
* Max t_{pd} of 4.4ns at 3.3V
* Up to 5.5V inputs accept voltages
* Low power consumption, I_{CC} = 10 μA (Max.)
* ±24 mA output driver at 3V
* Typical V_{OLP} (Output Ground Bounce) < 0.8V, V_{CC} = 3.3 V, T_A = 25 ºC
* Typical V_{OHV} (Output V_{OH} undershoot) > 2V, V_{CC} = 3.3 V, T_A = 25 ºC

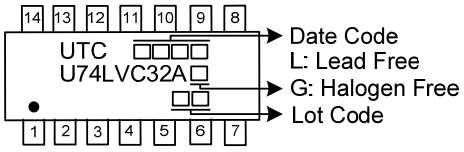
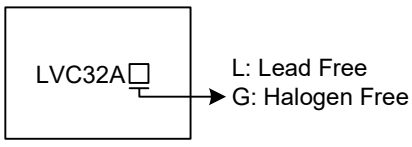
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC32AL-UEA-R	U74LVC32AG-UEA-R	SOP-14U	Tape Reel
U74LVC32AL-UEB-R	U74LVC32AG-UEB-R	TSSOP-14U	Tape Reel
U74LVC32AL-QAF-R	U74LVC32AG-QAF-R	QFN-14(2.5×3.0)	Tape Reel

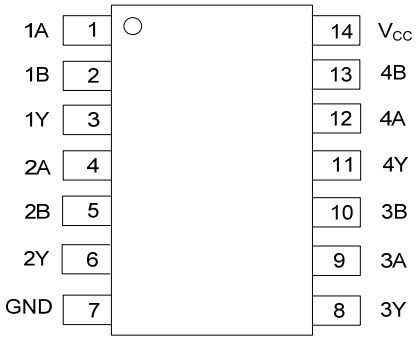
U74LVC32AG-UEA-R
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) UEA: SOP-14U, UEB: TSSOP-14U
QAF: QFN-14(2.5×3.0)
(3) G: Halogen Free and Lead Free, L: Lead Free

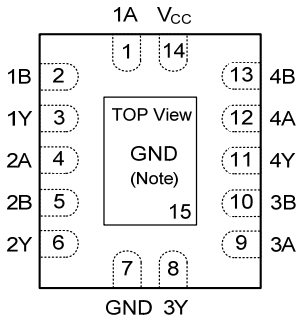
■ MARKING

SOP-14U / TSSOP-14U	QFN-14(2.5×3.0)
	

■ PIN CONFIGURATION



SOP-14U / TSSOP-14U



QFN-14(2.5×3.0)

Note: Connect exposed pad to GND

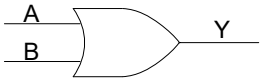
■ PIN DESCRIPTION

PIN	SYMBOL	FUNCTION
1, 4, 9, 12	1A-4A	Data inputs
2, 5, 10, 13	1B-4B	Data inputs
3, 6, 8, 11	1Y-4Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

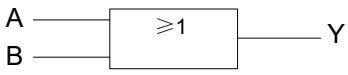
■ FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

■ LOGIC SYMBOL (one gate)



Logic symbol



IEEE/IEC symbol

■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{CC}	-0.5 ~ 6.5	V
Input Voltage		V_{IN}	-0.5 ~ 6.5	V
Output Voltage (any output in the high or low state)		V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Clamp Current		I_{IK}	-50	mA
Output Clamp Current		I_{OK}	-50	mA
Output Current		I_{OUT}	±50	mA
V_{CC} or GND Current		I_{CC}	±100	mA
Power Dissipation	T_A=-40°C to +125°C	P_D	500	mW
Storage Temperature		T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING COMDITIONS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		3.6	V
		Data retention only	1.5			V
High-Level Input Voltage	V_{IH}	V_{CC}=1.65V to 1.95V	0.65× V_{CC}			V
		V_{CC}=2.3V to 2.7V	1.7			V
		V_{CC}=2.7V to 3.6V	2			V
Low-Level Input Voltage	V_{IL}	V_{CC}=1.65V to 1.95V			0.35× V_{CC}	V
		V_{CC}=2.3V to 2.7V			0.7	V
		V_{CC}=2.7V to 3.6V			0.8	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
High-level Output Current	I_{OH}	V_{CC}=1.65V			-4	mA
		V_{CC}=2.3V			-8	mA
		V_{CC}=2.7V			-12	mA
		V_{CC}=3V			-24	mA
Low-level Output Current	I_{OL}	V_{CC}=1.65V			4	mA
		V_{CC}=2.3V			8	mA
		V_{CC}=2.7V			12	mA
		V_{CC}=3V			24	mA
Input Transition Rise or Fall Rate	Δt/Δv		0		7	ns/V
Operating Temperature	T_A		-40		+125	°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-14U	θ_{JA}	125	°C/W
	TSSOP-14U		150	°C/W
	QFN-14(2.5×3.0)		130	°C/W

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
High-Level Output Voltage	V_{OH}	V_{CC}=1.65V to 3.6V, I_{OH}=-100μA	V_{CC}-0.2			V
		V_{CC}=1.65V, I_{OH}=-4mA	1.2			V
		V_{CC}=2.3V, I_{OH}=-8mA	1.7			V
		V_{CC}=2.7V, I_{OH}=-12mA	2.2			V
		V_{CC}=3V, I_{OH}=-12mA	2.4			V
		V_{CC}=3V, I_{OH}=-24mA	2.2			V
Low-Level Output Voltage	V_{OL}	V_{CC}=1.65V to 3.6V, I_{OL}=100μA			0.2	V
		V_{CC}=1.65V, I_{OL}=4m			0.45	V
		V_{CC}=2.3V, I_{OL}=8mA			0.7	V
		V_{CC}=2.7V, I_{OL}=12mA			0.4	V
		V_{CC}=3V, I_{OL}=24mA			0.55	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=0 to 3.6V, V_{IN}=5.5V or GND			±5	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND, I_{OUT}=0			10	μA
Additional quiescent Supply Current	ΔI_{CC}	One input at V_{CC}–0.6V Other input sat V_{CC} or GND			500	μA
Input Capacitance	C_{IN}	V_{CC}=3.3V, V_{IN}=V_{CC} or GND		5		pF

Note: 1. All typical values are at V_{CC} = 3.3V

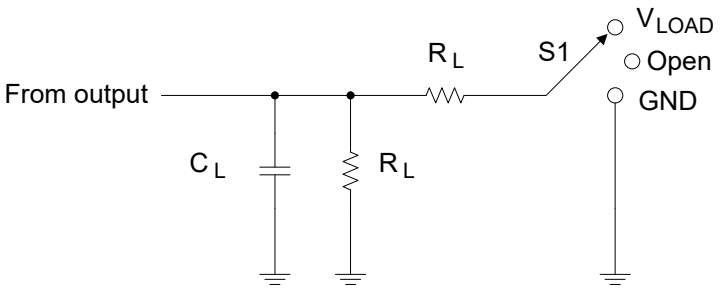
■ SWITCHING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (A or B) to output (Y)	t_{PLH}/t_{PHL}	V_{CC}=1.8V±0.15V, C_L=30pF, R_L=1KΩ	1		8.7	ns
		V_{CC}=2.5±0.2V, C_L=30pF, R_L=500Ω	1		5.4	ns
		V_{CC}=2.7V, C_L=50pF, R_L=500Ω			4.4	ns
		V_{CC}=3.3±0.3V, C_L=50pF, R_L=500Ω	1.5		3.8	ns
Skew between any two outputs of the same package switching in the same direction	$t_{sk(o)}$	V_{CC}=3.3±0.3V, C_L=50pF, R_L=500Ω			1	ns

■ OPERATING CHARACTERISTICS (f=10MHz, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power dissipation capacitance per gate	C_{PD}	V_{CC}=1.8V		7.5		pF
		V_{CC}=2.5V		10.6		pF
		V_{CC}=3.3V		12.5		pF

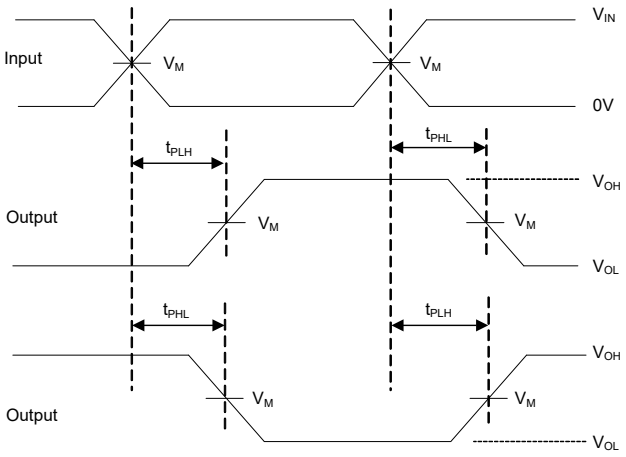
■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open

V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L
	V_{IN}	t_r, t_f				
1.8V±0.15V	V_{CC}	≤ 2ns	$V_{CC}/2$	$2\times V_{CC}$	30pF	1KΩ
2.5V±0.2V	V_{CC}	≤ 2ns	$V_{CC}/2$	$2\times V_{CC}$	30pF	500Ω
2.7V	V_{CC}	≤ 2.5ns	1.5V	6V	50pF	500Ω
3.3V±0.3V	V_{CC}	≤ 2.5ns	1.5V	6V	50pF	500Ω



Propagation delay times
Inverting and noninverting outputs

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω.