



UU9792

Preliminary

CMOS IC

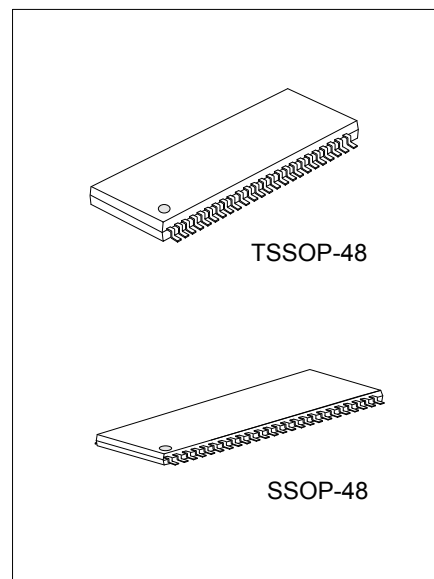
LCD SEGMENT DRIVERS STANDARD SEGMENT DRIVER

DESCRIPTION

The UTC **UU9792** is a LCD Segment Driver: 36 Segment output, 4 Common output

FEATURES

- * LCD driving port: 4 Common output, 36 Segment output
- * 2wire serial interface (SCL, SDA)
- * Integrated RAM for display data (DDRAM): 36×4bit
- * Integrated Oscillation circuit
- * Integrated Power supply circuit for LCD driving: 1/2 Bias , 1/3 Bias, 1/4 Duty
- * Low power consumption design
- * Operation power supply :2.5~5.5V



ORDERING INFORMATION

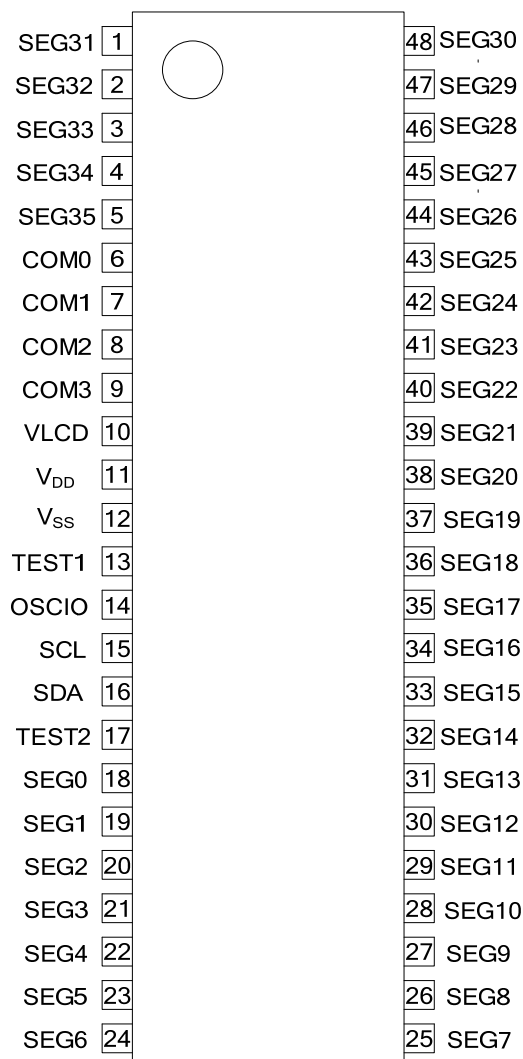
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UU9792L-R48-T	UU9792G-R48-T	SSOP-48	Tape Reel
UU9792L-P48-R	UU9792G-P48-R	TSSOP-48	Tape Reel

<p>UU9792G-R48-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) R48: SSOP-48, P48: TSSOP-48</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



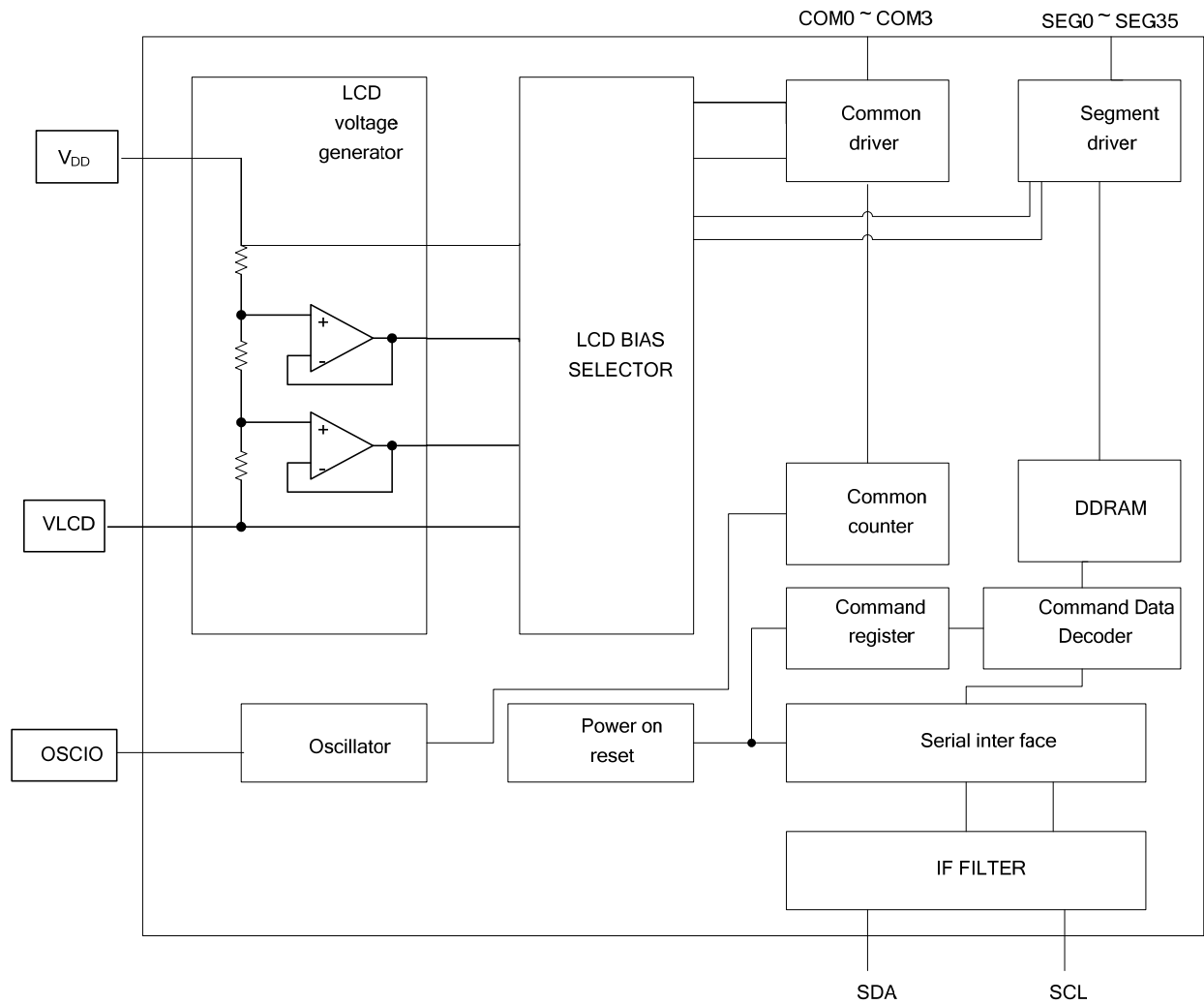
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1 ~ 5	SEG31-SEG35	SEGMENT output for LCD driving
18 ~ 48	SEG0-SEG30	
6 ~ 9	COM0~COM3	COMMON output for LCD driving
10	VLCD	Power supply for LCD driving
11	V _{DD}	Power supply
12	V _{SS}	GND
13	TEST1	TEST input Must be connected to VSS
14	OSCIO	External clock input. External clock and internal clock can be selected by command. Must be connected to VSS when internal oscillation circuit is used
15	SCL	Serial data transfer clock
16	SDA	Serial data input
17	TEST2	POR enable set H: POR disable(Use Soft ware Reset) L: POR enable

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Voltage	V_{DD}	-0.5 ~ +7.0	V
Power Supply for LCD driving	V_{LCD}	-0.5 ~ V_{DD}	V
Input voltage range	V_{IN}	-0.5 ~ $V_{DD}+0.5$	V
Operation temperature	T_{OPR}	-40 ~ +85	°C
Storage temperature range	T_{STG}	-55 ~ +125	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ STANDARD OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply	V_{DD}	2.5		5.5	V
Power Supply for LCD driving	V_{LCD}	2.5		5.5	V
Operating Temperature Range	T_{OPR}	-40		+85	°C

■ ELECTRICAL CHARACTERISTICS

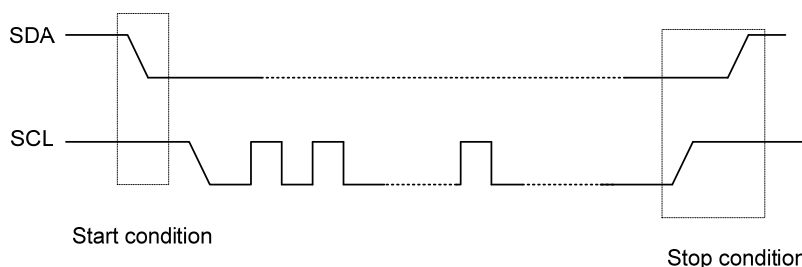
DC Characteristics ($V_{DD}=2.5 \sim 5.5V$, $V_{LCD}=2.5 \sim 5.5V$, $V_{SS}=0V$, $T_A=-40 \sim 85^{\circ}C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
"H" level input voltage	V_{IH}	SDA SCL	$0.7 \times V_{DD}$		V_{DD}	V
"L" level input voltage	V_{IL}	SDA SCL	V_{SS}		$0.3 \times V_{DD}$	V
Standby current	I_{ST}	Display off Oscillation off			5	uA
Operation current	I_{DD1}	$V_{DD}=3.3V$, $T_A=25^{\circ}C$, Power save mode1, FR=Power save model1, 1/3Bias, Frame inverse			20	uA
Frame frequency	f_{CLK}	$V_{DD}=3.3V$		80		Hz
SCL cycle time	t_{SCL}		2.5			us
LCD Driver on resistance	SEG	RON	$I_{LOAD}=\pm 10uA$	3.5		K Ω
	COM			3.5		K Ω

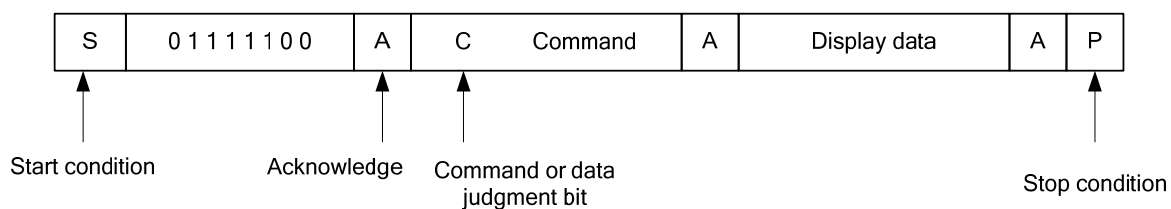
■ FUNCTION DESCRIPTIONS

Command/Data transfer method

This device is controlled by 2wire serial signal(SDA,SCL).



It has to generate the condition such as Start condition and Stop condition in 2wire serial interface transfer method.



Method of how to transfer command and data is shown as follows.

1. Generate "start condition"
2. Issue Slave address
3. Transfer command and display data

Acknowledge

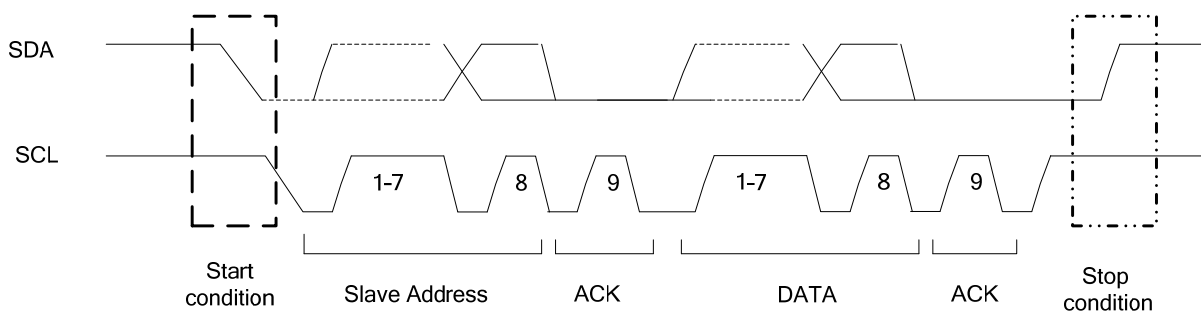
Data format is 8bits and return Acknowledge after transfer 8bits data.

When SCL 8th = "L" after transfer 8bit data (Slave address, Command display data),output open SDA line.

When SCL 9th = "L", stop output function.

(As Output format is NMOS-Open-Drain, can't output 'H' level.)

If no need Acknowledge function, Please input 'L' level from SCL 8th= 'L' to SCL 9th= 'L'



■ FUNCTION DESCRIPTIONS (Cont.)

Command transfer method

Issue the Slave Address (01111100) after the start condition is generated.

Command input follows after the Slave Address. The least significant bit (LSB) of the Slave Address determines if the operation to be done is Write or Read operation.

The MSB (command or data judgment bit) defines if the succeeding byte is a command or data.

When "Command or data judgment bit" = '1', the next byte is a command.

When "Command or data judgment bit" = '0', the next byte is display data.

S	Slave address	A	1 Command	A	1 Command	A	0 Command	A	Display	...	P
---	---------------	---	-----------	---	-----------	---	-----------	---	---------	-----	---

Once it enters display data transfer condition, it cannot input any command.

To input command again, please generate the "START condition" again.

If "START condition" or "STOP condition" is inputted in the middle of command transmission, the command will be cancelled. If the Slave address is continuously inputted following "START condition", it will be in command input condition.

Please input "Slave Address" in the first data transmission after "START condition".

When Slave Address cannot be recognized in the first data transmission, Acknowledge does not return and the next transmission will be invalid. When data transmission is in invalid status and the "START condition" is transmitted again, it will return to valid status.

Write display and transfer method

This device has Display Data RAM(DDRAM) of 20×4=80bit.

The relationship between data input and display data, DDRAM data and address are as follows.

Slave address			Command								
S	0 1 1 1 1 1 0	A	0	0 0 0 0 0 0 0	A	a b c d e f g h	A	i j k l m n o p	A	...	P

Display Data

The 8-bit display data will be stored in the DDRAM. The address to be written is the address specified by Address Set command, and the address is automatically incremented after every 4-bit of data.

Data can be continuously written in the DDRAM by transmitting Data continuously.

	0	1	2	3																22h	23h							
BIT	0	a	e																					COM0					
	1	b	f																					COM1					
	2	c	g																					COM2					
	3	d	h																					COM3					
		SEG0	SEG1	SEG2	SEG3																	SEG34	SEG35						
																			DDRAM address										

As data transfer to DDRAM is done every 4-bit data.

So it will be finished to transfer with no need to wait ACK.

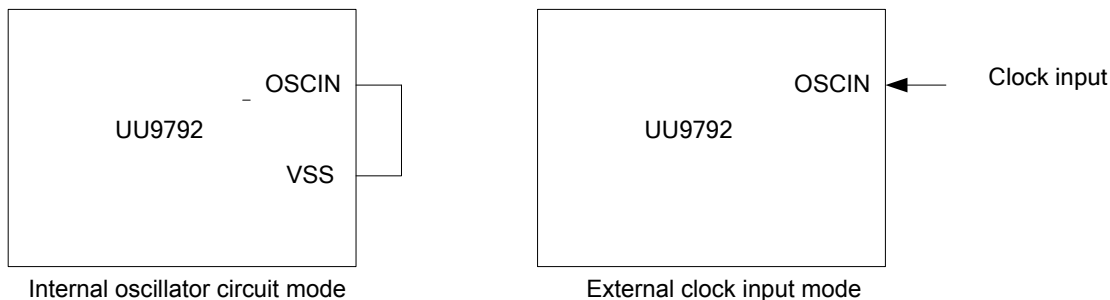
■ FUNCTION DESCRIPTIONS (Cont.)

OSCILLATOR

There are two kinds of clock for logic and analog circuit; from internal oscillator circuit or external clock.

If internal oscillator circuit will be used, OSCIN must be connected to V_{SS}.

When using external clock mode, it has to input external clock from OSCIN terminal after Set IC operation (ICSET) terminal.



LCD Driver Bias Circuit

This device generates LCD driving voltage with on-chip Buffer AMP.

And it can drive LCD at low power consumption.

1/3 Bias or 1/2 Bias can set in Mode Set command.

Line and frame inversion can set in DISCTL command

■ COMMAND

Description List of Command / Function

	Command	Function
1	Address set(ADSET)	DDRAM address setting(00-22h)
2	EVR set (EVRSET)	EVR setting(0-31)
3	Display Control(DISCTL)	Frame Frequency, Power save mode setting
4	IC operation set (ICSET)	LCD drive mode, software reset, display on/off
5	All pixel Control(APCTL)	All pixel control during display ON

■ DETAILED COMMAND DESCRIPTION

D7 (MSB) is bit for command or data judgment.

C:0—Next Byte is RAM write data

1—Next byte is command

Mode Set

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
C	1	0	*	P3	P2	*	*

Set display ON and OFF

Setting	P3	Reset initialize condition
Display off	0	○
Display on	1	

Display off: Regardless of DDRAM data, all SEGMENT and COMMON output will be stopped. Display off mode will be finished by Display on.

Display On: SEGMENT and COMMON output will be active and start to read the display data from DDRAM.

Set Bias level

setting	P2	Reset initialize condition
1/3 Bias	0	○
1/2 Bias	1	

Refer to LCD driving waveform

Address set (ADSET)

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
C	0	0	P4	P3	P2	P1	P0

Address data is specified in P [4:0].

The address range can be set as 00000~10011(2).

When the specified address is out of range, the address will be set to "00000"

Display control (DISCTL)

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
C	0	1	P4	P3	P2	P1	P0

Set Power mode FR

Power save mode FR	P4	P3	Reset initialize condition
Normal mode	0	0	○
Power save mode1	0	1	
Power save mode2	1	0	
Power save mode3	1	1	

*Operation current decrease in

Normal mode > Power save mode1 > Power save mode2 > Power save mode3

■ DETAILED COMMAND DESCRIPTION (Cont.)

Set Power mode SR

Power save mode SR	P1	P0	Reset initialize condition
Power save mode1	0	0	
Power save mode2	0	1	
Normal mode	1	0	○
High Power mode	1	1	

*Operation current increase in order of

Power save mode1 < Power save mode2 < Normal mode < High power mode order

High Power mode: $V_{DD} - V_{LCD} \geq 3.0V$

Setup	Current
Power save mode1	×0.5
Power save mode2	×0.67
Normal mode	×1.0
High power mode	×1.8

Set LCD driving waveform

Set up	P2	Reset initialize condition
Line	0	○
Frame	1	

Set IC Operation (ICSET)

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
C	1	1	0	1	*	P1	P0

Set Software Reset condition

Set up	P1	Reset initialize condition
No operation	0	○
Software reset	1	

Switch between internal clock and external clock

Setup	P0	Reset initialize condition
Internal clock	0	○
External clock input	1	

All Pixel control (APCTL)

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
C	1	1	1	1	1	P1	P0

All display set ON

APON	P1	Reset initialize condition
Normal	0	○
All pixel ON	1	

■ DETAILED COMMAND DESCRIPTION (Cont.)

All display set OFF

APOFF	P1	Reset initialize condition
Normal	0	○
All pixel OFF	1	

All pixels ON: All pixels are ON regardless of DDRAM data.

All pixels OFF: All pixels are OFF regardless of DDRAM data.

AP OFF has higher priority than APON

Blink control (BLKCTL)

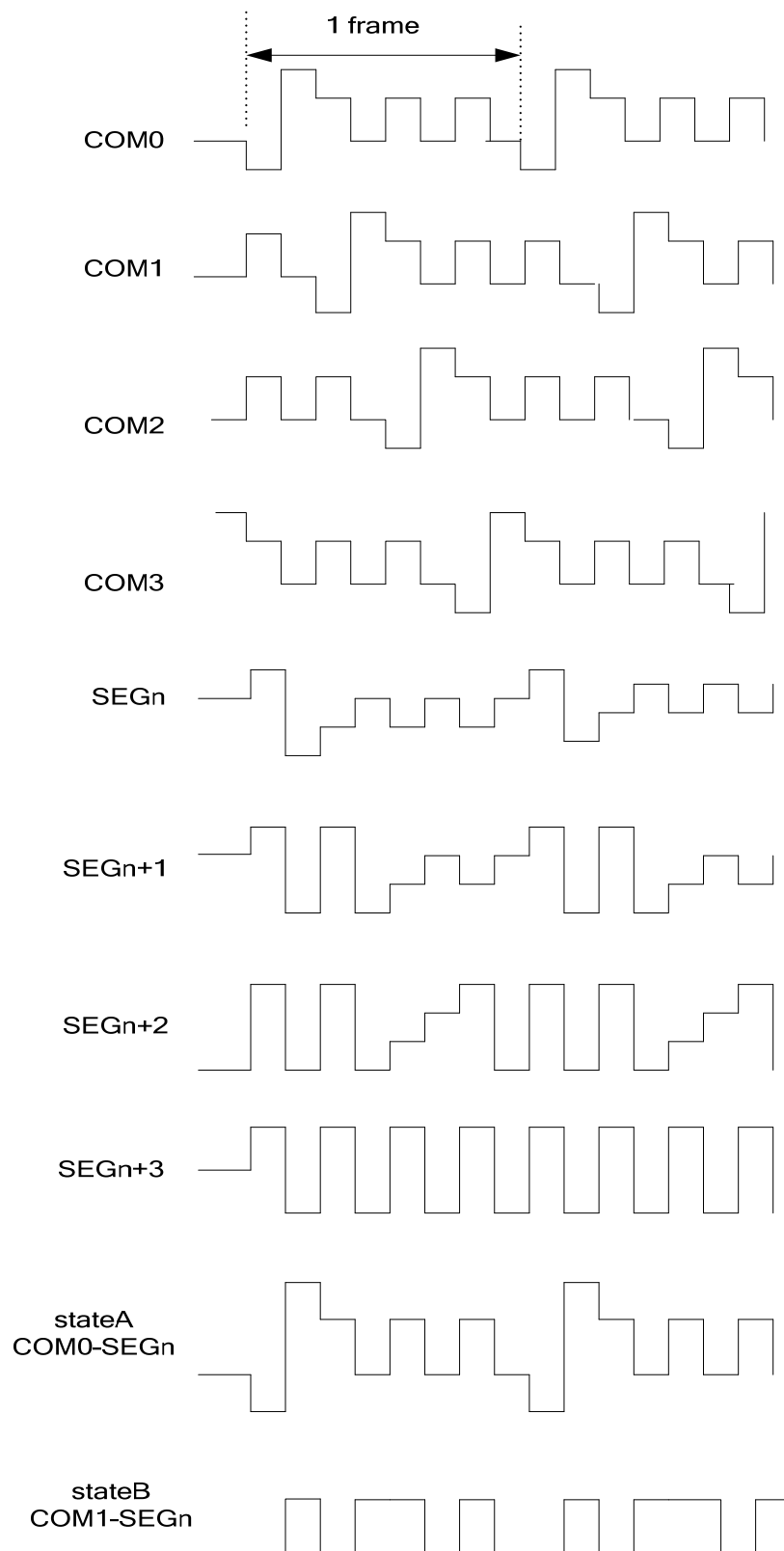
D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
C	1	1	1	0	*	P1	P0

Set blink mode

Blink mode(Hz)	P1	P0	Reset initialize condition
OFF	0	0	○
0.5	0	1	
1	1	0	
2	1	1	

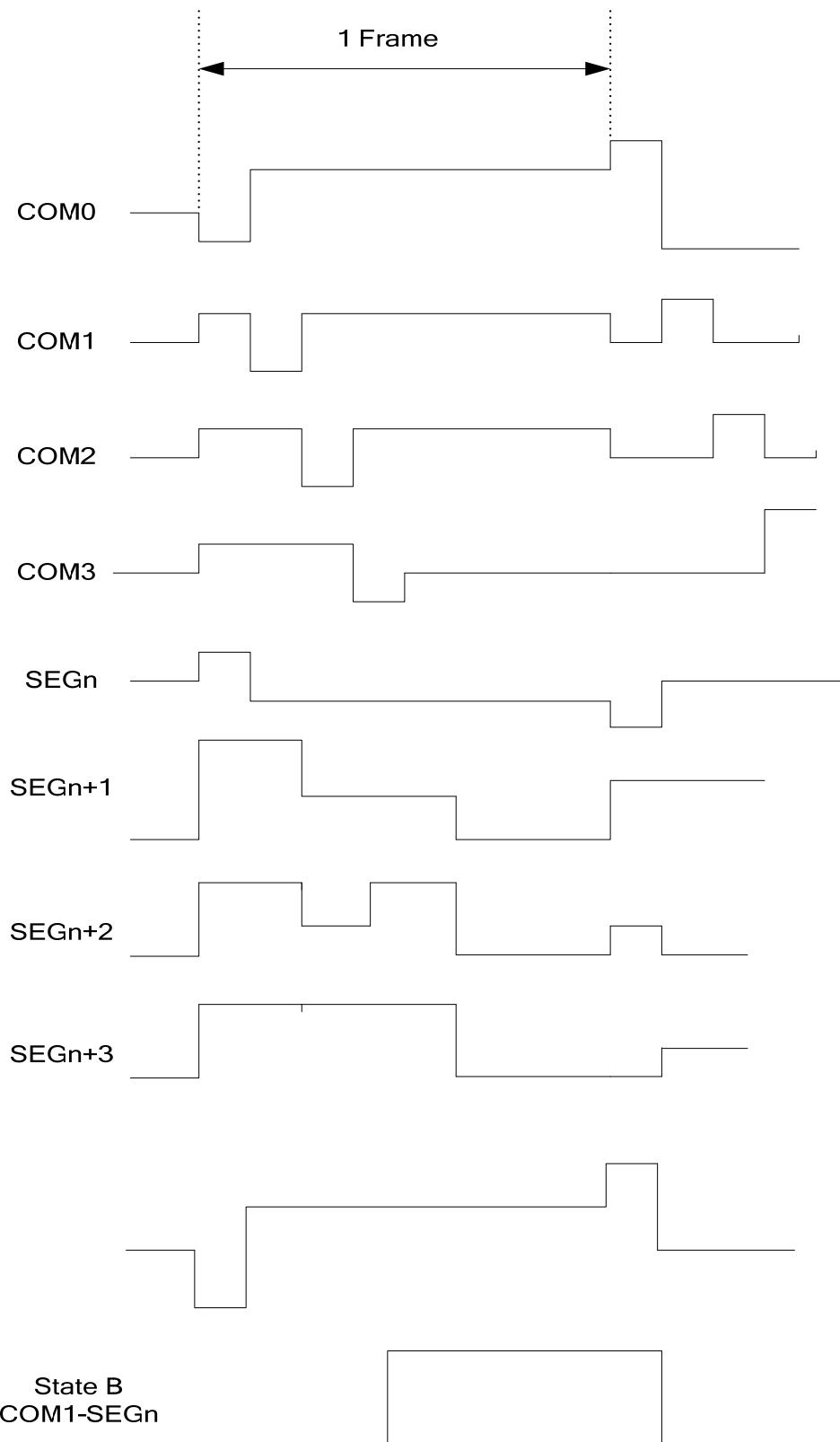
■ LCD DRIVING WAVEFORM

Line inversion mode (1/3 Bias)



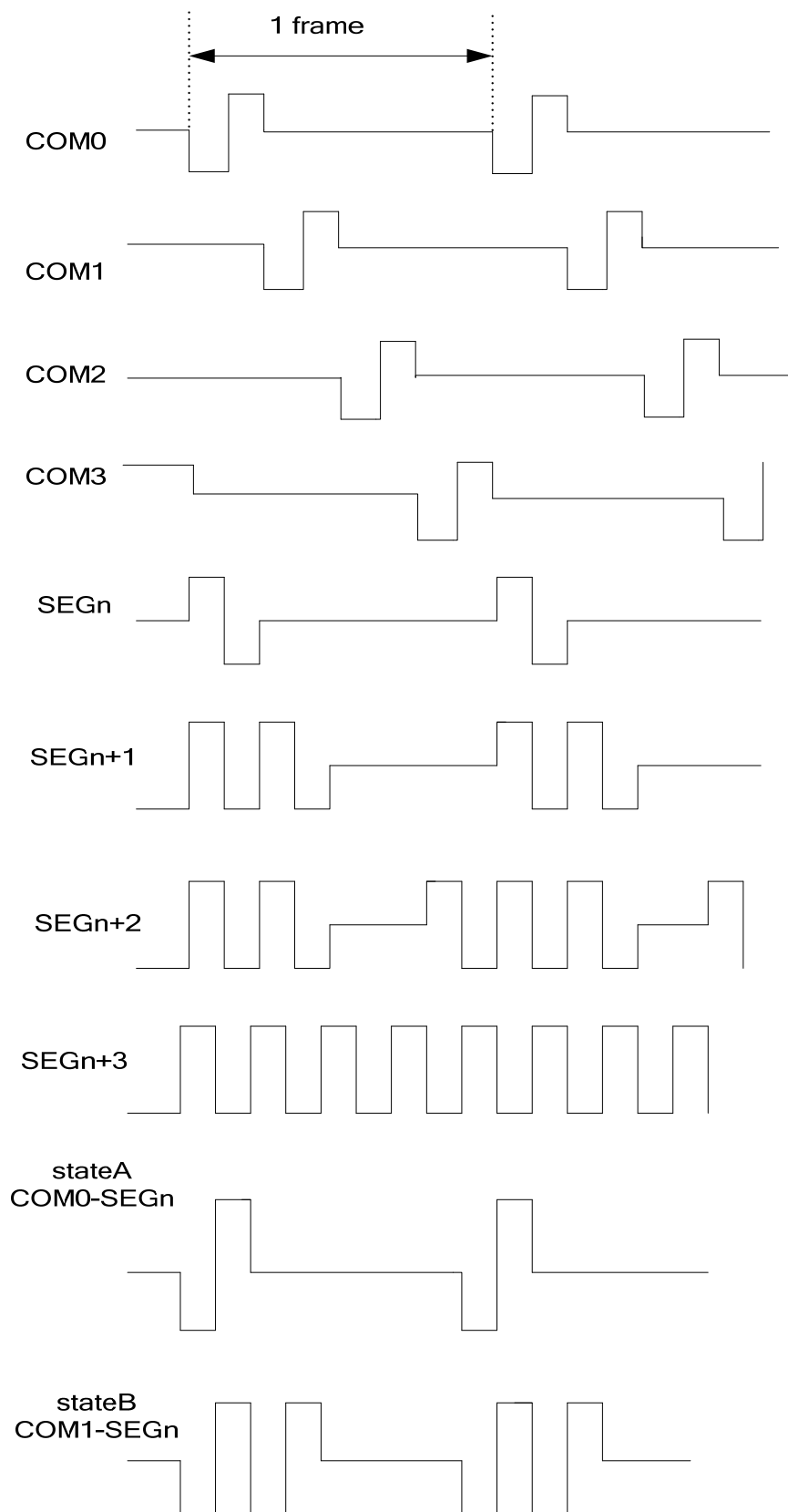
■ LCD DRIVING WAVEFORM (Cont.)

Frame inversion mode



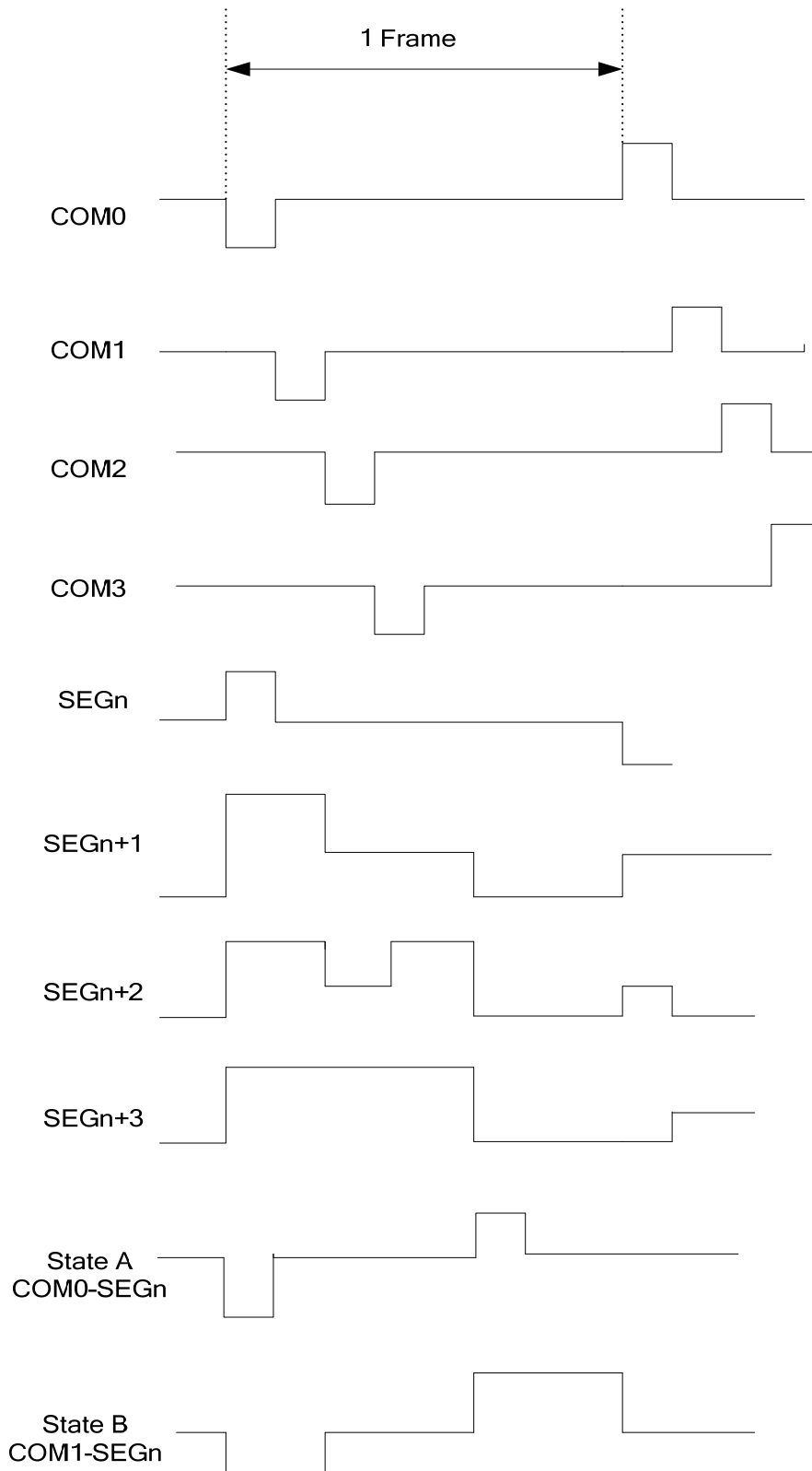
■ LCD DRIVING WAVEFORM (Cont.)

Line inversion mode (1/2 Bias)

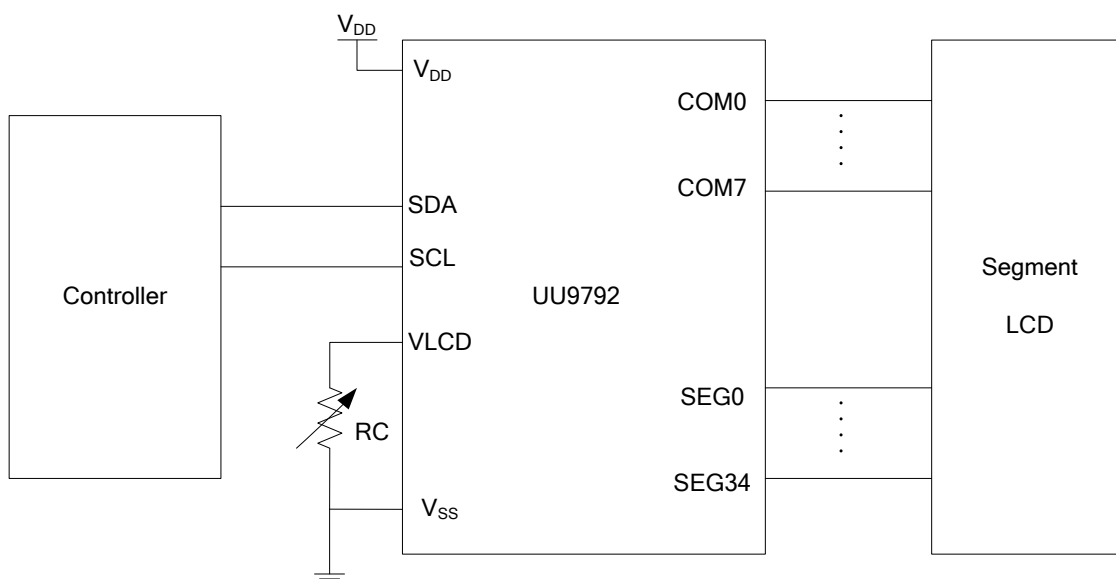


■ LCD DRIVING WAVEFORM (Cont.)

Frame inversion mode



■ TYPICAL APPLICATION CIRCUIT



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