



US2236095

Preliminary

LINEAR INTEGRATED CIRCUIT

ULTRA SMALL, LOW INPUT VOLTAGE, LOW R_{ON} , LOAD SWITCHES

DESCRIPTION

The UTC **US2236095** is ultra-small, low ON resistance (R_{ON}) load switches with controlled turn on. The devices contain a P-channel MOSFET that operates over an input voltage range of 1.0 V to 3.6 V. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals.

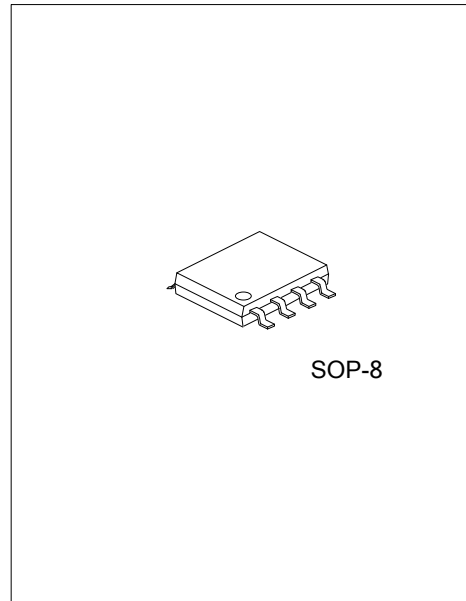
FEATURES

- * Low Input Voltage: 1.0V~3.6V
- * Ultra-Low ON Resistance
 - $R_{ON} = 78\text{ m}\Omega$ at $V_{IN} = 3.6\text{V}$
 - $R_{ON} = 93\text{ m}\Omega$ at $V_{IN} = 2.5\text{V}$
 - $R_{ON} = 109\text{ m}\Omega$ at $V_{IN} = 1.8\text{V}$
 - $R_{ON} = 146\text{ m}\Omega$ at $V_{IN} = 1.2\text{V}$
- * 500mA Maximum Continuous Switch Current
- * Ultra Low Quiescent Current: 82nA at 1.8V
- * Ultra Low Shutdown Current: 44nA at 1.8V
- * Low Control Input Thresholds Enable Use of 1.2V/1.8V/2.5V/3.3V Logic
- * Controlled Slew Rate to Avoid Inrush Currents: 40 μ s t_r

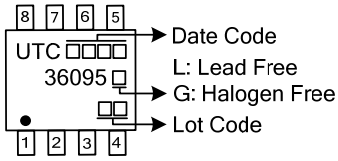
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
US2236095L-S08-R	US2236095G-S08-R	SOP-8	Tape Reel

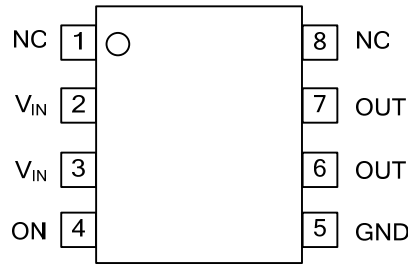
<p>US2236095G-S08-R</p> <ul style="list-style-type: none"> (1) Packing Type (2) Package Type (3) Green Package 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING



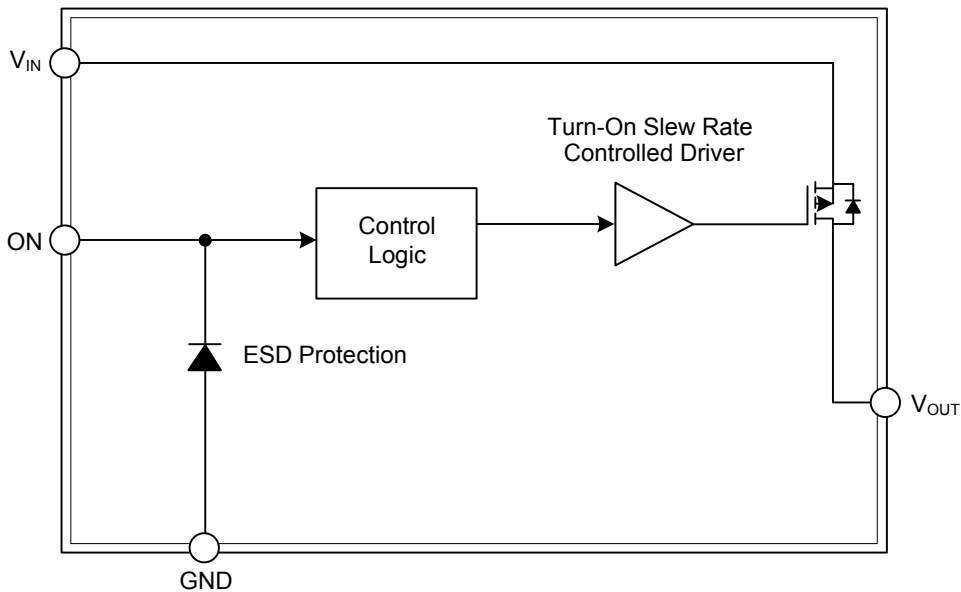
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1, 8	NC	
2, 3	V _{IN}	Switch input, bypass this input with a ceramic capacitor to ground
4	ON	Switch control input, active high
5	GND	Ground
6, 7	V _{OUT}	Switch output

BLOCK DIAGRAM



FUNCTION TABLE

ON (Control Input)	V _{IN} to V _{OUT}
L	OFF
H	ON

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage Range	V_{IN}	4.0	V
Output Voltage Range	V_{OUT}	$V_{IN} + 0.3$	V
Input Voltage Range	V_{ON}	4.0	V
Maximum Continuous Switch Current	I_{MAX}	500	mA
Power Dissipation at $T_A=25^{\circ}C$	P_D	0.48	W
Maximum junction Temperature	T_J	+125	$^{\circ}C$
Operating Temperature Range	T_{OPR}	-40 ~ +85	$^{\circ}C$
Storage Temperature Range	T_{STG}	-65 ~ +150	$^{\circ}C$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	205	$^{\circ}C/W$

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}	1.0		3.6	V
Output Voltage Range	V_{OUT}			V_{IN}	
High-Level Input Voltage, ON	V_{IH}	0.85		3.6	V
Low-Level Input Voltage, ON	V_{IL}			0.4	V
Input Capacitor	C_{IN}	1.0			μF

■ ELECTRICAL CHARACTERISTICS ($V_{IN}=1.0V\sim 3.6V$, $T_A=25^{\circ}C$ unless otherwise specified)

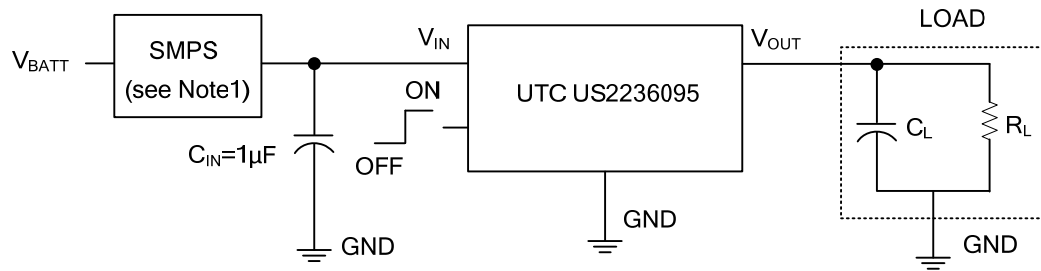
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP (Note)	MAX	UNIT
Quiescent Current	I_{IN}	$I_{OUT}=0$, $V_{IN}=V_{ON}$	$V_{IN}=1.1V$	37	120	nA
			$V_{IN}=1.8V$	82	235	nA
			$V_{IN}=3.6V$	204	880	nA
OFF-State Supply Current	$I_{IN(OFF)}$	$V_{ON}=GND$, $OUT=Open$	$V_{IN}=1.1V$	22	210	nA
			$V_{IN}=1.8V$	44	260	nA
			$V_{IN}=3.6V$	137	700	nA
OFF-State Switch Current	$I_{IN(LEAKAGE)}$	$V_{ON}=GND$, $V_{OUT}=0$	$V_{IN}=1.1V$	22	140	nA
			$V_{IN}=1.8V$	45	230	nA
			$V_{IN}=3.6V$	137	610	nA
ON-State Resistance	R_{ON}	$I_{OUT}=-200mA$	$V_{IN}=3.6V$	78	95	m Ω
			$V_{IN}=2.5V$	93	110	m Ω
			$V_{IN}=1.8V$	109	130	m Ω
			$V_{IN}=1.2V$	146	200	m Ω
			$V_{IN}=1.1V$	174	330	m Ω
ON Input Leakage Current	I_{ON}	$V_{ON}=1.1V\sim 3.6V$ or GND			25	nA

Note: Typical values are at the specified V_{IN} and $T_A=25^{\circ}C$.

■ SWITCHING CHARACTERISTICS ($V_{IN}=3.6V$, $T_A=25^\circ C$ unless otherwise specified)

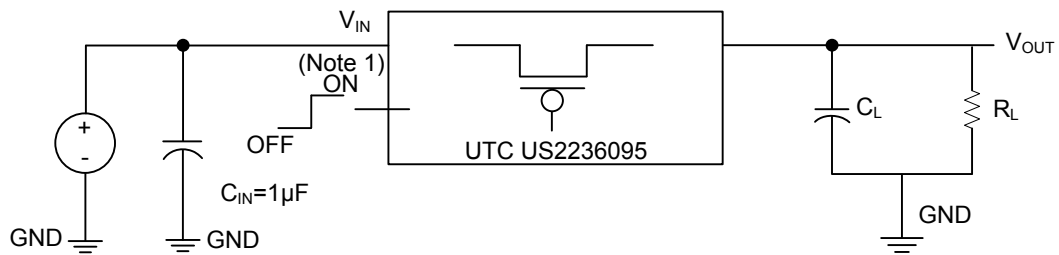
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Turn-ON Time	t_{ON}	$R_L=500\Omega$	$C_L=0.1\mu F$		33		μs
			$C_L=1\mu F$		39		μs
			$C_L=3.3\mu F$		46		μs
Turn-OFF Time	t_{OFF}	$R_L=500\Omega$	$C_L=0.1\mu F$		38		μs
			$C_L=1\mu F$		322		μs
			$C_L=3.3\mu F$		1145		μs
V_{OUT} Rise Time	t_r	$R_L=500\Omega$	$C_L=0.1\mu F$		25		μs
			$C_L=1\mu F$		28		μs
			$C_L=3.3\mu F$		34		μs
V_{OUT} Fall Time	t_f	$R_L=500\Omega$	$C_L=0.1\mu F$		116		μs
			$C_L=1\mu F$		1060		μs
			$C_L=3.3\mu F$		3840		μs

■ TYPICAL APPLICATIONS



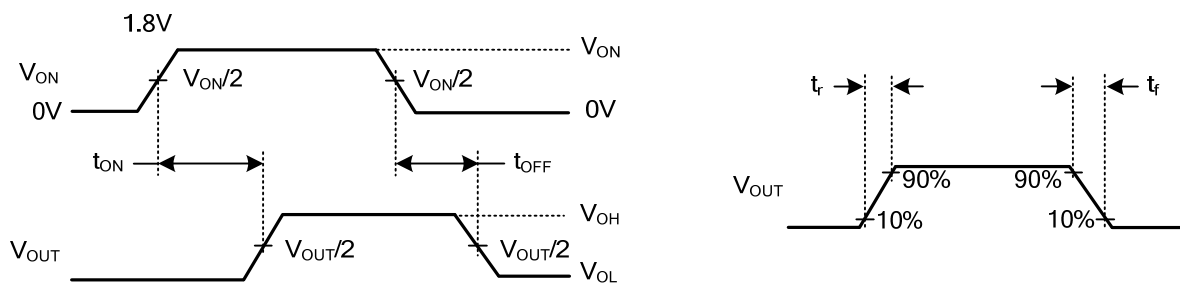
Note: Switched mode power supply

■ TEST CIRCUIT AND WAVEFORMS



Note: t_r and t_f of the control signal is 100ns.

TEST CIRCUIT



t_{ON}/t_{OFF} WAVEFORMS

■ APPLICATION INFORMATION

ON/OFF Control

The ON pin controls the state of the switch. Activating ON continuously holds the switch in the on state so long as there is no fault. ON is active-high and has a low threshold, making it capable of interfacing with low voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2V, 1.8V, 2.5V or 3.3V GPIOs.

Input Capacitor

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{IN} and GND. A 1.0 μ F ceramic capacitor, C_{IN} , placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor, this in order to avoid excessive voltage drop.

Output Capacitor

Due to the integral body diode in the PMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN} .

Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for V_{IN} , V_{OUT} , and GND helps minimize the parasitic electrical effects along with minimizing the case-to-ambient thermal impedance.

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