



## J113

## N-CHANNEL JFET

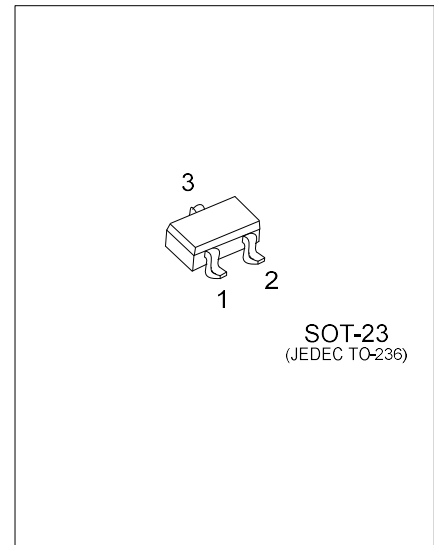
### N-CHANNEL SWITCH

#### DESCRIPTION

The UTC J113 is designed for low level analog switching, sample and hold circuits and chopper stabilized amplifiers.

#### FEATURES

\* Source & Drain are interchangeable.



#### ORDERING INFORMATION

| Ordering Number |               | Package | Pin Assignment |   |   | Packing   |
|-----------------|---------------|---------|----------------|---|---|-----------|
| Lead Free       | Halogen Free  |         | 1              | 2 | 3 |           |
| J113L-AE3-R     | J113G-AE3-R   | SOT-23  | D              | S | G | Tape Reel |
| J113L-AE3-A-R   | J113G-AE3-A-R | SOT-23  | S              | D | G | Tape Reel |

Note: Pin Assignment: D: Drain S: Source G: Gate

|  |   |
|--|---|
| <p>J113G-AE3-A-R</p> <ul style="list-style-type: none"> <li>(1) Packing Type</li> <li>(2) Pin Code</li> <li>(3) Package Type</li> <li>(4) Green Package</li> </ul> | <ul style="list-style-type: none"> <li>(1) R: Tape Reel</li> <li>(2) refer to Pin Assignment</li> <li>(3) AE3: SOT-23</li> <li>(4) G: Halogen Free and Lead Free, L: Lead Free</li> </ul> |
|--|---|

#### MARKING

| J113  | J113-A  |
|---|---|
| <p>J113 □</p> <p>→ L: Lead Free<br/>G: Halogen Free</p> | <p>113A □</p> <p>→ L: Lead Free<br/>G: Halogen Free</p> |

■ **ABSOLUTE MAXIMUM RATINGS** ( $T_A=25^{\circ}\text{C}$ , unless otherwise specified)

| PARAMETER            | SYMBOL    | RATING     | UNIT               |
|----------------------|-----------|------------|--------------------|
| Drain-Gate Voltage   | $V_{DG}$  | 35         | V                  |
| Gate-Source Voltage  | $V_{GS}$  | -30        | V                  |
| Forward Gate Current | $I_{GF}$  | 50         | mA                 |
| Power Dissipation    | $P_D$     | 350        | mW                 |
| Junction Temperature | $T_J$     | +150       | $^{\circ}\text{C}$ |
| Storage Temperature  | $T_{STG}$ | -55 ~ +150 | $^{\circ}\text{C}$ |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **THERMAL DATA**

| PARAMETER           | SYMBOL        | RATING | UNIT                        |
|---------------------|---------------|--------|-----------------------------|
| Junction to Ambient | $\theta_{JA}$ | 357    | $^{\circ}\text{C}/\text{W}$ |
| Junction to Case    | $\theta_{JC}$ | 125    | $^{\circ}\text{C}/\text{W}$ |

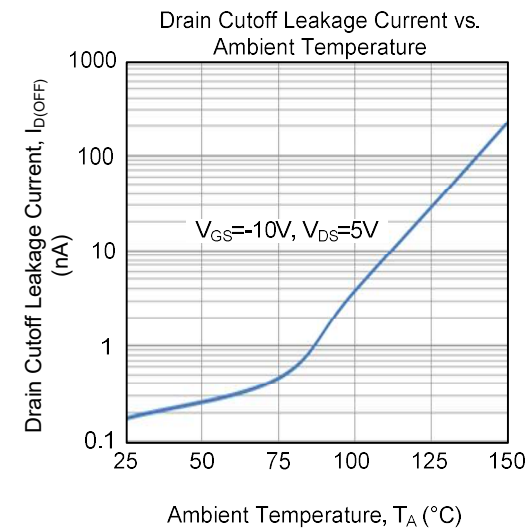
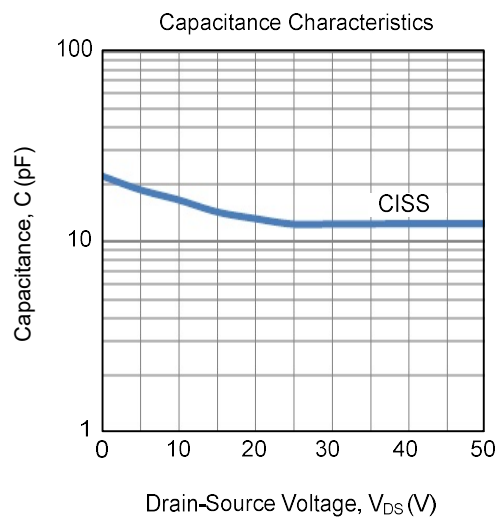
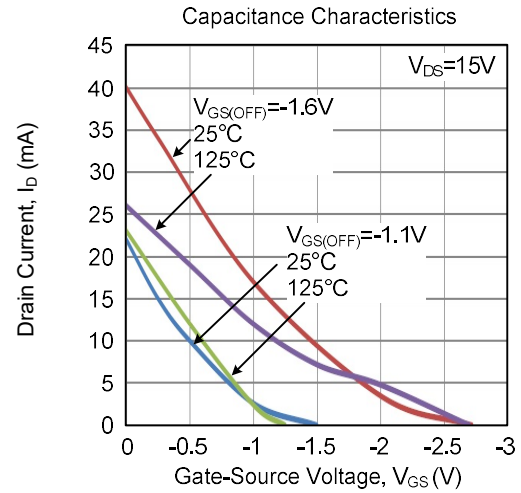
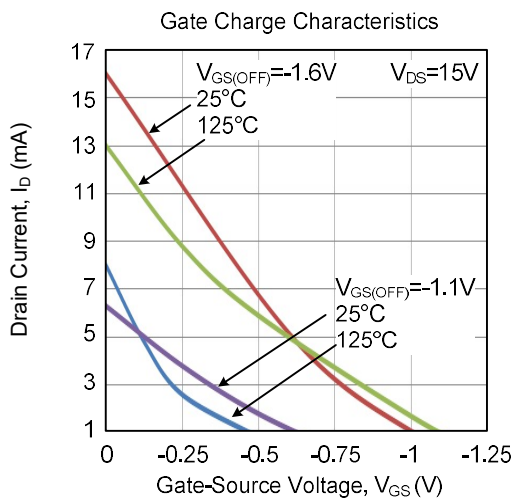
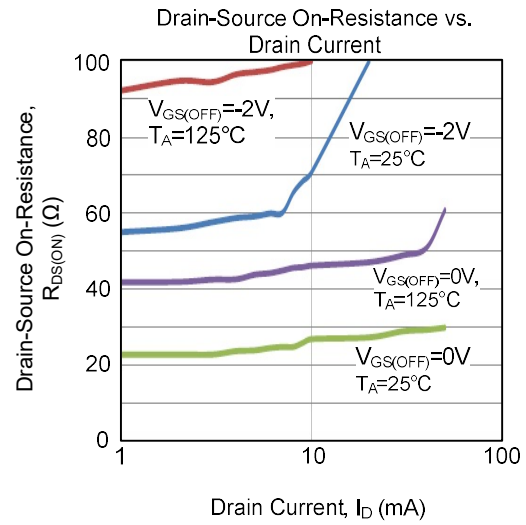
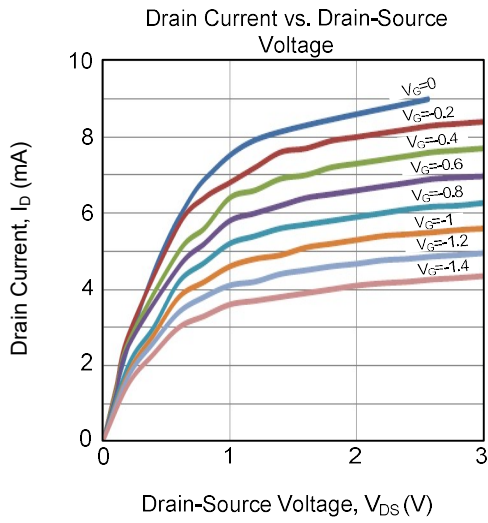
Note: Device mounted on FR-4 PCB 36mm × 18mm × 1.5mm, mounting pad for the collector lead minimum 6cm<sup>2</sup>.

■ **ELECTRICAL CHARACTERISTICS** ( $T_A=25^{\circ}\text{C}$ , unless otherwise specified)

| PARAMETER                           | SYMBOL        | TEST CONDITIONS   | MIN  | TYP | MAX  | UNIT     |
|-------------------------------------|---------------|---|------|-----|------|----------|
| <b>OFF CHARACTERISTICS</b>          |               |   |      |     |      |          |
| Gate-Source Breakdown Voltage       | $V_{(BR)GSS}$ | $I_G=-1.0\mu\text{A}$ , $V_{DS}=0$                        | -30  |     |      | V        |
| Gate Reverse Current (Note)         | $I_{GSS}$     | $V_{GS}=-15\text{V}$ , $V_{DS}=0$                         |      |     | -1.0 | nA       |
| Gate-Source Cut-Off Voltage         | $V_{GS(OFF)}$ | $V_{DS}=15\text{V}$ , $I_D=1.0\mu\text{A}$                | -0.5 |     | -3.0 | V        |
| Drain Cutoff Leakage Current        | $I_{D(OFF)}$  | $V_{DS}=5.0\text{V}$ , $V_{GS}=-10\text{V}$               |      |     | 1.0  | nA       |
| <b>ON CHARACTERISTICS</b>           |               |   |      |     |      |          |
| Zero-Gate Voltage Drain Current     | $I_{DSS}$     | $V_{DS}=15\text{V}$ , $V_{GS}=0$                          | 2.0  |     |      | mA       |
| Drain-Source On Resistance          | $R_{DS(ON)}$  | $V_{DS}\leq 0.1\text{V}$ , $V_{GS}=0$                     |      |     | 100  | $\Omega$ |
| <b>SMALL SIGNAL CHARACTERISTICS</b> |               |   |      |     |      |          |
| Drain-Gate On Capacitance           | $C_{DG(ON)}$  | $V_{DS}=0\text{V}$ , $V_{GS}=0\text{V}$ , $F=1\text{MHz}$ |      |     | 28   | pF       |
| Source-Gate On Capacitance          | $C_{SG(ON)}$  | $V_{DS}=0\text{V}$ , $V_{GS}=0\text{V}$ , $F=1\text{MHz}$ |      |     | 28   | pF       |

Note: Pulse test: pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .

■ TYPICAL CHARACTERISTICS



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