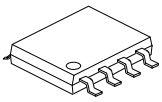
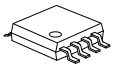
UCA9617 **CMOS IC**

LEVEL TRANSLATING FM+ I²C-BUS REPEATER



SOP-8



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■ DESCRIPTION

The **UCA9617** enables I²C-bus or SMBus translation down to V_{CC}(A) as low as 0.8V without degradation of system performance. The **UCA9617** contains two bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage (as low as 0.8V) and a 2.5V, 3.3V or 5V I²C-bus or SMBus. All inputs and I/Os are overvoltage tolerant to 5.5V even when the device is unpowered (V_{CC}(B) and/or V_{CC}(A)=0V). Using the **UCA9617** enables the system designer to isolate two halves of a bus for both voltage and capacitance. The SDA and SCL pins are overvoltage tolerant and are high-impedance when the **UCA9617** is unpowered.

The **UCA9617** includes a power-up circuit that keeps the output drivers turned off until V_{CC}(B) is above 2.2V and until after the internal reference circuits have settled ~ 400μs, and the V_{CC}(A) is above 0.8V. V_{CC}(B) and V_{CC}(A) can be applied in any sequence at power-up.

After power-up and with the enable (EN) HIGH, a LOW level on port A (below 0.3V_{CC}(A)) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to about 0.55V. When port A rises above 0.3V_{CC}(A), the port B pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When port B falls first and goes below 0.4V, the port A driver is turned on and port A pulls down to ~ 0V. The port A pull-down is not enabled unless the port B voltage goes below 0.4V.

If the port B low voltage goes below 0.4V, the port B pull-down driver is enabled and port B will onl y be able to rise to 0.55V until port A rises above 0.3V_{CC}(A), then port B will continue to rise being pulled up by the external pull-up resistor. The V_{CC}(A) is only used to provide the 0.35V_{CC}(A) reference to the port A input comparators and for the power good detect circuit. The **UCA9617** includes a V_{CC}(A) overvoltage disable that turns the channel off if 0.4V_{CC}(A)+0.8V>V_{CC}(B). The **UCA9617** logic and all I/Os are powered by the V_{CC}(B) pin.

■ FEATURES

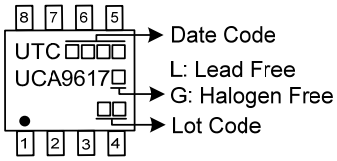
* Footprint and functional replacement for **UCA9617** at Fast-mode speeds
* 2 channel, bidirectional buffer isolates capacitance and allows 540pF on either side of the device at 1 MHz and up to 4000pF at lower speeds
* Voltage level translation from 0.8V to 5.5V and from 2.2V to 5.5V
* Port A operating supply voltage range of 0.8V to 5.5V with normal levels
* Port B operating supply voltage range of 2.2V to 5.5V with static offset level
* 5V tolerant I²C-bus and enable pins
* 0Hz to 1000kHz clock frequency (the maximum system operating frequency may be less than 1000kHz because of the delays added by the repeater)
* Active HIGH repeater enable input referenced to V_{CC}(B)
* Open-drain input/outputs
* Latching free operation
* Supports arbitration and clock stretching across the repeater
* Accommodates Standard-mode, Fast-mode and Fast-mode Plus I²C-bus devices, SMBus (standard and high power mode), PMBus and multiple masters
* Powered-off high-impedance I²C-bus pins

■ ORDERING INFORMATION

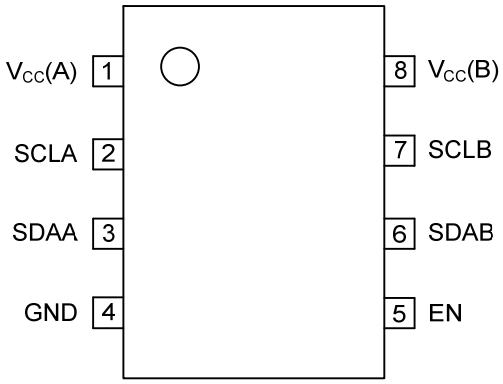
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCA9617L-S08-R	UCA9617G-S08-R	SOP-8	Tape Reel
UCA9617L-SM1-R	UCA9617G-SM1-R	MSOP-8	Tape Reel

UCA9617G-S08-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S08: SOP-8, SM1: MSOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO	PIN NAME	DESCRIPTION
1	V_{CC}(A)	port A supply voltage (0.8V to 5.5V)
2	SCLA	serial clock port A bus
3	SDAA	serial data port A bus
4	GND	supply ground (0V)
5	EN	active HIGH repeater enable input
6	SDAB	serial data port B bus
7	SCLB	serial clock port B bus
8	V_{CC}(B)	port B supply voltage (2.2V to 5.5V)

■ BLOCK DIAGRAM

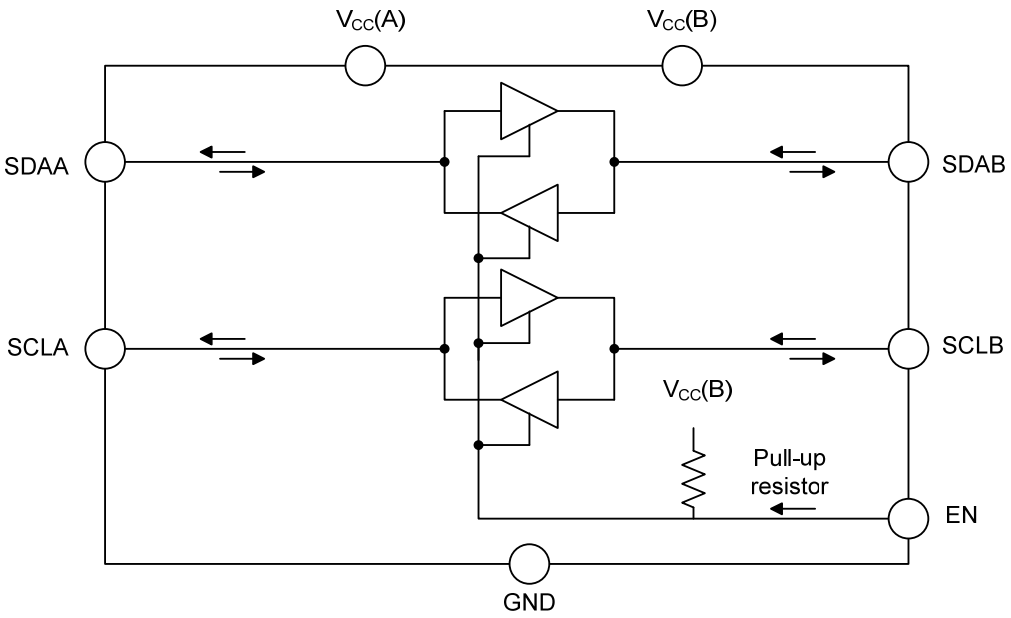


Figure 1 . Functional diagram

■ ABSOLUTE MAXIMUM RATING

PARAMETER	CONDITIONS	SYMBOL	RATINGS	UNIT
Supply Voltage Port B		$V_{CC}(B)$	-0.5 ~ 7	V
Supply Voltage Port A	Adjustable	$V_{CC}(A)$	-0.5 ~ 7	V
Voltage on an Input/output pin	Port A and Port B, Enable Pin (EN)	$V_{I/O}$	-0.5 ~ 7	V
Input/Output Current	Port A, port B	$I_{I/O}$	50	mA
Input Current	EN, $V_{CC}(A)$, $V_{CC}(B)$, GND	I_I	50	mA
Total Power Dissipation		P_D	100	mW
Ambient Temperature	operating in free air	T_A	-40 ~ +85	°C
Junction Temperature		T_J	+125	°C
Storage Temperature		T_{STG}	-55 ~ +125	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS

($V_{CC}(A)$=0.8V~5.5V(Note 1), $V_{CC}(B)$=2.2V~5.5V, GND=0V, T_A=40°C~+85°C unless otherwise specified)
(Typical values measured with $V_{CC}(A)$= 0.95V and $V_{CC}(B)$=2.5V at 25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLIES						
supply voltage port A	$V_{CC}(A)$	(Note 2)	0.8		$V_{CC}(B)$	V
supply voltage port B	$V_{CC}(B)$		2.2		5.5	V
supply current port A	$I_{CC}(A)$	$V_{CC}(A)$=0.95V			8	μA
		$V_{CC}(A)$=5.5V			50	uA
port B HIGH-level supply current	$I_{CCH}(B)$	$V_{CC}(B)$=5.5V, SDAn=SCLn=$V_{CC}(n)$		0.6	2.5	mA
port B LOW-level supply current	$I_{CCL}(B)$	$V_{CC}(B)$=5.5V, one SDA and one SCL=GND, other SDA and SCL open (with pull-up resistors)		0.5	2.9	mA
INPUT AND OUTPUT SDAA AND SCLA						
HIGH-level input voltage	V_{IH}		0.7× $V_{CC}(A)$		$V_{CC}(B)$	V
LOW-level input voltage	V_{IL}	(Note 5, 6)			0.2× $V_{CC}(A)$	V
input clamping voltage	V_{IK}	I_I=-18mA	-1.2		-0.3	V
input leakage current	I_{LI}	V_I=5.5V			±1	μA
LOW-level input current	I_{IL}	SDA, SCL, V_I=0.2V			10	μA
LOW-level output voltage	V_{OL}	I_{OL}=13mA, $V_{CC}(B)$=2.2V		0.1	0.2	V
input/output capacitance	C_{IO}	V_I= 3V or 0V, V_{CC}=3.3V, EN=LOW		7	10	pF
		V_I= 3V or 0V, V_{CC}=0V		7	10	pF
INPUT AND OUTPUT SDAB AND SCLB						
HIGH-level input voltage	V_{IH}		0.7× $V_{CC}(B)$		$V_{CC}(B)$	V
LOW-level input voltage	V_{IL}				0.3	V
input clamping voltage	V_{IK}	I_I=-18mA	-1.2		-0.3	V
input leakage current	I_{LI}	V_I=5.5V			±1	μA
LOW-level input current	I_{IL}	SDA, SCL,V_I=0.2V			10	μA
LOW-level output voltage	V_{OL}	I_{OL}=150uA at $V_{CC}(B)$=2.2V (Note 3)	0.4			V
		I_{OL}=13mA at $V_{CC}(B)$=2.2V (Note 4)		0.54	0.63	V
difference between LOW-level output and LOW-level input voltage	V_{OL-VIL}	V_{OL} at I_{OL}=1mA, guaranteed by design		90		mV
input/output capacitance	C_{IO}	V_I= 3V or 0V, $V_{CC}(B)$=3.3V, EN=LOW		7	10	pF
		VI= 3V or 0V, V_{CC}=0V		7	10	pF

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE						
LOW-level input voltage	V_{IL}				0.3× V_{CC}(B)	V
HIGH-level input voltage	V_{IH}		0.7× V_{CC}(B)		5.5	V
LOW-level input current on pin EN	$I_{IL(EN)}$	V_I=0.2V,EN, V_{CC}(B)=2.2V	-25	-4		μA
DYNAMIC CHARACTERISTICS						
LOW to HIGH propagation delay	t_{PLH}	Port B~Port A, Figure 4			-103	nS
LOW to HIGH propagation delay2	t_{PLH2}	Port B~Port A, Figure 4	67	94	130	nS
HIGH to LOW propagation delay	t_{PHL}	Port B~Port A, Figure 2	20	76	152	nS
LOW to HIGH output transition time	t_{TLH}	Port A, Figure 2		80		nS
falling slew rate	SRf	Port A, 0.7V_{CC}(A)~0.3V_{CC}(A)	0.022	0.037	0.14	v/nS
LOW to HIGH propagation delay	t_{PLH}	Port A~Port B, Figure 3	40	60	137	nS
HIGH to LOW propagation delay	t_{PHL}	Port A~Port B, Figure 3	20	80	173	nS
LOW to HIGH output transition time	t_{TLH}	Port B, Figure 3		80		nS
falling slew rate	SRf	Port B, 0.7V_{CC}(B)~0.3V_{CC}(B)	0.029	0.056	0.4	v/nS
enable time	t_{en}	Quiescent-0.3V, EN HIGH to enable, Figure 5			100	nS
disable time	t_{dis}	Quiescent+0.3V, EN LOW to disable, Figure 5			100	nS

Notes: 1. V_{CC}(A) may be as high as 5.5V for overvoltage tolerance but 0.4V_{CC}(A)+0.8V ≤ V_{CC}(B) for the channels to be enabled and functional normally.
2. For part to function, 0.4V_{CC}(A) must be equal or less than V_{CC}(B) - 0.8V. The voltage on the A port can still be up to 5.5V without damage to the pins.
3. Pull-up should result in I_{OL}≥150μA.
4. Guaranteed by design and characterization.
5. V_{IL} for port A with envelope noise must be below 0.3V_{CC}(A) for stable performance.
6. When V_{CC}(A) is less than 1V, care is required to make certain that the system ground offset and noise are minimized such that there is reasonable difference between the V_{IL} present at the **UCA9617** A-side input and the 0.25V_{CC}(A) input threshold.
7. Power supply decoupling capacitors need to be present for both V_{CC}(A) and V_{CC}(B) and the 0.1uF decoupling for V_{CC}(B) needs to be located near the V_{CC}(B) pin.

■ AC WAVEFORMS

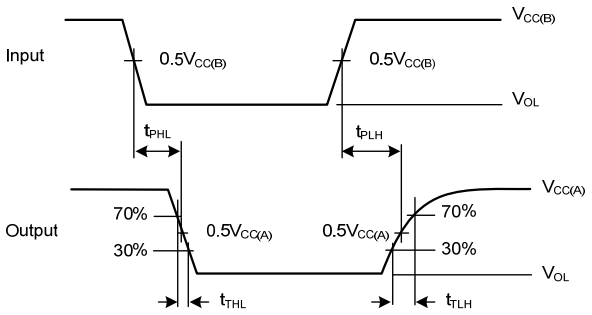


Figure 2. Propagation delay and transition times, port B to port A

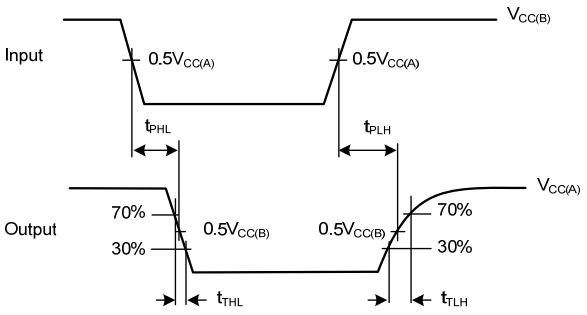


Figure 3. Propagation delay and transition times, port A to port B

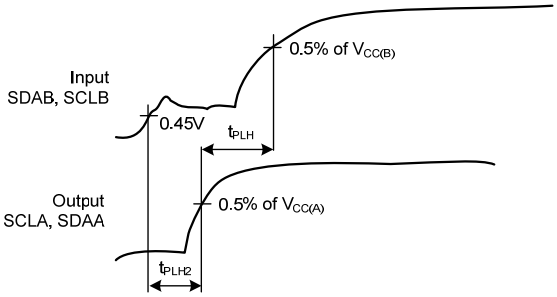


Figure 4. Propagation delay

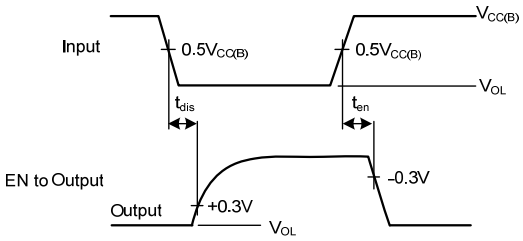
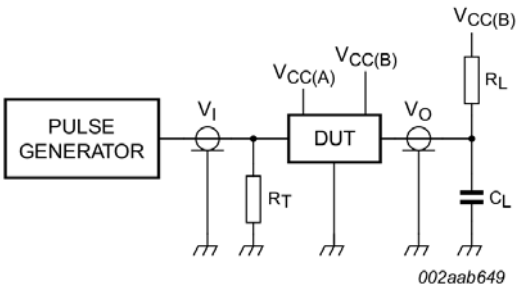


Figure 5. Enable and disable times

■ TEST INFORMATION



R_L = load resistor; 1.35 kΩ on port A and port B.
C_L = load capacitance includes jig and probe capacitance; 50 pF
R_T = termination resistance should be equal to Z_o of pulse generators

Figure 6. Test circuit for open-drain outputs

■ APPLICATION INFORMATION

The **UCA9617** enables I^2C-bus or SMBus translation down to V_{CC}(A) as low as 0.8V without degradation of system performance. The **UCA9617** contains two bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage (as low as 0.8V) and a 2.5V, 3.3V or 5V I^2C-bus or SMBus. All inputs and I/Os are overvoltage tolerant to 5.5V even when the device is unpowered (V_{CC}(B) and/or V_{CC}(A)=0V).

The 2.2V to 5.5V bus port B drivers have the static level offset, while the adjustable voltage bus port A drivers eliminate the static offset voltage. This results in a LOW on the port B translating into a nearly 0V LOW on the port A which accommodates the smaller voltage swings of lower voltage logic.

The static offset design of the port B **UCA9617** I/O drivers prevents them from being connected to the static or incremented offset of other bus buffers. Port A of two or more **UCA9617**s can be connected together, however , to allow a star topography with port A on the common bus, and port A can be connected directly to any other buffer with static or incremented offset outputs. Multiple **UCA9617**s can be connected in series, port A to port B, with no build-up in offset voltage with only time of flight delays to consider.

The **UCA9617** drivers are not enabled unless V_{CC}(A) is above 0.8V and V_{CC}(B) is above 2.2V. The EN pin is referenced to V_{CC}(B) and can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the enable pin when the bus is idle.

The output pull-down on the port B internal buffer LOW is set for approximately 0.55V, while the input threshold of the internal buffer is set about 90mV lower (0.45V). When the port B I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a latching condition from occurring. The output pull-down on port A drives a hard LOW and the input level is set at 0.35V_{CC}(A) to accommodate the need for a lower LOW level in systems where the low voltage side supply voltage is as low as 0.8V.

Enable

The EN pin is active HIGH with thresholds referenced to V_{CC}(B) and an internal pull-up to V_{CC}(B) that maintains the device active unless the user selects to disable the repeater to isolate a badly behaved slave on power-up until after the system power-up reset.

It should never change state during an I^2C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I^2C-bus parts being enabled.

The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

I^2C-bus systems

Pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I^2C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part designed to work with Standard mode, Fast-mode and Fast-mode Plus I^2C-bus devices in addition to SMBus devices. Standard mode and Fast-mode I^2C-bus devices only specify 3mA output drive; this limits the termination current to 3mA in a generic I^2C-bus system where Standard- mode devices, Fast-mode devices and multiple masters are possible. When only Fast-mode Plus devices are used with 30mA at 5V drive strength, then lower value pull-up resistors can be used.

■ TYPICAL APPLICATION CIRCUIT

The **UCA9617** is 5V tolerant, so it does not require any additional circuitry to translate between 0.8V to 5.5V bus voltages and 2.2V to 5.5V bus voltages. A typical application is shown in Figure 7. In this example, the system master is running on a 3.3V I^2C-bus while the slave is connected to a 1.2V bus. Both buses run at 1000kHz. Master devices ca n be placed on either bus.

When port A of the **UCA9617** is pulled LOW by a driver on the I^2C-bus, a comparator detects the falling edge when it goes below $0.3V_{CC}(A)$ and causes the internal driver on port B to turn on, causing port B to pull down to about 0.5V. When port B of the **UCA9617** falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on port A to turn on and pull the port A pin down to ground.

The $V_{CC}(A)$ is only used to provide the $0.35V_{CC}(A)$ reference to the port A input comparators and for the power good detect circuit. The **UCA9617** includes a $V_{CC}(A)$ overvoltage disable that turns the channel off if $0.4V_{CC}(A)+0.8V>V_{CC}(B)$. The **UCA9617** logic and all I/Os are powered by the $V_{CC}(B)$ pin.

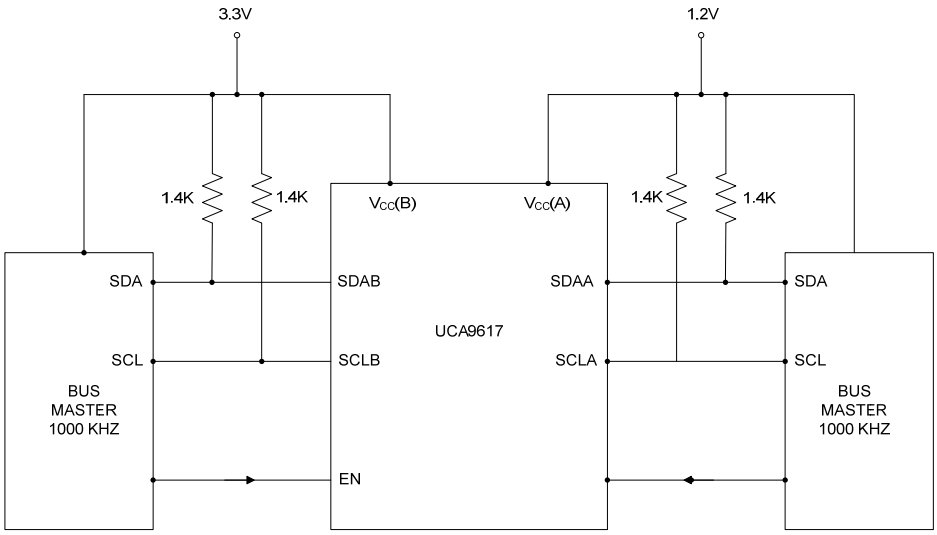


Figure 7. Typical application