



UD12N04Z

Preliminary

Power MOSFET

6.0A, 40V DUAL N-CHANNEL ENHANCEMENT MODE TRENCH POWER MOSFET

■ DESCRIPTION

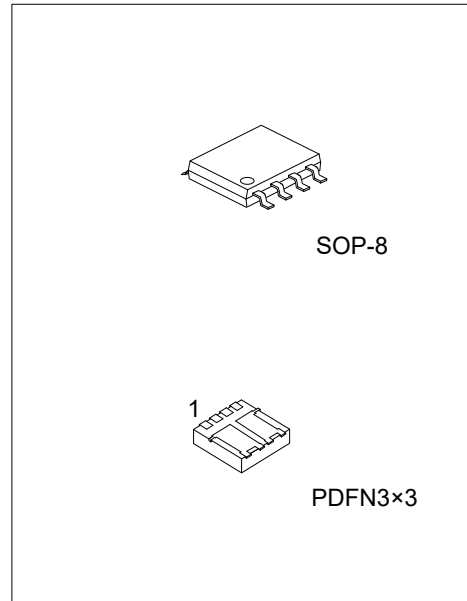
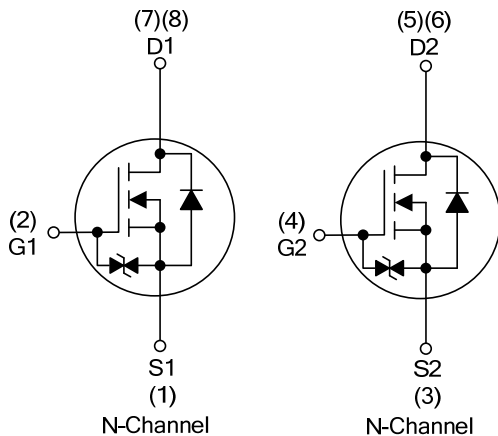
The UTC **UD12N04Z** is a Dual N-channel enhancement mode power MOSFET using UTC's advanced technology to provide customers with an extremely low on-state resistance and superior switching performance.

The UTC **UD12N04Z** is suitable for high frequency DC-DC converters with synchronous rectification applications.

■ FEATURES

- * $R_{DS(ON)} \leq 38 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=6.0\text{A}$
 $R_{DS(ON)} \leq 54 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=6.0\text{A}$
- * High Power and Current Handling Capability
- * High Cell Density Trench Technology
- * With ESD Protected

■ SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UD12N04ZL-S08-R	UD12N04ZG-S08-R	SOP-8	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel
UD12N04ZL-P3030-R	UD12N04ZG-P3030-R	PDFN3×3	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UD12N04ZG-S08-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) S08: SOP-8, P3030: PDFN3×3</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING

SOP-8	PDFN3×3
<p>UTC □□□□ → Date Code</p> <p>L: Lead Free</p> <p>G: Halogen Free</p> <p>□□□□ → Lot Code</p>	<p>UD</p> <p>12N04Z</p> <p>• □□□□ → Date Code</p>

■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	40	V
Gate-Source Voltage		V_{GSS}	± 12	V
Drain Current	Continuous	I_D	6	A
	Pulsed (Note 2)	I_{DM}	12	A
Avalanche Energy	Single Pulsed (Note 4)	E_{AS}	11	mJ
Peak Diode Recovery dv/dt (Note 5)		dv/dt	2.1	V/ns
Power Dissipation	SOP-8	P_D	1.08	W
	PDFN3×3		19	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. Mounted on a ceramic board.

4. $L = 0.01\text{mH}$, $I_{AS} = 46.9\text{A}$, $V_{DD} = 20\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.

5. $I_{SD} \leq 12\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-8	θ_{JA}	125	$^\circ\text{C}/\text{W}$
	PDFN3×3		60	$^\circ\text{C}/\text{W}$
Junction to Case	SOP-8	θ_{JC}	115	$^\circ\text{C}/\text{W}$
	PDFN3×3		6.58	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

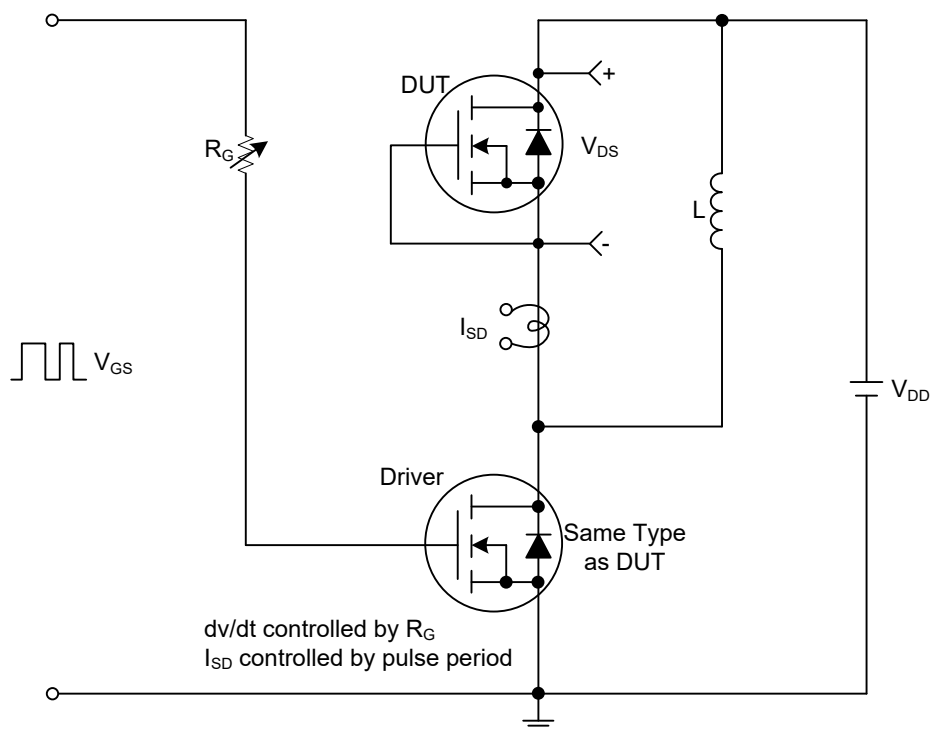
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	40			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =40V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+12V, V _{DS} =0V			+10	μA
	Reverse		V _{GS} =-12V, V _{DS} =0V			-10	μA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		2.5	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =6.0A			38	mΩ
			V _{GS} =4.5V, I _D =6.0A			54	mΩ
DYNAMIC CHARACTERISTICS							
Input Capacitance		C _{ISS}	V _{DS} =10V, V _{GS} =0V, f=1.0MHz		401		pF
Output Capacitance		C _{OSS}			72		pF
Reverse Transfer Capacitance		C _{RSS}			62		pF
SWITCHING CHARACTERISTICS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =32V, V _{GS} =10V, I _D =12A (Note 1, 2)		17		nC
Gate-Source Charge		Q _{GS}			3		nC
Gate-Drain Charge		Q _{GD}			5		nC
Turn-on Delay Time (Note 1)		t _{D(ON)}	V _{DD} =20V, V _{GS} =10V, I _D =12A, R _G =3.0Ω (Note 1, 2)		2		ns
Rise Time		t _R			17		ns
Turn-off Delay Time		t _{D(OFF)}			18		ns
Fall-Time		t _F			20		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				12	A
Maximum Body-Diode Pulsed Current		I _{SM}				24	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =6.0A, V _{GS} =0V			1.4	V
Reverse Recovery Time (Note 1)		t _{rr}	I _S =12A, V _{GS} =0V		21		ns
Reverse Recovery Charge		Q _{rr}	dl _F /dt=100A/μs (Note1)		8		nC

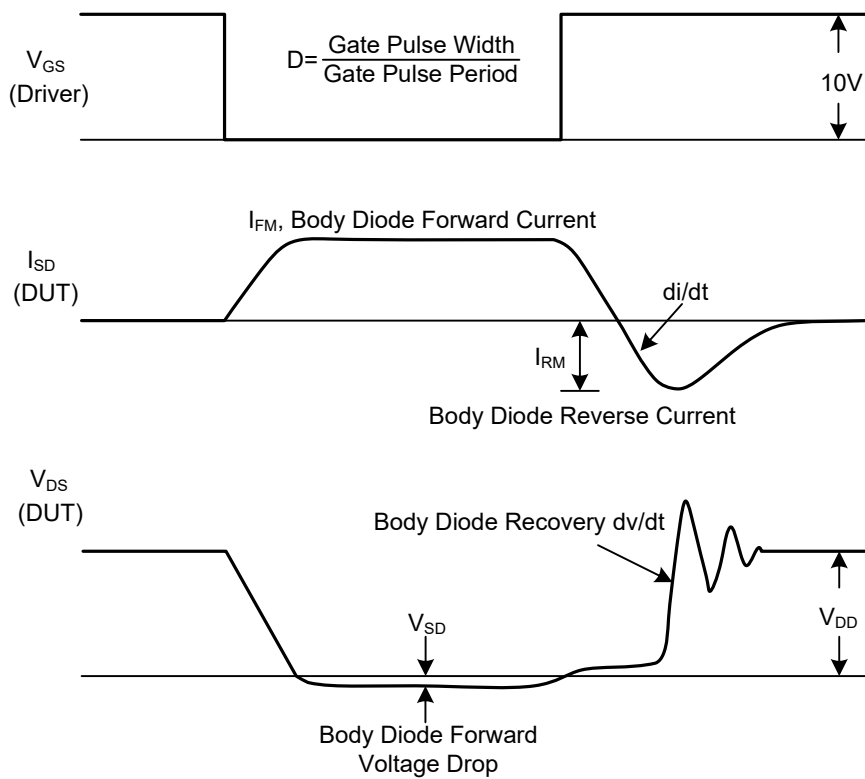
Notes: 1. Pulse Test: Pulse width $\leq 10\mu\text{s}$, Duty cycle $\leq 1\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



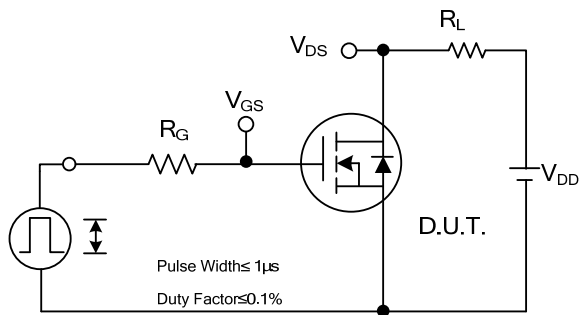
Peak Diode Recovery dv/dt Test Circuit



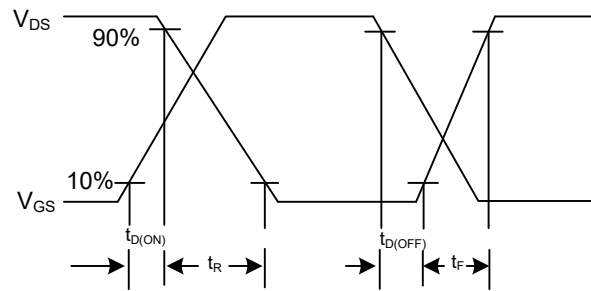
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

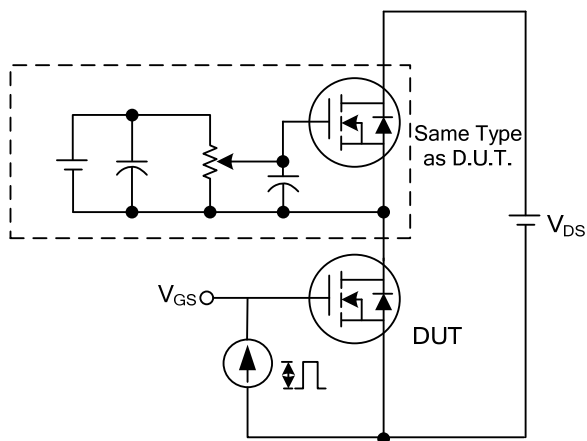
■ TEST CIRCUITS AND WAVEFORMS



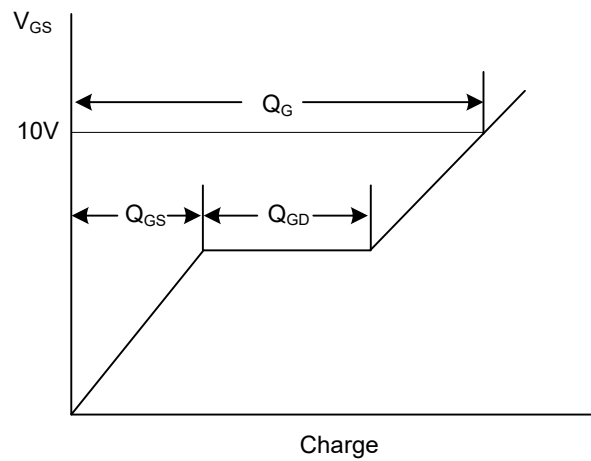
Switching Test Circuit



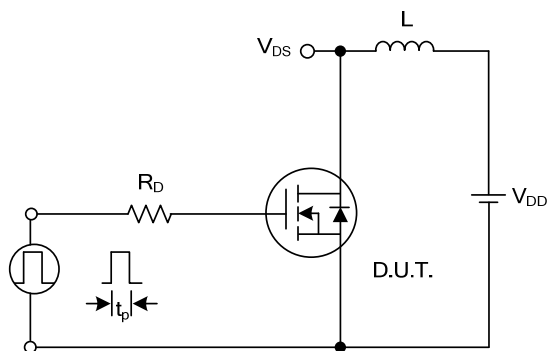
Switching Waveforms



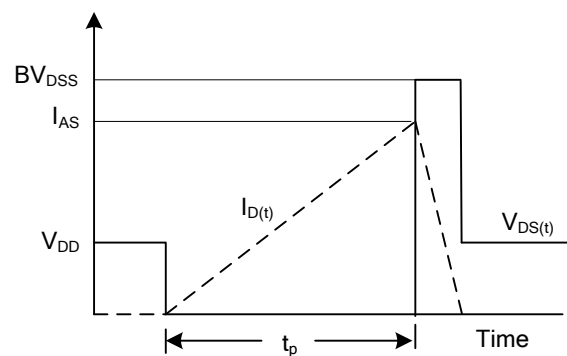
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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