

**UT20NP06**

Preliminary

Power MOSFET**DUAL ENHANCEMENT MODE
(N-CHANNEL / P-CHANNEL)****DESCRIPTION**

The UTC **UT20NP06** incorporates a N-channel MOSFET and a P-channel MOSFET, it uses UTC's advanced technology to provide customers a minimum on-state resistance, high switching speed, low gate charge and cost effectiveness.

The UTC **UT20NP06** is universally applied in low voltage applications.

FEATURES***N-CHANNEL**

$$R_{DS(on)} \leq 30 \text{ m}\Omega @ V_{GS}=10\text{V}, I_D=10\text{A}$$

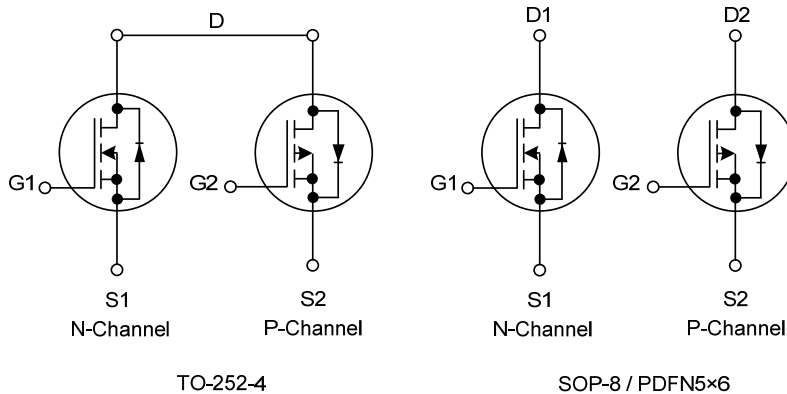
$$R_{DS(on)} \leq 46 \text{ m}\Omega @ V_{GS}=4.5\text{V}, I_D=10\text{A}$$

***P-CHANNEL**

$$R_{DS(on)} \leq 63 \text{ m}\Omega @ V_{GS}=-10\text{V}, I_D=-10\text{A}$$

$$R_{DS(on)} \leq 76 \text{ m}\Omega @ V_{GS}=-4.5\text{V}, I_D=-10\text{A}$$

* High switching speed

SYMBOL**ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT20NP06L-TN4-R	UT20NP06G-TN4-R	TO-252-4	S1	G1	D	S2	G2	-	-	-	Tape Reel
UT20NP06L-S08-R	UT20NP06G-S08-R	SOP-8	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel
UT20NP06L-P5060-R	UT20NP06G-P5060-R	PDFN5x6	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT20NP06G-TN4-R 		(1) R: Tape Reel (2) TN4: TO-252-4, S08: SOP-8, P5060: PDFN5x6 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING

PACKAGE	MARKING
TO-252-4	UTC UT20NP06 Lot Code → [][][][][][] → Date Code 1 L: Lead Free G: Halogen Free
SOP-8	[][][][][][] → Date Code UTC UT20NP06 Lot Code → [][][][][][] L: Lead Free G: Halogen Free
PDFN5x6	UTC UT 20NP06 Lot Code → [][][][][][] → Date Code

■ **ABSOLUTE MAXIMUM RATINGS** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER			SYMBOL	RATINGS		UNIT
				N-CH	P-CH	
Drain-Source Voltage			V _{DSS}	60	-60	V
Gate-Source Voltage			V _{GSS}	±20	±20	V
Drain Current	Continuous	T _C =25°C	I _D	10	-10	A
	Pulsed		I _{DM}	20	-20	A
Avalanche Energy, Single Pulse			E _{AS}	34	34	mJ
Power Dissipation		TO-252-4	P _D	42		W
		SOP-8		2.5		W
		PDFN5x6		38		W
Junction Temperature			T _J	+150		°C
Range of Storage Temperature			T _{STG}	-55 ~ +150		°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3. N-Channel: $L=0.1\text{mH}$, $I_{\text{AS}}=26\text{A}$, $V_{\text{DD}}=50\text{V}$, $R_{\text{G}}=25\Omega$, Starting $T_{\text{J}}=25^{\circ}\text{C}$

P-Channel: $L=0.1\text{mH}$, $I_{\text{AS}}=-26\text{A}$, $V_{\text{DD}}=-50\text{V}$, $R_{\text{G}}=25\Omega$, Starting $T_{\text{J}}=25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-252-4	θ_{JA}	110	$^{\circ}\text{C/W}$
	SOP-8		125	$^{\circ}\text{C/W}$
	PDFN5x6		35	$^{\circ}\text{C/W}$
Junction to Case	TO-252-4	θ_{JC}	3 (Note)	$^{\circ}\text{C/W}$
	SOP-8		50 (Note)	$^{\circ}\text{C/W}$
	PDFN5x6		3.28(Note)	$^{\circ}\text{C/W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

N-Channel

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	60			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =60V, V _{GS} =0V, T _J =25°C			1	μA
			V _{DS} =48V, V _{GS} =0V, T _J =125°C			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V			+100	nA
	Reverse		V _{GS} =-20V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance (Note)		R _{DS(ON)}	V _{GS} =10V, I _D =10A			30	mΩ
			V _{GS} =4.5V, I _D =10A			46	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		1400		pF
Output Capacitance		C _{OSS}			110		pF
Reverse Transfer Capacitance		C _{RSS}			84		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note)		Q _G	V _{GS} =48V, V _{DS} =10V, I _D =10A		40		nC
Gate to Source Charge		Q _{GS}			6.2		nC
Gate to Drain Charge		Q _{GD}			8.5		nC
Turn-ON Delay Time (Note)		t _{D(ON)}	V _{DD} =30V, V _{GS} =10V, I _D =10A, R _G =25Ω		7		ns
Rise Time		t _R			18		ns
Turn-OFF Delay Time		t _{D(OFF)}			28		ns
Fall-Time		t _F			20		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I _S				10	A
Maximum Pulsed Drain-Source Diode Forward Current		I _{SM}				20	A
Drain-Source Diode Forward Voltage (Note)		V _{SD}	I _S =10A, V _{GS} =0V			1.2	V

■ ELECTRICAL CHARACTERISTICS (Cont.)

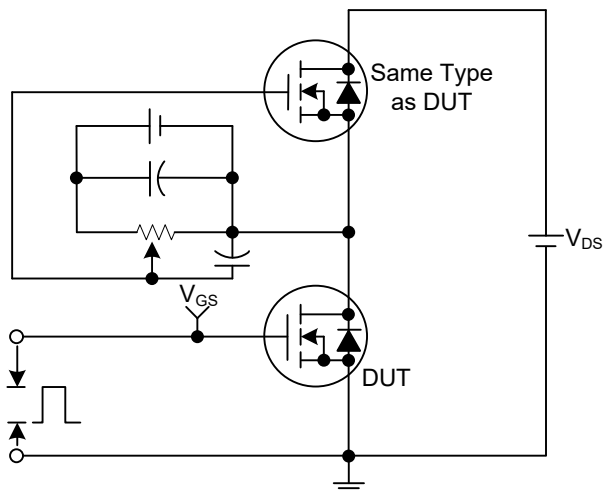
P-Channel

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =-250μA, V _{GS} =0V	-60			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =-60V, V _{GS} =0V, T _J =25°C			-1	μA
			V _{DS} =-48V, V _{GS} =0V, T _J =125°C			-10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V			+100	nA
	Reverse		V _{GS} =-20V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0		-3.0	V
Static Drain-Source On-State Resistance (Note)		R _{DS(ON)}	V _{GS} =-10V, I _D =-10A			63	mΩ
			V _{GS} =-4.5V, I _D =-10A			76	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =-25V, f=1.0MHz		1450		pF
Output Capacitance		C _{OSS}			110		pF
Reverse Transfer Capacitance		C _{RSS}			84		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note)		Q _G	V _{GS} =-48V, V _{DS} =-10V, I _D =-10A		32		nC
Gate to Source Charge		Q _{GS}			8		nC
Gate to Drain Charge		Q _{GD}			7.5		nC
Turn-ON Delay Time (Note)		t _{D(ON)}	V _{DD} =-30V, V _{GS} =-10V, I _D =-10A, R _G =3Ω		7		ns
Rise Time		t _R			17		ns
Turn-OFF Delay Time		t _{D(OFF)}			42		ns
Fall-Time		t _F			22		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I _S				-10	A
Maximum Pulsed Drain-Source Diode Forward Current		I _{SM}				-20	A
Drain-Source Diode Forward Voltage (Note)		V _{SD}	I _S =-1.0A, V _{GS} =0V			-1.2	V

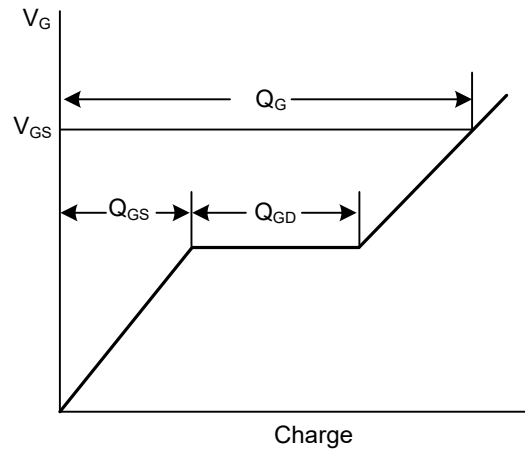
Note: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

■ TEST CIRCUITS AND WAVEFORMS

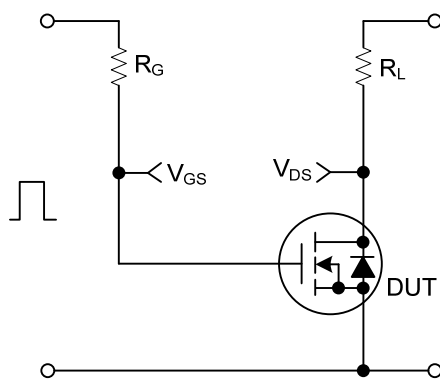
N-CHANNEL



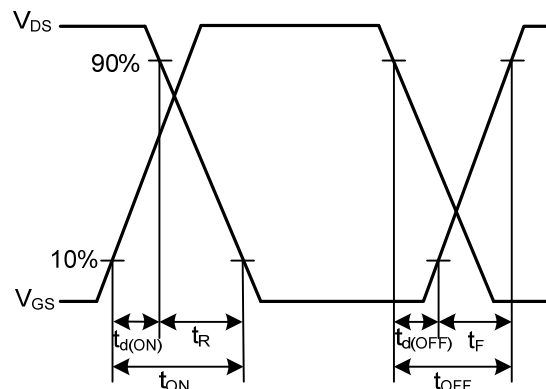
Gate Charge Test Circuit



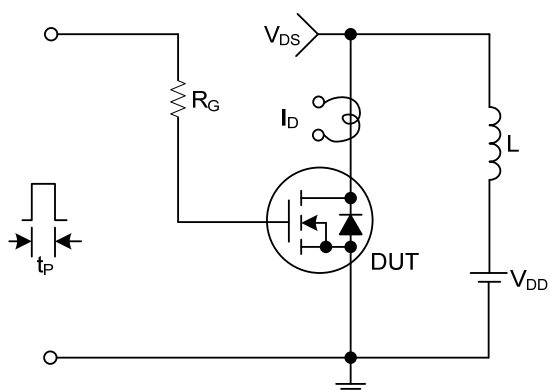
Gate Charge Waveforms



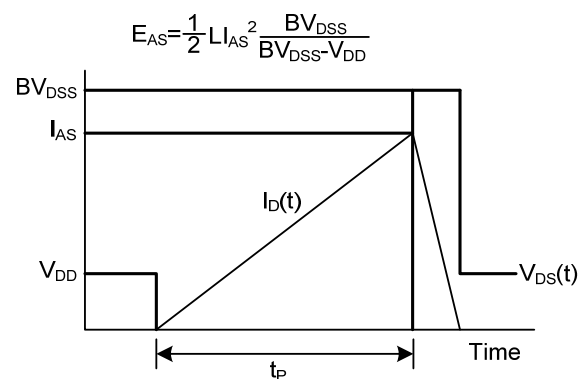
Resistive Switching Test Circuit



Resistive Switching Waveforms



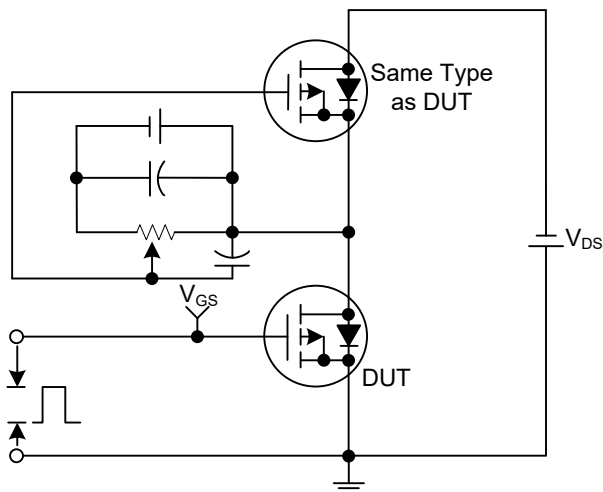
Unclamped Inductive Switching Test Circuit



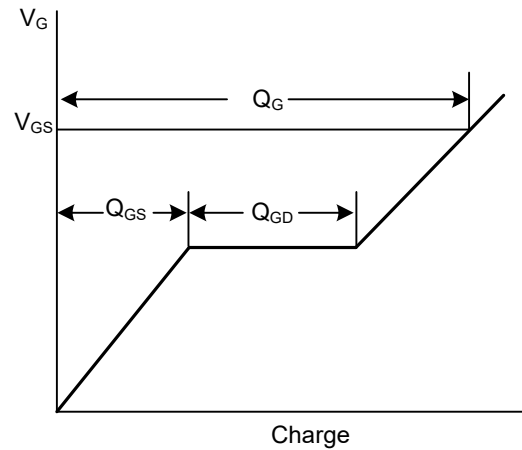
Unclamped Inductive Switching Waveforms

■ TEST CIRCUITS AND WAVEFORMS

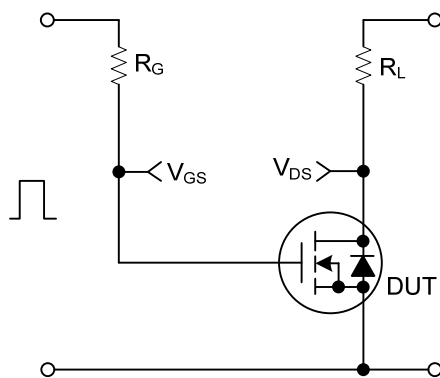
P-CHANNEL



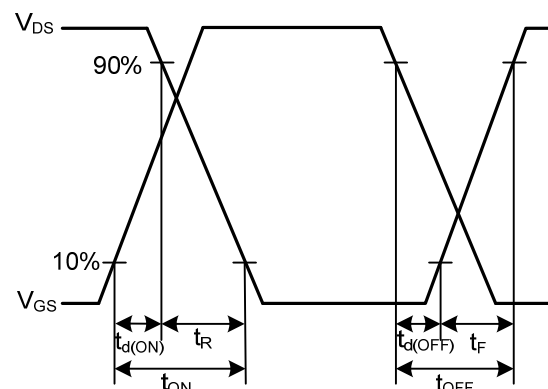
Gate Charge Test Circuit



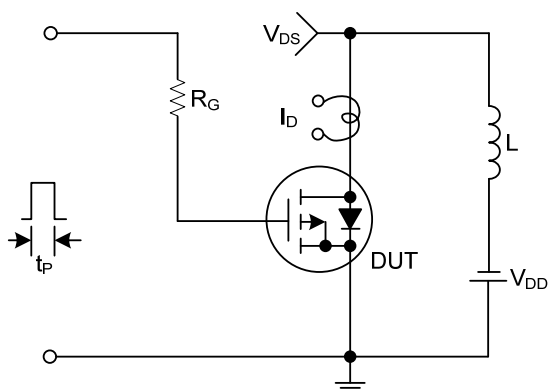
Gate Charge Waveforms



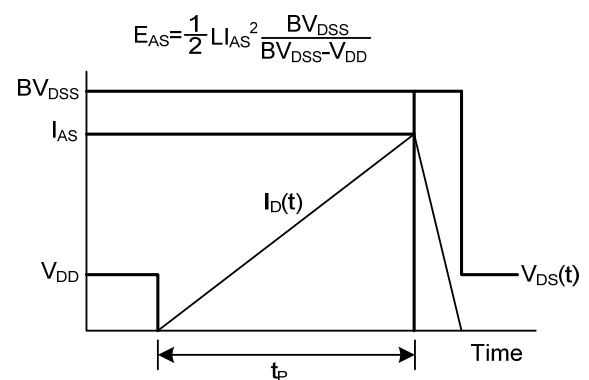
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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