



UC3943

LINEAR INTEGRATED CIRCUIT

HIGH PERFORMANCE CURRENT MODE CONTROLLERS

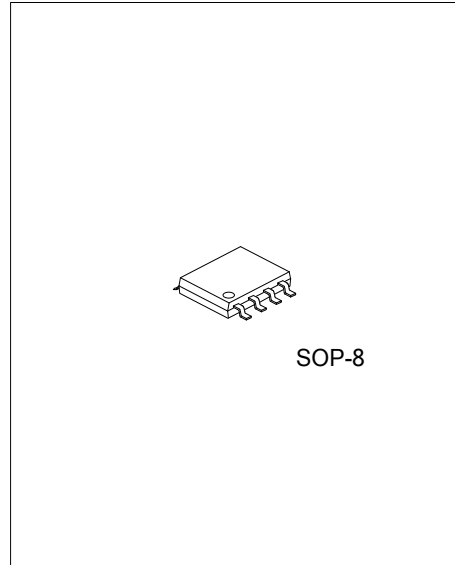
DESCRIPTION

The UTC **UC3943** is specifically designed for off-line and dc-to-dc converter applications offering the designer a cost-effective solution with minimal external components.

The UTC **UC3943** has UVLO thresholds 8.4V (on) and 7.6V(off), ideally suited for off-line converters.

FEATURES

- * With burstmode for lower standby power
- * With greenmode for higher light load efficiency
- * Oscillator frequency guaranteed at 250kHz
- * Automatic feed forward compensation
- * Latching PWM for cycle-by-cycle current limiting
- * Internally trimmed reference with undervoltage lockout
- * High current totem pole output
- * Undervoltage lockout with hysteresis
- * Low startup and operating current



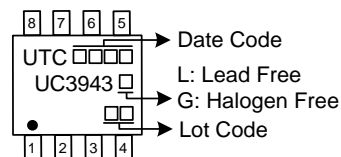
SOP-8

ORDERING INFORMATION

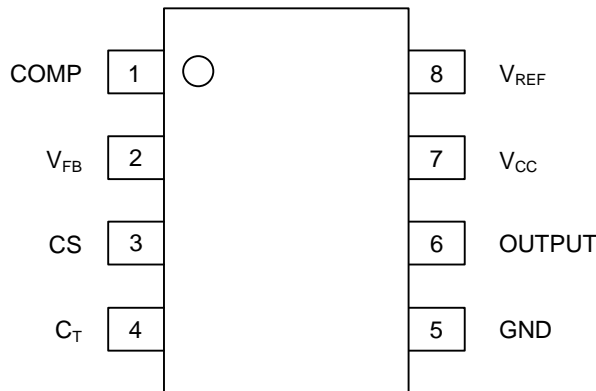
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UC3943L-S08-R	UC3943G-S08-R	SOP-8	Tape Reel

<p>UC3943G-S08-R</p> <ul style="list-style-type: none"> (1) Packing Type (2) Package Type (3) Green Package 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING



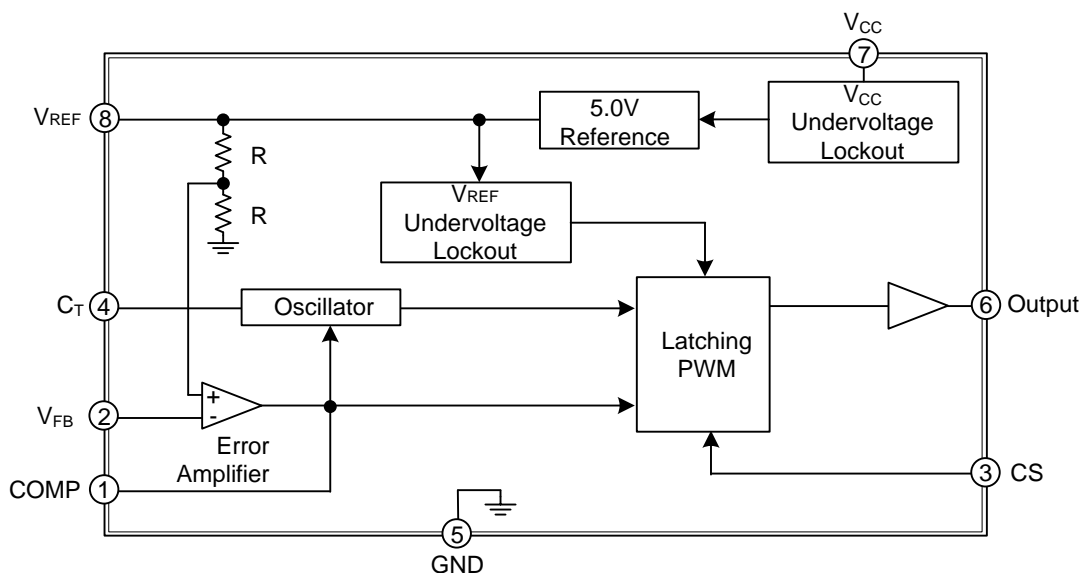
■ PIN CONFIGURATION



■ PIN DESCRIPTIONS

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	COMP	O	Error amp output to provide loop compensation maintaing V_{FB} at 2.5V
2	V_{FB}	I	Error amp inverting input, The non-inverting input of error amp is 2.5V band gap reference
3	CS	I	Current sense input to PWM control gate drive of output
4	C_T	I	To set oscillator frequency
5	GND		Power ground
6	OUTPUT	O	To direct drive power MOSFET
7	V_{CC}		Power supply
8	V_{REF}	O	5V regulated output

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Total Power Supply and Zener Current	(I _{CC} + I _Z)	30	mA
Output Current, Source or Sink (Note 2)	I _O	1.0	A
Output Energy (capacitive load per cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V _{IN}	-0.3 ~ +5.5	V
Error Amp. Output Sink Current	I _{O(SINK)}	10	mA
Power Dissipation	P _D	800	mW
Operating Junction Temperature	T _J	+150	°C
Operating Temperature	T _{OPR}	-40 ~ +125	°C
Storage Temperature	T _{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Maximum Package power dissipation limits must be observed.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ _{JA}	156	°C/W

■ ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C, V_{CC}=15V (Note 1), C_T=4.7nF, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE SECTION						
Output Voltage	V _{REF}	I _O =1.0mA, T _J =25°C	4.9	5.0	5.1	V
Line Regulation	ΔV _{LINE}	V _{CC} =12V ~ 25V		2.0	20	mV
Load Regulation	ΔV _{LOAD}	I _O =1.0mA ~ 20mA		15	35	mV
Temperature Stability	T _S			0.2		mV/°C
Total Output Variation	V _{REF}	Line, Load, Temperature	4.82		5.18	V
Output Noise Voltage	e _N	F=10kHz ~ 10Hz, T _J =25°C		50		μV
Long Term Stability	S	T _A =125°C, 1000Hrs		5		mV
Output Short Circuit Current	I _{SC}		-40	-145	-245	mA
OSCILLATOR SECTION						
Frequency	F	T _J =25°C	65	70	75	kHz
		T _A =0°C ~ 70°C	64		76	
Standby Frequency	F _B	T _J =25°C	21			
		T _A =0°C ~ 70°C	20			
Frequency Change with Voltage	Δf _{OSC} /ΔV	12 ≤ V _{CC} ≤ 25V		0.2	1.0	%
Frequency Change with Temperature	Δf _{OSC} /ΔT	0°C ≤ T _A ≤ 70°C		0.5		%
Oscillator Voltage Swing (Peak to Peak)	V _{OSC}			1.6		V
Discharge Current	I _{DISCHG}	T _J =25°C	7.8	8.3	8.8	mA
		0°C ≤ T _A ≤ 70°C	7.6	8.3	8.8	

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER SECTION						
Voltage Feedback Input	V_{FB}	$V_O=2.5V$	2.42	2.50	2.58	V
Input Bias Current	$I_{I(BIAS)}$	$V_{FB}=5.0V$		-0.1	-2.0	μA
Open Loop Voltage Gain	G_{VO}	$2 \leq V_O \leq 4V$	65	90		dB
Unity Gain Bandwidth	GB_W	$T_J = 25^\circ C$	0.7	1.0		MHz
Power Supply Rejection Ratio	PSRR	$12V \leq V_{CC} \leq 25V$	60	70		dB
Output Sink Current	I_{SINK}	$V_O=1.6V, V_{FB}=2.7V$	2.0	12		mA
Output Source Current	I_{SOURCE}	$V_O=5.0V, V_{FB}=2.3V$	-0.5	-1.0		mA
Output Voltage Swing High State	V_{OH}	$V_{FB}=2.3V, R_L=15k \text{ to GND}$	5.0	6.2		V
Output Voltage Swing Low State	V_{OL}	$V_{FB}=2.7V, R_L=15k \text{ to } V_{REF}$		0.8	1.1	V
CURRENT SENSE SECTION						
Current Sense Input Voltage Gain	G_V	(Note 2, 3)	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold	$V_{I(THR)}$	(Note 2)	0.9	1.0	1.1	V
Power Supply Rejection Ratio	PSRR	$12 \leq V_{CC} \leq 25V$ (Note 2)		70		dB
Input Bias Current	$I_{I(BIAS)}$			-2	-10	μA
Propagation Delay	$t_{D(IN/OUT)}$	Current Sense Input to Output		150	300	ns
OUTPUT SECTION						
Output Low Voltage	V_{OL}	$I_{SINK}=20mA$		0.1	0.4	V
		$I_{SINK}=200mA$		1.6	2.2	V
Output High Voltage	V_{OH}	$I_{SOURCE}=20mA$	13	13.5		V
		$I_{SOURCE}=200mA$	12	13.4		V
Output Voltage with UVLO Activated	$V_{OL(UVLO)}$	$V_{CC}=6.0V, I_{SINK}=1.0mA$		0.1	1.1	V
Output Voltage Rise Time	t_R	$T_J = 25^\circ C, C_L=1nF$		50	150	ns
Output Voltage Fall Time	t_F	$T_J = 25^\circ C, C_L=1nF$		50	150	ns
UNDER-VOLTAGE LOCKOUT SECTION						
Startup Threshold	V_{THR}		7.8	8.4	9	V
Min. Operating Voltage After Turn-on(V_{CC})	$V_{CC(MIN)}$		7.0	7.6	8.2	V
PWM SECTION						
Duty Cycle	MAX	DC	94	96		%
	MIN				0	%
Total DEVICE						
Power Startup Supply Current	$I_{CC}+I_C$	$V_{THR} -0.05V$		0.25	0.5	mA
Power Operating Supply Current	$I_{CC}+I_C$	Note 1		12	17	mA
Power Supply Zener Voltage	V_Z	$I_{CC}=25mA$	30	36		V

Notes: 1. Adjust V_{CC} above the Startup threshold before setting to 15V.

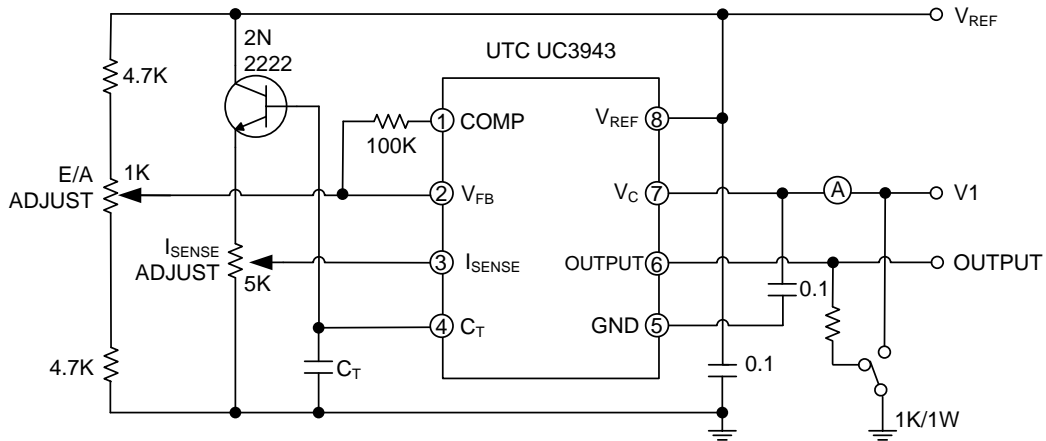
2. This parameter is measured at the latch trip point with $V_{FB}=0V$.

3. Comparator gain is defined as : $G_V = \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$

■ TYPICAL APPLICATION CIRCUIT

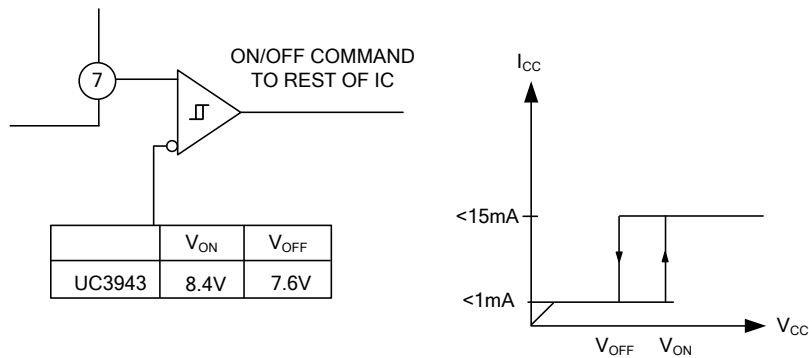
Open Loop Test Circuit

All of the parameters are not all tested in production, although been guaranteed. The timing and bypass capacitors must be connected to Pin 5 in a single point ground very closely. To sample the oscillator waveform, the transistor and 5kΩ potentiometer are used, and also can apply an adjustable ramp to I_{SENSE} Pin.

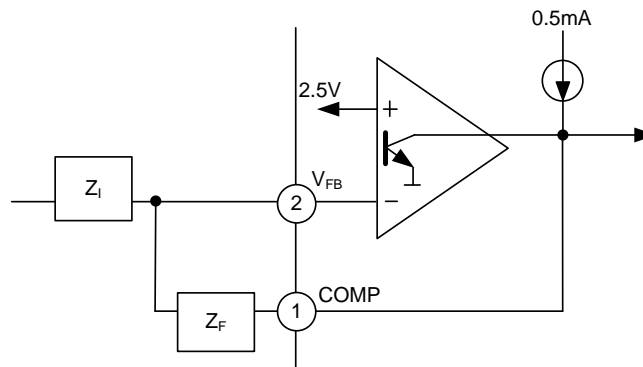


Under Voltage Lockout

Under-Voltage Lock-Out: the output driver is biased to a high impedance state. To prevent activating the power switch with output leakage current, Pin 6 should be shunted to ground with a bleeder resistor.



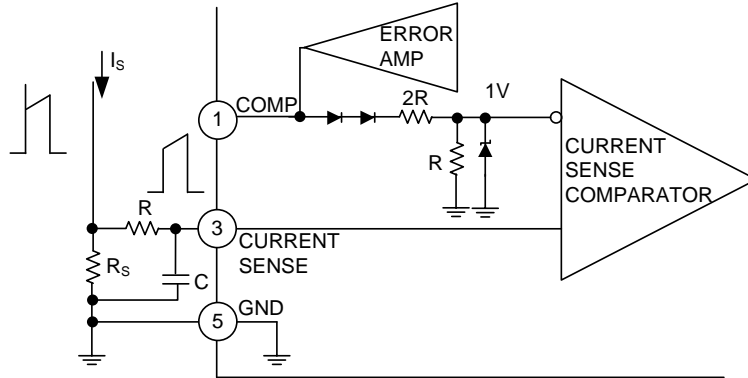
Error Amp Configuration



Error amp can source sink up to 0.5mA

■ APPLICATION INFORMATION

Current Sense Circuit

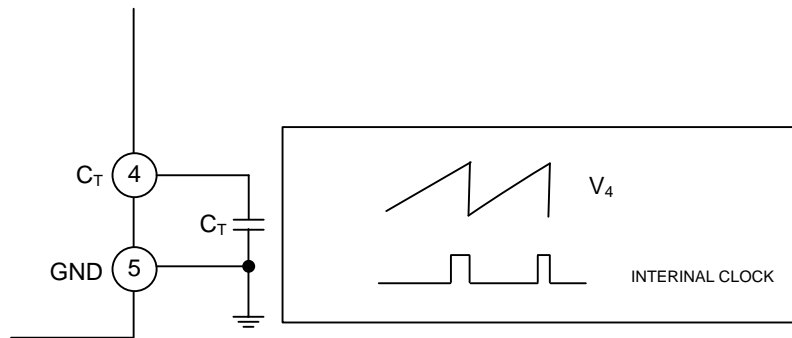


Peak current (I_s) is equaled:

$$I_{S(MAX)} = 1.0V/R_S$$

There should be a small RC filter to suppress switch transients.

Oscillator Waveforms and Maximum Duty Cycle

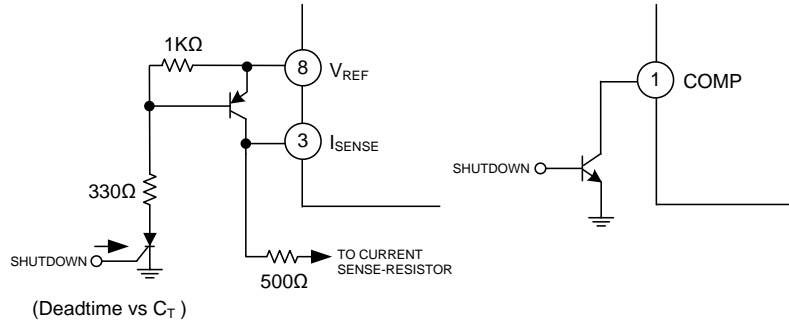


C_T (Oscillator timing capacitor) can be charged and discharged by an internal current source. At discharge time, the internal clock signal blanks the output to the low. Both oscillator frequency and maximum duty cycle can be determined by Selection of C_T . All charge and discharge times can be calculated by the next formulas:

$$f_{osc} = 0.329 / (1000C_T)$$

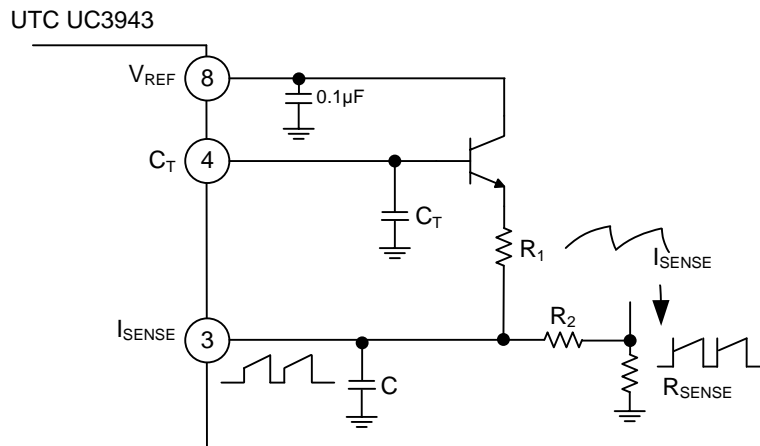
APPLICATION INFORMATION (Cont.)

Shutdown Techniques



The UTC **UC3943's** shutdown can be accomplished by two ways: raise Pin 3 above 1V; or pull Pin 1 below a voltage two diode drops above ground. Either method can cause the PWM comparator's output to be high. Because the PWM latch is reset dominant, the output will remain low until the next clock cycle after the shutdown condition at Pins 1 and/or 3 is removed.

Slope Compensation



TYPICAL CHARACTERISTICS

Fig. 1 Timing Capacitor vs. Oscillator Frequency

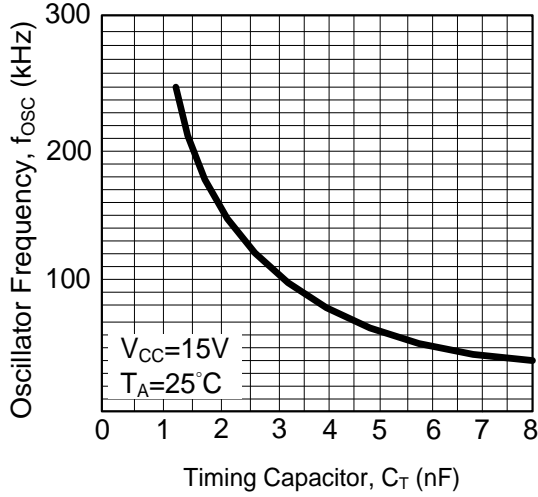


Fig. 2 Output Deadtime vs. Oscillator Frequency

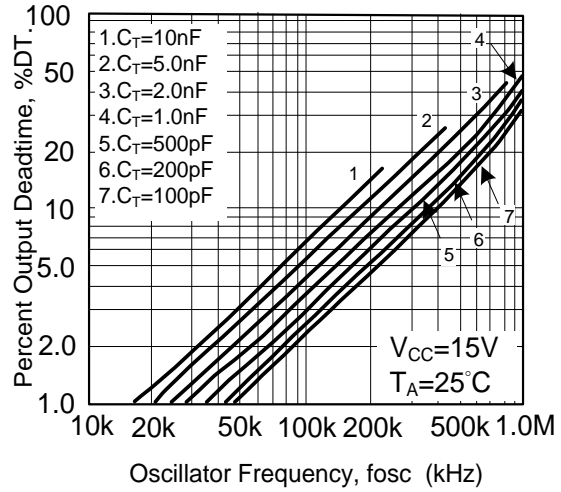


Fig. 3 Error Amp Large Signal Transient Response

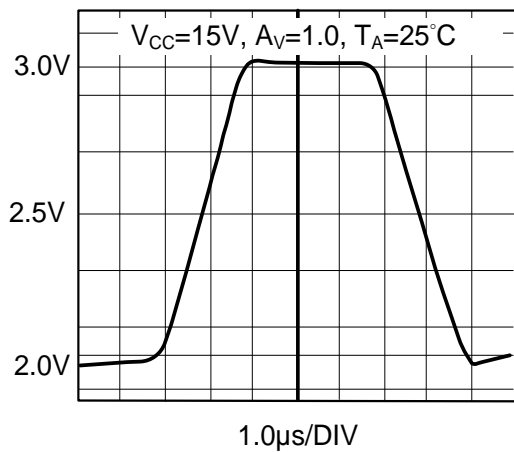


Fig. 4 Error Amp Small Signal Transient Response

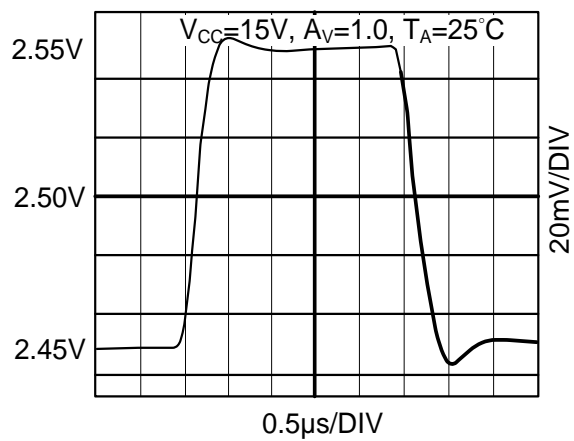


Fig. 5 Error Amp Open Loop Gain Phase vs. Frequency

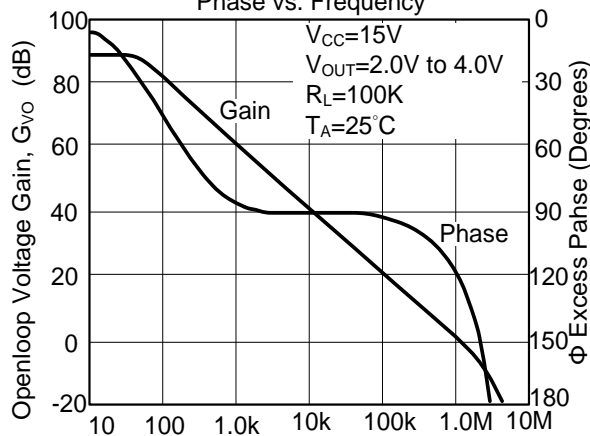
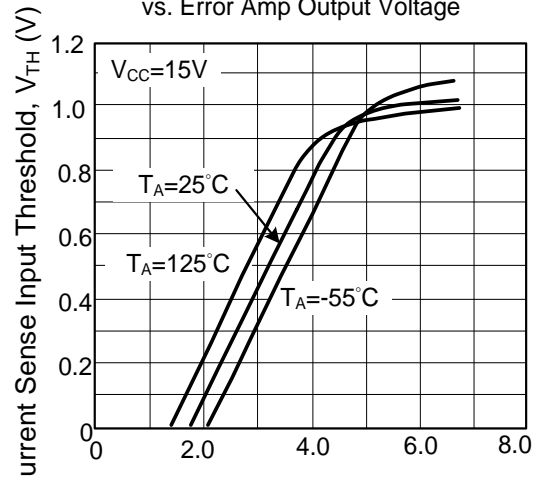


Fig. 6 Current Sense Input Threshold vs. Error Amp Output Voltage



■ TYPICAL CHARACTERISTICS (Cont.)

Fig. 7 Reference Voltage Change vs. Source Current

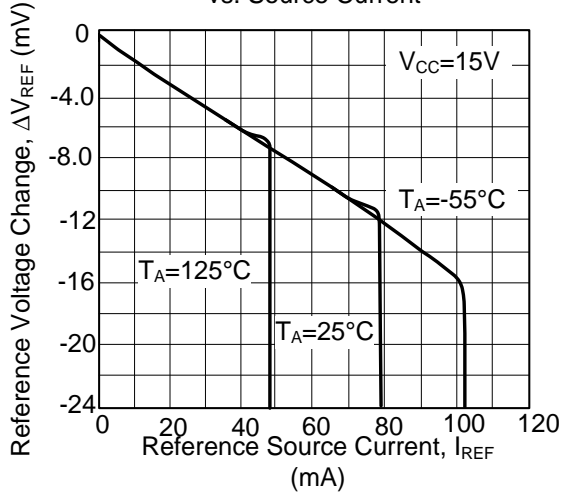


Fig. 8 Supply Current vs. Supply Voltage

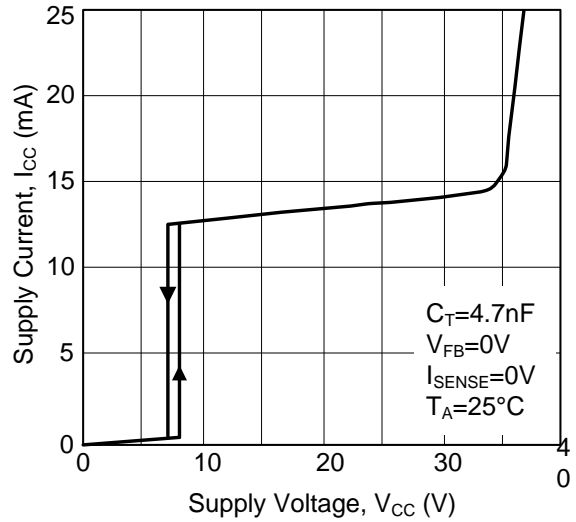


Fig. 9 Reference Load Regulation

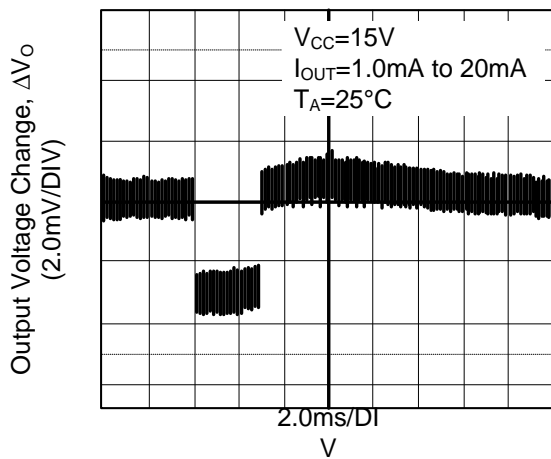


Fig. 10 Reference Line Regulation

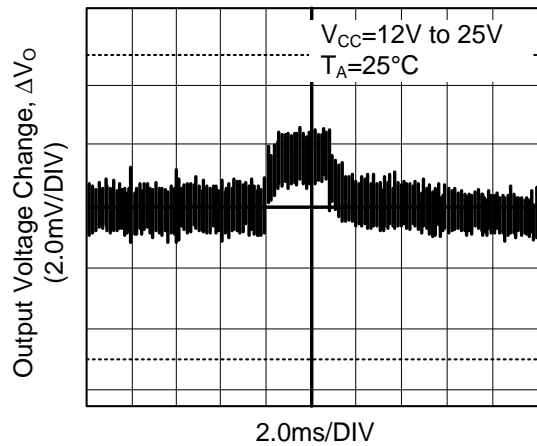
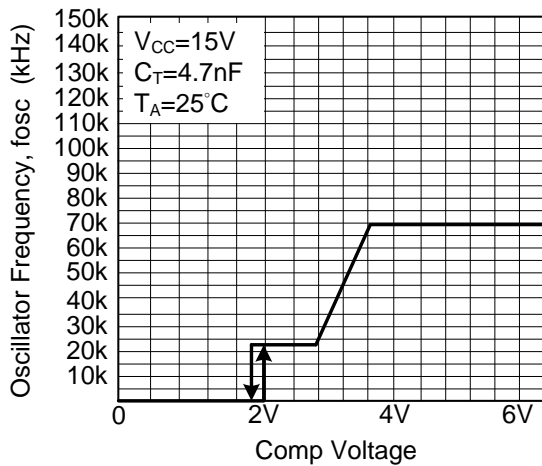


Fig. 11 Fosc Versus Comp Voltage



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