

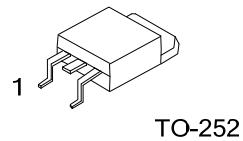
F2N50-MH

Power MOSFET

2.0A, 500V N-CHANNEL POWER MOSFET

■ DESCRIPTION

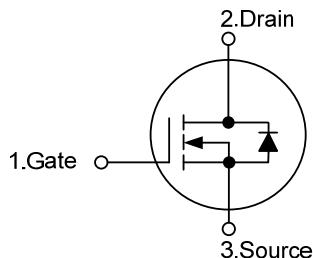
The UTC F2N50-MH is a N-Channel enhancement mode silicon gate power MOSFET with Fast Body Diode, is designed high voltage, high speed power switching applications such, is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient AC to DC converters and bridge circuits.



■ FEATURES

- * $R_{DS(ON)} \leq 5.2 \Omega$ @ $V_{GS}=10V$, $I_D=1.0A$
- * Fast body diode MOSFET technology
- * 100% avalanche tested
- * High switching speed

■ SYMBOL



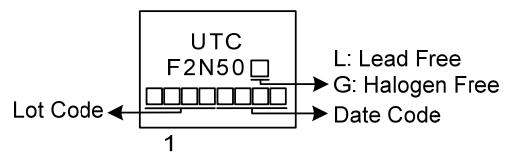
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
F2N50L-TN3-R	F2N50G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>F2N50G-TN3-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING



F2N50-MH

Power MOSFET

■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	2	A
	Pulsed (Note 2)	I_{DM}	4	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	54	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.8	V/ns
Power Dissipation		P_D	30	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature

3. L = 30mH, $I_{AS} = 1.9\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 2.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	110	$^\circ\text{C/W}$
Junction to Case		θ_{JC}	3.6 (Note)	$^\circ\text{C/W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

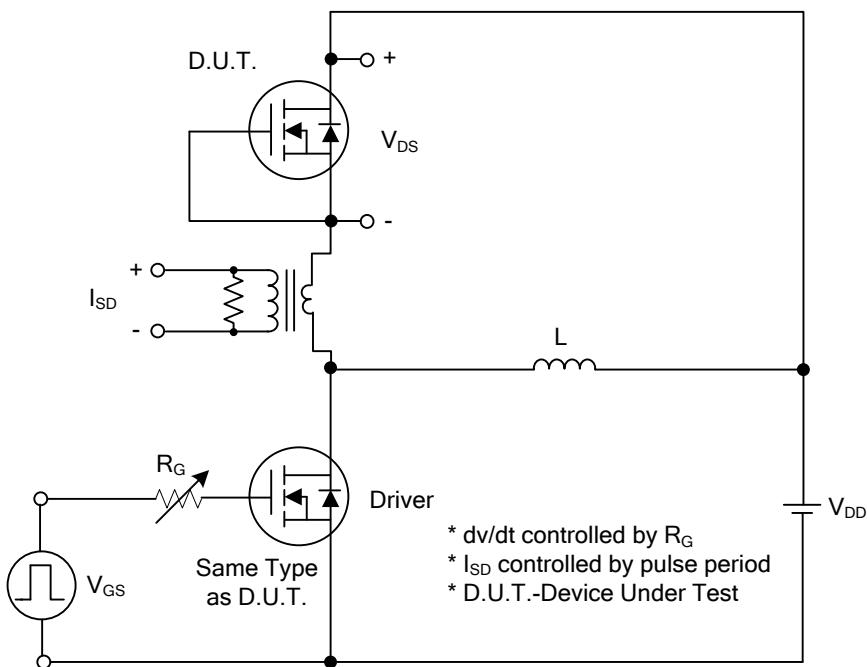
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	500			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate- Source Leakage Current	Forward	$V_{GS}=30\text{V}$, $V_{DS}=0\text{V}$			100	nA
	Reverse	$V_{GS}=-30\text{V}$, $V_{DS}=0\text{V}$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=1.0\text{A}$			5.2	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		150		pF
Output Capacitance	C_{OSS}			26		pF
Reverse Transfer Capacitance	C_{RSS}			3		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=400\text{V}$, $V_{GS}=10\text{V}$, $I_D=2.0\text{A}$ $I_G=1\text{mA}$ (Note 1, 2)		6.5		nC
Gate to Source Charge	Q_{GS}			2.5		nC
Gate to Drain Charge	Q_{GD}			1.2		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DD}=30\text{V}$, $V_{GS}=10\text{V}$, $I_D=2.0\text{A}$, $R_G = 25\Omega$ (Note 1, 2)		6		ns
Rise Time	t_R			18		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			135		ns
Fall-Time	t_F			48		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				2	A
Maximum Body-Diode Pulsed Current	I_{SM}				4	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=2.0\text{A}$, $V_{GS}=0\text{V}$			1.4	V
Body Diode Reverse Recovery Time (Note 1)	t_{rr}	$I_S=2.0\text{A}$, $V_{GS}=0\text{V}$		95		ns
Body Diode Reverse Recovery Charge	Q_{rr}	$dl_F/dt=100\text{A}/\mu\text{s}$		0.5		μC

Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

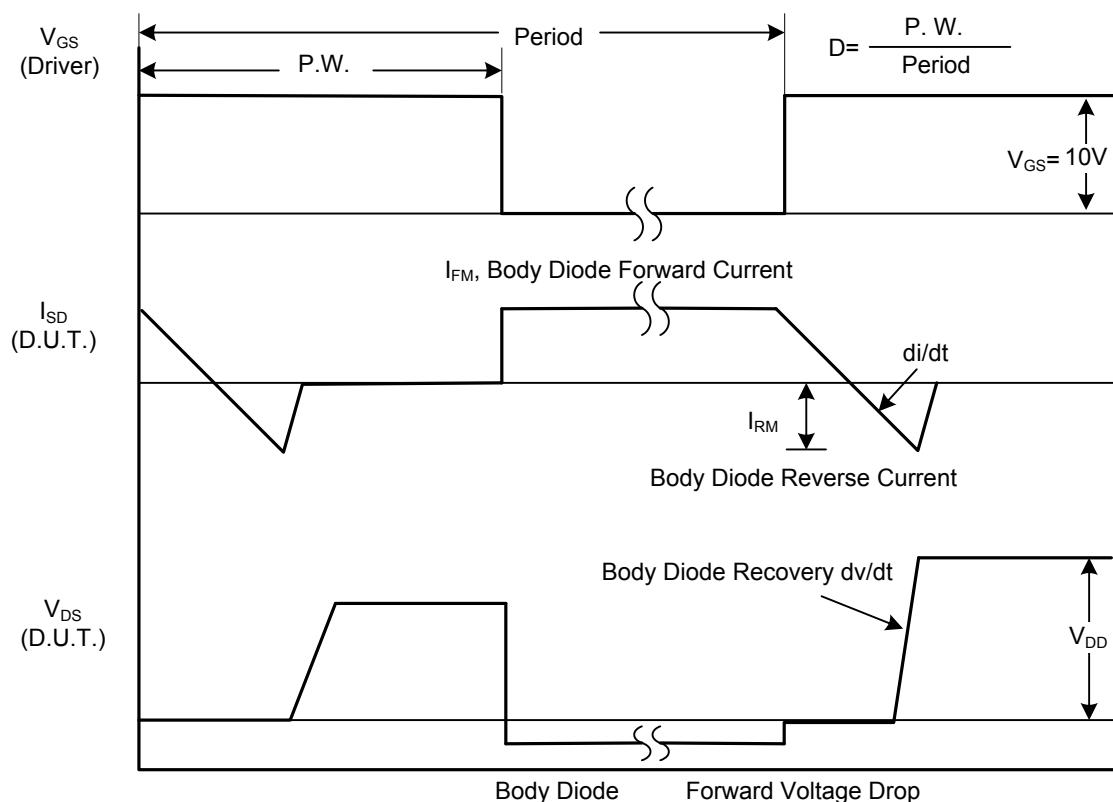
2. Essentially independent of operating temperature.



■ TEST CIRCUITS AND WAVEFORMS

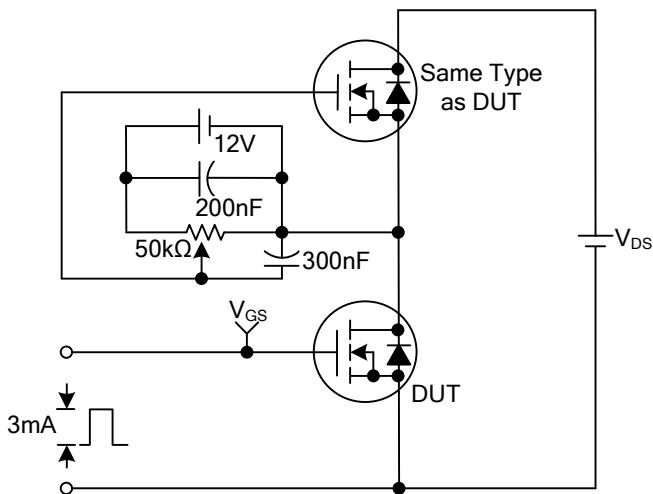


Peak Diode Recovery dv/dt Test Circuit

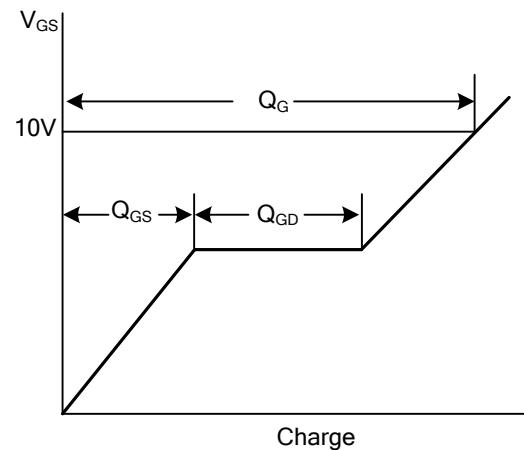


Peak Diode Recovery dv/dt Waveforms

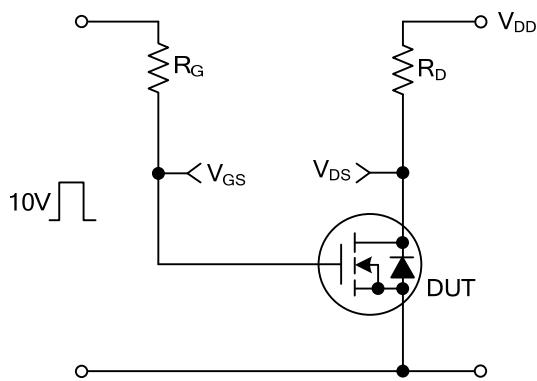
■ TEST CIRCUITS AND WAVEFORMS



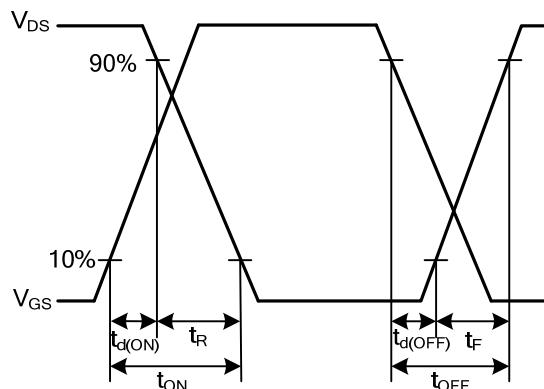
Gate Charge Test Circuit



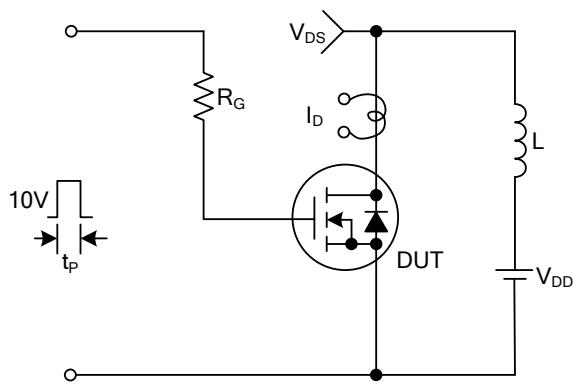
Gate Charge Waveforms



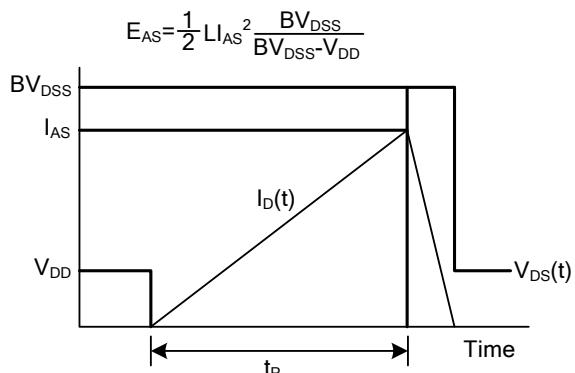
Resistive Switching Test Circuit



Resistive Switching Waveforms

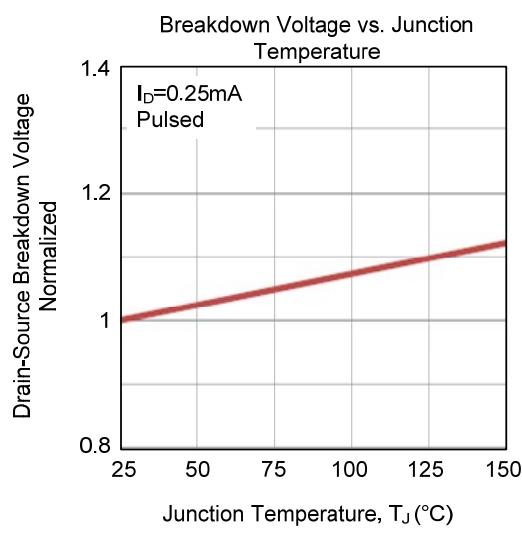
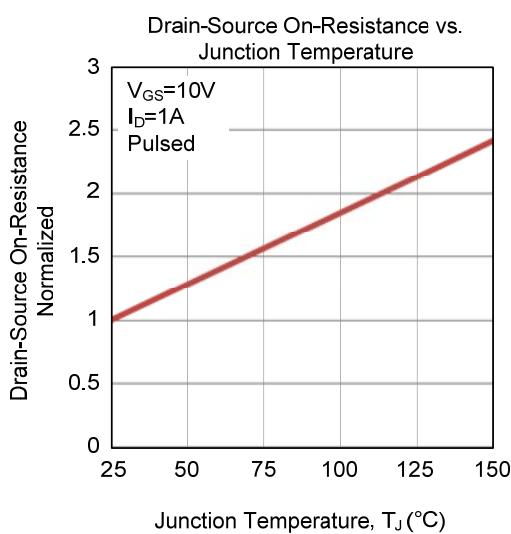
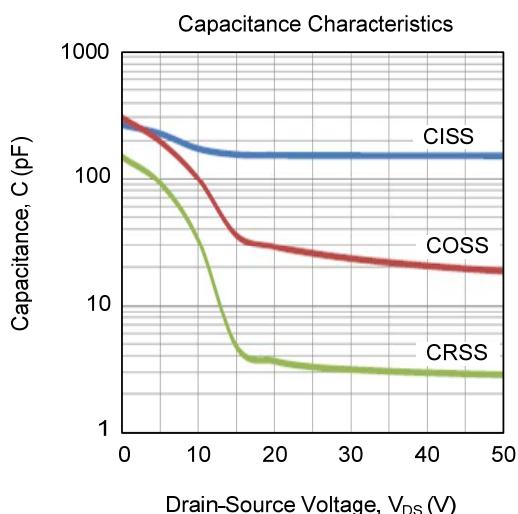
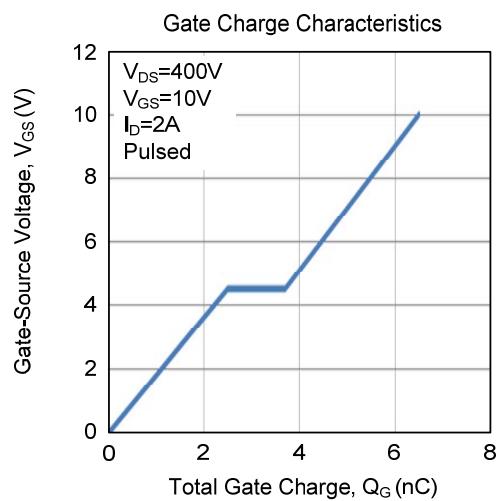
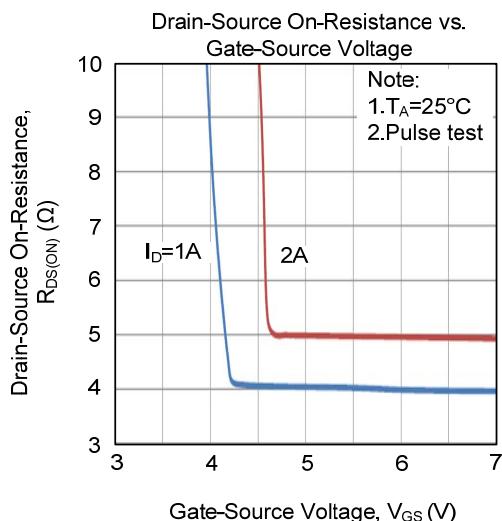
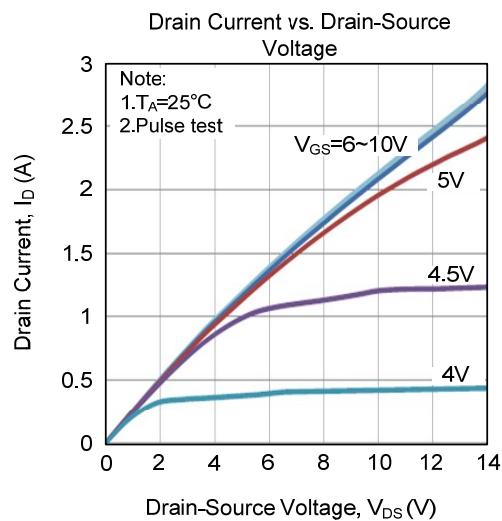


Unclamped Inductive Switching Test Circuit

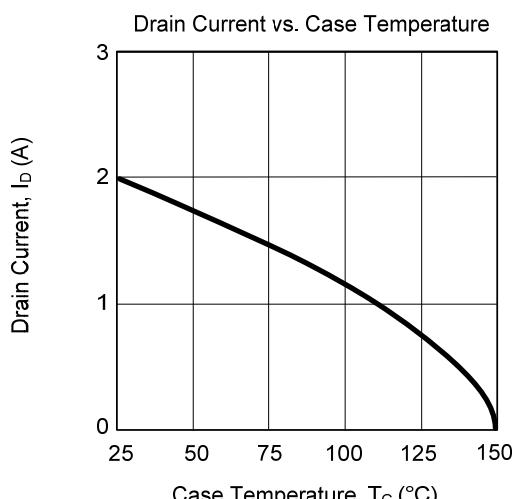
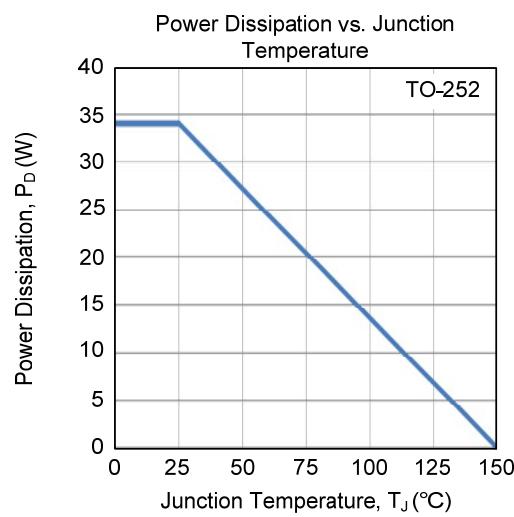
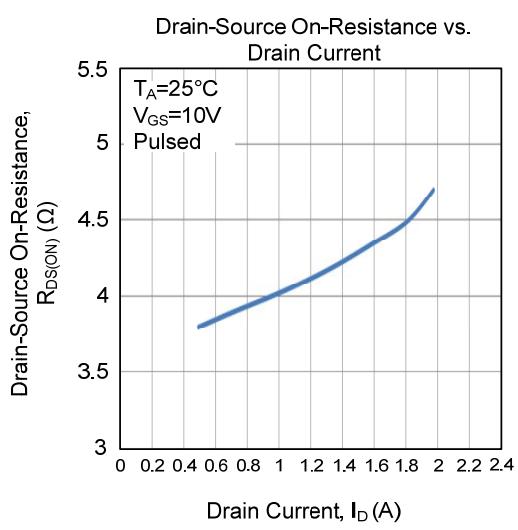
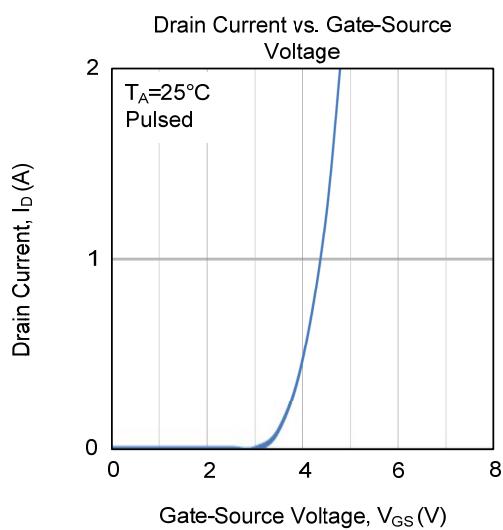
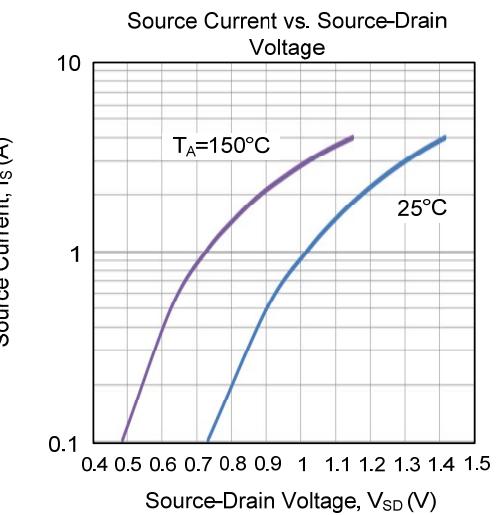
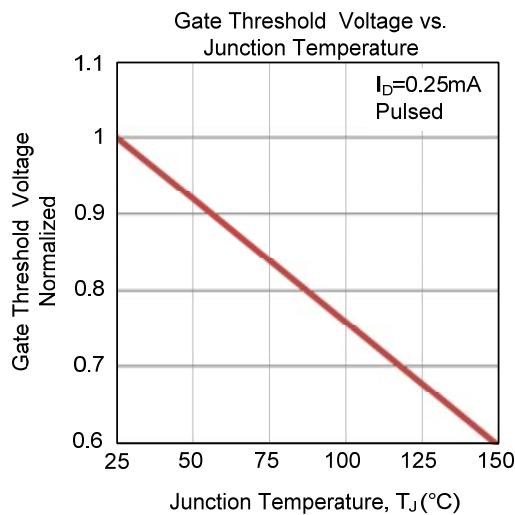


Unclamped Inductive Switching Waveforms

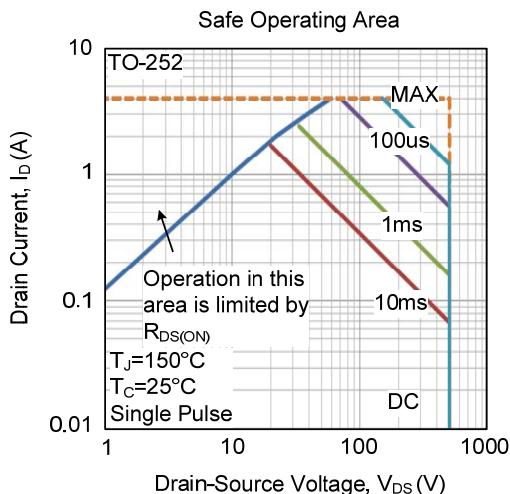
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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