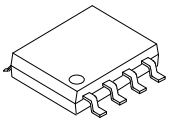
CURRENT MODE PWM CONTROLLER



SOP-8

■ DESCRIPTION

The UTC **UC3849** is a highly integrated low cost current mode PWM controller.

The PWM switching frequency can be programmed at normal operation externally and trimmed to tight range. The circuit works in extended 'burst mode' under no load or light load condition, which aims at minimizing switching loss. This can achieve lower standby power and higher conversion efficiency.

With a low startup current, the UTC **UC3849** could use a large value start-up resistor. Built-in slope compensation enhances the stability of the system. Leading-edge blanking on sense input removes the signal glitch due to snubber circuit diode reverse recovery.

The UTC **UC3849** includes protection function like: OCP (Cycle-by-Cycle current limiting), OLP (over load protection), UVLO (under voltage lockout). The OCP threshold compensation is internally-designed to reach constant output power. With UTC advanced frequency shuffing technique, EMI performance is greatly improved.

It has such application as laptop/power adaptor, PC/TV/set-top box power supplies, open-frame SMPS, battery charge and so on.

■ FEATURES

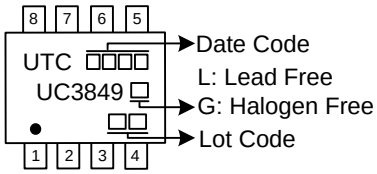
* Low V_{IN}/V_{DD} Startup Current: 3.5μA
* Low Operating Current: 0.8mA
* Under Voltage Lockout (UVLO)
* Burst Mode Control for Improved Efficiency
* Minimum Standby Power Design
* Audio Noise Free Operation
* Programmable PWM Frequency
* Built-in Synchronized Slope Compensation
* Leading Edge Blanking on Sense Input
* Complete Protection Coverage with Auto Self-Recovery
  - External Programmable over Temperature Protection (OTP)
  - With or Without On-chip V_{DD} OVP for System OVP
  - Under Voltage Lockout with Hysteresis (UVLO)
  - Gate Output Maximum Voltage Clamp (16V)
  - Line Compensated Cycle-by-Cycle Over-Current Threshold Setting For Constant Output Current Limiting Over Universal Input Voltage Range (OCP)
  - Over Load Protection. (OLP)

■ ORDERING INFORMATION

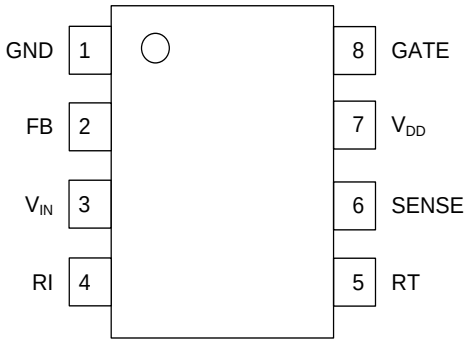
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UC3849L-S08-R	UC3849G-S08-R	SOP-8	Tape Reel

UC3849G-S08-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



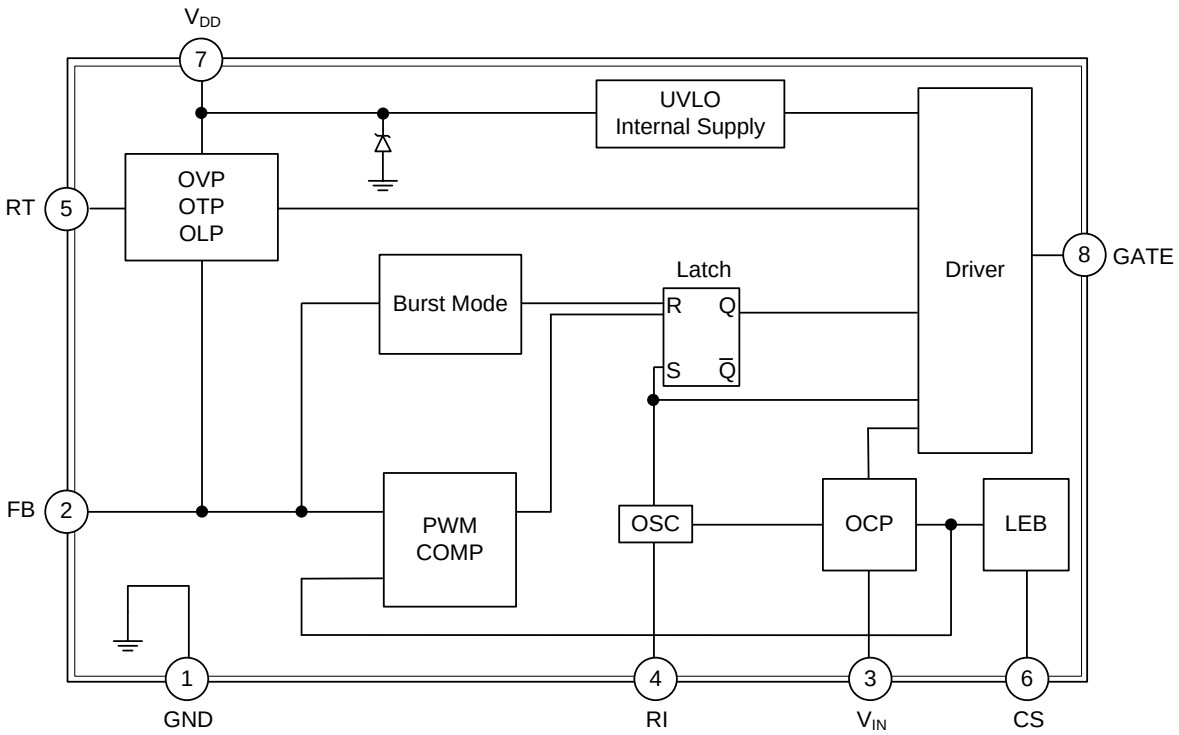
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	GND	P	Ground
2	FB	I	Feedback input pin. PWM duty cycle is determined by voltage level into this pin and current-sense signal level at Pin 6.
3	V_{IN}	I	Connected through a large value resistor to rectified line input for Startup IC supply and line voltage sensing.
4	RI	I	Internal Oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.
5	RT	I	Temperature sensing input pin. Connected through a NTC resistor to GND.
6	SENSE	I	Current sense input pin. Connected to MOSFET current sensing resistor node.
7	V_{DD}	P	DC power supply pin.
8	GATE	O	Totem-pole gate drive output for power MOSFET.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage	V_{DD}/V_{IN}	36	V
Zener Clamp Voltage (Note 2)	V_{DD}	V_{DD}_Clamp+0.1	V
V_{DD} Clamp Continuous Current	I_{VDD}	10	mA
Input Voltage	V_{FB}	-0.3 ~ 7	V
Input Voltage to Sense Pin	V_{SENSE}	-0.3 ~ 7	V
Input Voltage to RT Pin	V_{RT}	-0.3 ~ 7	V
Input Voltage to RI Pin	V_{RI}	-0.3 ~ 7	V
Operating Junction Temperature	T_J	-20 ~ +150	°C
Storage Temperature	T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. V_{DD} Clamp has a nominal value of 35V.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	150	°C/W

■ RECOMMENDED OPERATING CONDITION

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD} Supply Voltage	V_{DD}		11.5		25	V
RI Resistor Value	RI		100		130	KΩ
Ambient Operating Temperature	T_{OPR}		-20		85	°C

■ ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{DD}=16V, RI=100KΩ. Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY SECTION						
Start Up Current	$I_{VDD(Startup)}$	$V_{CC}=V_{CCon}$-0.1V		4	15	μA
Operation Current	$I_{VDD(Operation)}$	V_{FB}=3V		0.8	1.8	mA
Start Threshold Voltage	$V_{CC(ON)}$		15.5	16.5	17.5	V
Min. Operating Voltage	$V_{CC(MIN)}$		8.7	9.7	11	V
OVP Threshold	V_{OVP}	V_{FB}=3V	27	28.5	30	V
V_{CC} Zener Clamp Voltage	V_{CC}(clamp)	I_{CC}=10mA	31	33	35	V
OSC SECTION						
Frequency in Normal Mode	$F_{(SW)}$	V_{FB}=4V	60	65	70	kHz
Frequency in Power-Saving Mode		V_{FB}=1.5V	20			kHz
Shuffling Frequency	$\Delta F_{(SW)}/F_{(SW)}$		-9		+9	%
Frequency Variation VS V_{CC} Deviation	F_{DV}	V_{CC}=12V ~ 25V			10	%
Frequency Variation VS Temperature Deviation	F_{DT}	T=-20 ~ 105°C			10	%
Max Duty Cycle	DC_{MAX}	V_{FB}=4.4V, V_{CS}=0	70	77	85	%
FEEDBACK INPUT SECTION						
PWM Input Gain	A_{VCS}	$\triangle V_{FB}/\triangle V_{CS}$		3		V/V
V_{FB} Open Voltage	$V_{FB(Open)}$			5.5		V
FB Pin Short Circuit Current	$I_{FB(Short)}$	Short FB pin to GND		0.24		mA
Burst-Mode Out FB Voltage	V_{FB-OUT}	V_{CS}=0		1.07		V
Reduce-Frequency end FB Voltage	V_{FB-END}	V_{CS}=0		1.13		V
OLP Threshold	V_{FB-OLP}	V_{CS}=0		4.65		V
Delay Time Of OLP	T_{D-OLP}			88		mS
CURRENT LIMITING SECTION						
Peak Current Limitation	V_{CS}	V_{FB}=4.4V，I_{VIN}=0	0.84	0.97	1.10	V
L.E.B Time				350		nS
Threshold Voltage For I_{VIN}=0	$V_{SENSE-H}$	I_{VIN}=0		0.97		V
Threshold Voltage For I_{VIN}=60uA	$V_{SENSE-L}$	I_{VIN}=170uA		0.84		V
GATE SECTION						
Output Voltage Low State	V_{OL}	I_{SINK}=20mA			0.8	V
Output Voltage High State	V_{OH}	I_{SOURCE}=20mA	10			V
Output Voltage Rise Time	t_R	CL = 1.0 nF	150	300	500	ns
Output Voltage Fall Time	t_F	CL = 1.0 nF	30	60	100	ns
OVER TEMPERATURE PROTECT SECTION						
Output Current of RT Pin	I_{RT}		94	100	106	μA
OTP Threshold Voltage	$V_{TH(OTP)}$		0.89	0.94	0.99	V
FREQUENCY SHUFFLING SECTION						
Frequency Shuffling Section	$F_{REQ(Shuffling)}$			4		mS

■ OPERATION DESCRIPTION

Startup Current and Start up Control

The UTC **UC3849** use a large value startup resistor which is about 2 MΩ and 1/8W, so the startup current is to be very low and power dissipation is low. For a typical AC/DC adaptor with universal input range design , a capacitor is used to provide a fast startup.

The turn-on and turn-off threshold of the UTC **UC3849** is design to 16.5V /10V. During startup, the hold-up capacitor must be charge to 16.5V through the startup resistor.

Frequency shuffling for EMI improvement

The UTC **UC3849** operates with the frequency shuffling/jittering (switching frequency modulation). The oscillation frequency is modulated with an internally generated random source so that the tone energy is evenly spread out. The spread spectrum minimizes the conduction band EMI, thus eases the system design in satisfying the requirement for stringent EMI.

Green Power Operation

The power dissipation of switching mode power supply is very important in zero load or light load condition, the core loss of the transformer and the loss on the snubber circuit. The transformer power loss is in proportion to the number of the switching events within a fixed period of time especially in zero load or light load condition, so reducing the switching event frequency play important part in reduction of power loss. At from no load to light/medium, when FB input above burst out threshold level (1.13V), the IC work out of burst mode. At from medium load to light load, when FB input below light load level (2.65V), the IC reduce the switching event frequency. At from light load to no load, when FB input below burst enter level (1.07V), the MOSFET transistor will be shutdown，in this way the power dissipation is reduced.

Current Sensing & Constant Output Power Limiting & Leading edge Blanking

The switch current is detected by a sense resistor into the sense pin. If OCP threshold voltage is fixed, output power will be change along with universal AC input range. UTC UC3489 offered Cycle-by-Cycle current limiting and OCP threshold compensation which is in aversely proportional to AC input, so that constant output power limiting can be got. When sense input is over OCP threshold voltage, the current limit comparator can turn off the external MOSFET. At initial external MOSFET on state, an internal leading edge blanking circuit turn off the sense voltage spike. The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

If the IC works at CCM and duty cycle above 50%, the close loop will not stability. UTC **UC3849** adds voltage ramp onto the sense pin voltage. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation.

Gate Drive

The UTC **UC3849** Gate and the Gate of an external MOSFET are connected together for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI. Good tradeoff is achieved through the internal totem pole gate drive design with right output strength and dead time control. With this dedicated control scheme, the low idle loss and good EMI system design can be achieved easier. Moreover, an internal 16V clamp is added for MOSFET gate protection at higher than expected V_{DD} input.

■ OPERATION DESCRIPTION (Cont.)

Protection Controls

The UTC **UC3849** includes the following protection circuits for optimizing device performance and system stability: Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), over temperature protection (OTP), on-chip V_{DD} over voltage protection (OVP) and under voltage lockout (UVLO).

Under output overload condition, the voltage at FB pin is biased higher. If FB input becomes higher than the power limit threshold value for a period of more than 88mS, control circuit would shut down the Power MOSFET. In addition, when an over temperature condition occurs, the control circuit would turn off the power MOSFET, and this device turns back to the normal operation after temperature drops below the hysteresis value.

V_{DD} is supplied with transformer auxiliary winding output. It is clamped when V_{DD} exceeds 33V. When the voltage of V_{DD} pin is lower than UVLO (enter) limit, the Power MOSFET is turned off and device enters power on startup sequence thereafter.

The OCP threshold value is self adjusted lower at higher current into VIN pin. This OCP threshold slope adjustment helps to compensate the increased output power limit at higher AC voltage caused by inherent Over-Current sensing and control delay. A constant output power limit is achieved with recommended OCP compensation scheme on the UTC **UC3849**.

Over Temperature Protection

For UTC **UC3849**, in order to protect this circuit against over temperature, a NTC resistor is located between RT and GND in series with a regular. The value of this NTC transistor drops low when the ambient temperature rises. The RT pin voltage goes low at high temperature as the fixed internal current IRT flowing through the resistors. The internal OTP circuit is triggered and shutdown the MOSFET when the sensed input voltage is lower than V_{TH}_OTP.

■ TYPICAL APPLICATION CIRCUIT