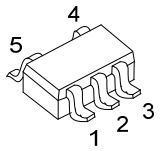
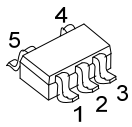
U74CBTLV1G125

CMOS IC

LOW-VOLTAGE SINGLE FET BUS SWITCH



SOT-25



SOT-353

SOT-553

■ DESCRIPTION

The **U74CBTLV1G125** provides a single high-speed line switch. The switch is disabled when the output-enable ($\overline{OE}$) input is high.

This device is fully specified for partial-power-down applications using I_{OFF}. The I_{OFF} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

■ FEATURES

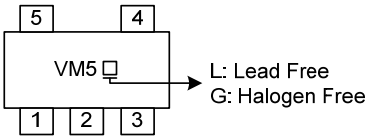
* 5Ω Switch Connection Between Two Ports
* Rail-to-Rail Switching on Data I/O Ports
* I_{OFF} Supports Partial-Power-Down Mode

■ ORDERING INFORMATION

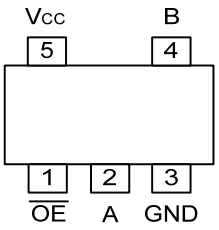
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74CBTLV1G125L-AF5-R	U74CBTLV1G125G-AF5-R	SOT-25	Tape Reel
U74CBTLV1G125L-AL5-R	U74CBTLV1G125G-AL5-R	SOT-353	Tape Reel
U74CBTLV1G125L-AN5-R	U74CBTLV1G125G-AN5-R	SOT-553	Tape Reel

U74CBTLV1G125G-AF5-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) AF5: SOT-25, AL5: SOT-353, AN5: SOT-553 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



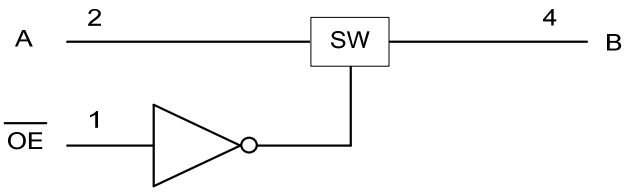
■ PIN CONFIGURATION



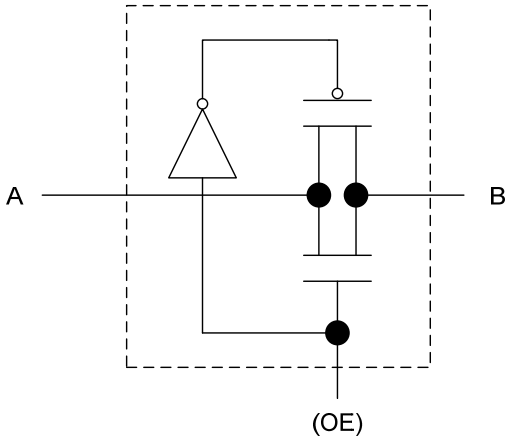
■ FUNCTION TABLE (each bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

■ LOGIC DIAGRAM (positive logic)



■ SIMPLIFIED SCHEMATIC(each FET switch)



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 4.6	V
Input Voltage	V_I	-0.5 ~ 4.6	V
Continuous Channel Current		128	mA
Input Clamp Current($V_{I/O}$<0)	I_{IK}	-50	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOT-25	θ_{JA}	230	°C/W
	SOT-353		350	°C/W
	SOT-553		370	°C/W

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.3		3.6	V
High-control input voltage	V_{IH}	V_{CC}=2.3V~2.7V	1.7			V
		V_{CC}=2.7V~3.6V	2			V
Low-control input voltage	V_{IL}	V_{CC}=2.3V~2.7V			0.7	V
		V_{CC}=2.7V~3.6V			0.8	V
Ambient Operating Temperature	T_A		-40		+125	°C

Note: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ STATIC CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS			T_A=25°C			T_A=-40~+125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
Digital Input Diode Voltage	V_{IK}	V_{CC} =3V, I_I=-18mA					-1.2			-1.2	V
Input Leakage Current	I_I	V_{CC}=3.6V, V_I=V_{CC} or GND					±1			±100	μA
Power off Leakage Current	I_{off}	V_{CC}=0,V_I or V_O=0 to 3.6V					10			10	μA
Quiescent Supply Current	I_{CC}	V_{CC}=3.6V, V_I= V_{CC} or GND, I_O=0					10			200	μA
Additional Quiescent Supply Current — Control inputs	ΔI_{CC} (Note 2)	V_{CC}=3.6V, One input at 3V, Other inputs at V_{CC} or GND					300			5000	μA
Resistor between two ports	R_{ON} (Note 3)	V_{CC}=2.3V Typ. at V_{CC}=2.5V	V_I=0V	I_I=64mA		7	10			15	Ω
				I_I=24mA		7	10			15	Ω
			V_I=1.7V, I_I=-15mA			15	25			38	Ω
		V_{CC}=3V	V_I=0V	I_I=64mA		5	7			11	Ω
				I_I=24mA		5	7			11	Ω
			V_I=2.4V, I_I=-15mA			10	15			25.5	Ω

Notes: 1. All typical values are at V_{CC}=3.3V (unless otherwise noted), T_A=25°C.
2. This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
3. Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

■ DYNAMIC CHARACTERISTICS

See Fig. 1 and Fig. 2 for test circuit and waveforms.

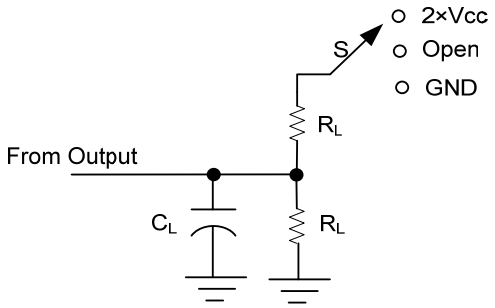
PARAMETER	SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
From input (A or B) to output (B or A)	t_{pd} (t_{PLH}/t_{PHL})	V_{CC}=2.5V±0.2V			0.21			0.4	ns
		V_{CC}=3.3V±0.3V			0.25			0.5	ns
From input ($\overline{OE}$) to output (A or B)	t_{en} (t_{PZL}/t_{PZH})	V_{CC}=2.5V±0.2V	1		5.5			6.5	ns
		V_{CC}=3.3V±0.3V	1		5.5			6.5	ns
From input ($\overline{OE}$) to output (A or B)	t_{dis} (t_{PLZ}/t_{PHZ})	V_{CC}=2.5V±0.2V	1		5			6.3	ns
		V_{CC}=3.3V±0.3V	1		4.1			5.4	ns

Note: The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

■ OPERATING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Control input Capacitance	C_I	V_I=3V or 0		2.5		pF
I/O Capacitance (OFF)	$C_{IO(OFF)}$	V_O=3V or 0, $\overline{OE}$ =V_{CC}		7		pF

■ TEST CIRCUIT AND WAVEFORMS

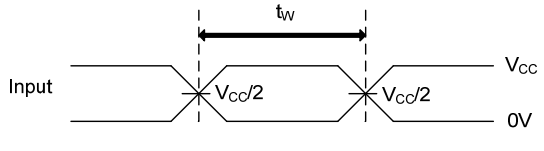


V_{CC}	R_L	C_L	VΔ
2.5V±0.2V	500	30pF	0.15V
3.3V±0.3V	500	50pF	0.3V

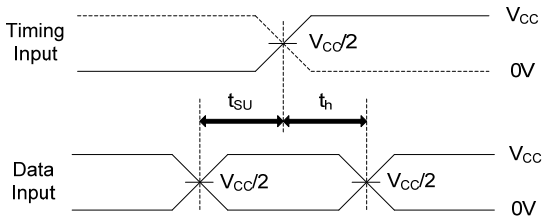
TEST	S
t_{PD}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	2×Vcc

Note: C_L includes probe and jig capacitance.

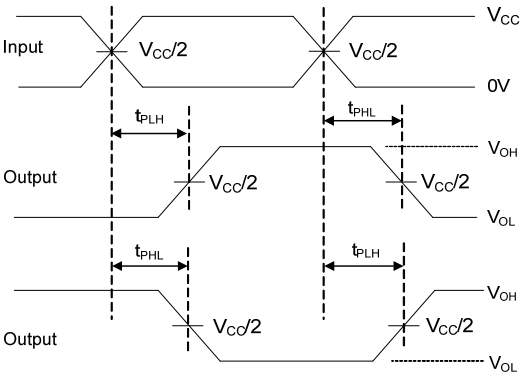
Fig. 1 Load circuitry for switching times



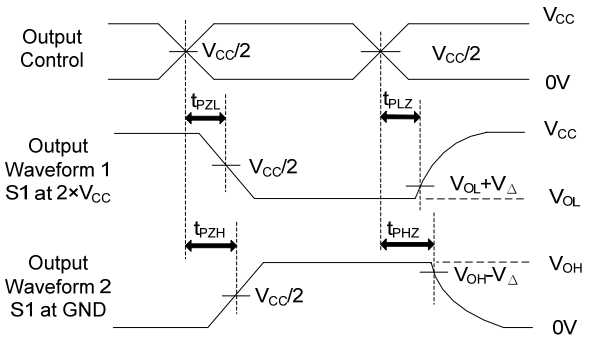
PULSE DURATION



SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Note: All input pulses are supplied by generators having the following characteristics:
t_r, t_f ≤ 2ns; P_{RR} ≤ 10MHz; Z_O=50Ω.

Fig. 2 Propagation delay from input(A) to output(B) and Output transition time