



## F1N50-HD

Preliminary

Power MOSFET

## 1.0A, 500V N-CHANNEL POWER MOSFET

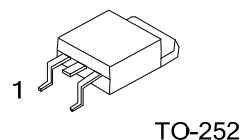
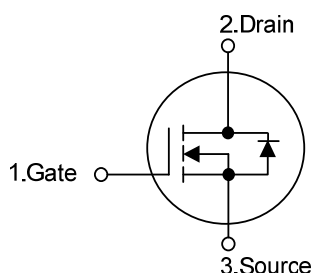
### DESCRIPTION

The UTC **F1N50-HD** is a N-Channel enhancement mode silicon gate power MOSFET with Fast Body Diode. is designed high voltage, high speed power switching applications such. such as fast switching time, low gate charge, low on-state resistance and high rugged avalanche characteristics.

### FEATURES

- \*  $R_{DS(ON)} \leq 8.2 \Omega$  @  $V_{GS}=10V$ ,  $I_D=0.5A$
- \* Fast body diode MOSFET technology
- \* Fast switching capability
- \* Avalanche energy tested
- \* Improved dv/dt capability, high ruggedness

### SYMBOL



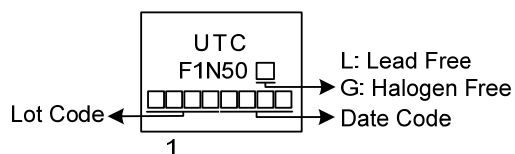
### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
F1N50L-TN3-R	F1N50G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>F1N50G-TN3-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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### MARKING



■ ABSOLUTE MAXIMUM RATINGS ( $T_C=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	500	V
Gate-Source Voltage		$V_{GSS}$	$\pm 30$	V
Drain Current	Continuous	$I_D$	1	A
	Pulsed (Note 2)	$I_{DM}$	2	A
Avalanche Energy	Single Pulsed (Note 3)	$E_{AS}$	34	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	6.6	V/ns
Power Dissipation		$P_D$	29	W
Junction Temperature		$T_J$	+150	$^{\circ}\text{C}$
Storage Temperature		$T_{STG}$	-55 ~ +150	$^{\circ}\text{C}$

- Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.  
 2. Repetitive Rating : Pulse width limited by maximum junction temperature.  
 3.  $L=30\text{mH}$ ,  $I_{AS}=1.5\text{A}$ ,  $V_{DD}=90\text{V}$ ,  $R_G=25\Omega$ , Starting  $T_J = 25^{\circ}\text{C}$   
 4.  $I_{SD} \leq 0.5\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	110	$^{\circ}\text{C}/\text{W}$
Junction to Case	$\theta_{JC}$	4.31	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

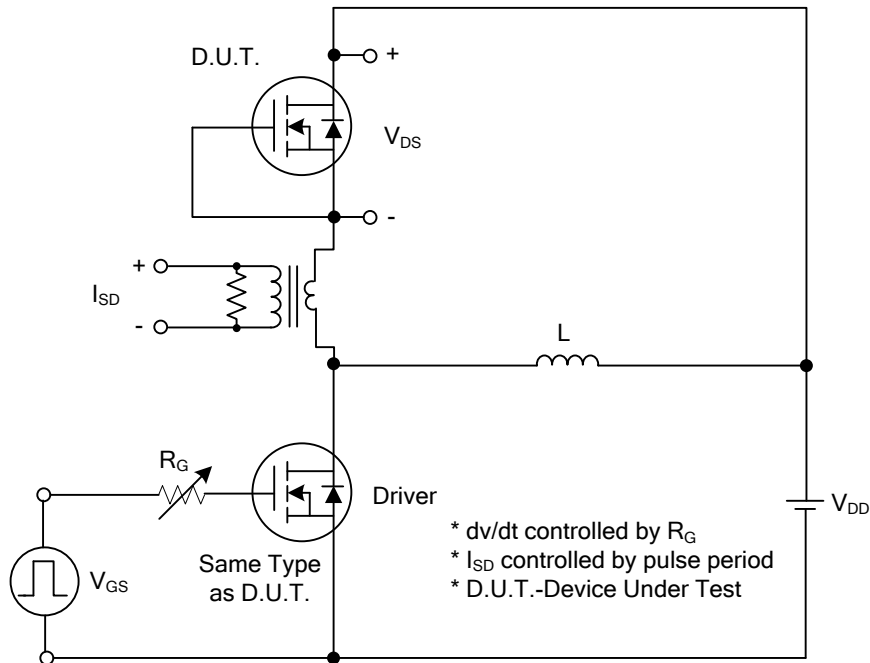
■ ELECTRICAL CHARACTERISTICS (T<sub>J</sub>=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	500			V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =500V, V <sub>GS</sub> =0V			10	μA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =30V, V <sub>DS</sub> =0V			100	nA
		V <sub>GS</sub> =-30V, V <sub>DS</sub> =0V			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2.0		4.0	V
Drain to Source On-state Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =0.5A			8.2	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1.0MHz		146		pF
Output Capacitance	C <sub>OSS</sub>			19		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			2.1		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q <sub>G</sub>	V <sub>DS</sub> =400V, V <sub>GS</sub> =10V, I <sub>D</sub> =1A, I <sub>G</sub> =1mA (Note 1, 2)		4.3		nC
Gate Source Charge	Q <sub>GS</sub>			1.9		nC
Gate Drain Charge	Q <sub>GD</sub>			0.8		nC
Turn-ON Delay Time (Note 1)	t <sub>D(ON)</sub>	V <sub>DD</sub> =100V, V <sub>GS</sub> =10V, I <sub>D</sub> =1A, R <sub>G</sub> =25Ω (Note 1, 2)		5		ns
Turn-ON Rise Time	t <sub>R</sub>			15		ns
Turn-OFF Delay Time	t <sub>D(OFF)</sub>			11		ns
Turn-OFF Fall-Time	t <sub>F</sub>			23		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I <sub>S</sub>				1	A
Maximum Pulsed Drain-Source Diode Forward Current	I <sub>SM</sub>				2	A
Drain-Source Diode Forward Voltage (Note 1)	V <sub>SD</sub>	I <sub>S</sub> =1A, V <sub>GS</sub> =0V			1.4	V
Reverse Recovery Time (Note 1)	t <sub>rr</sub>	I <sub>S</sub> =1A, V <sub>GS</sub> =0V, dI/dt=100A/μs		62		ns
Reverse Recovery Charge	Q <sub>rr</sub>			121		nC

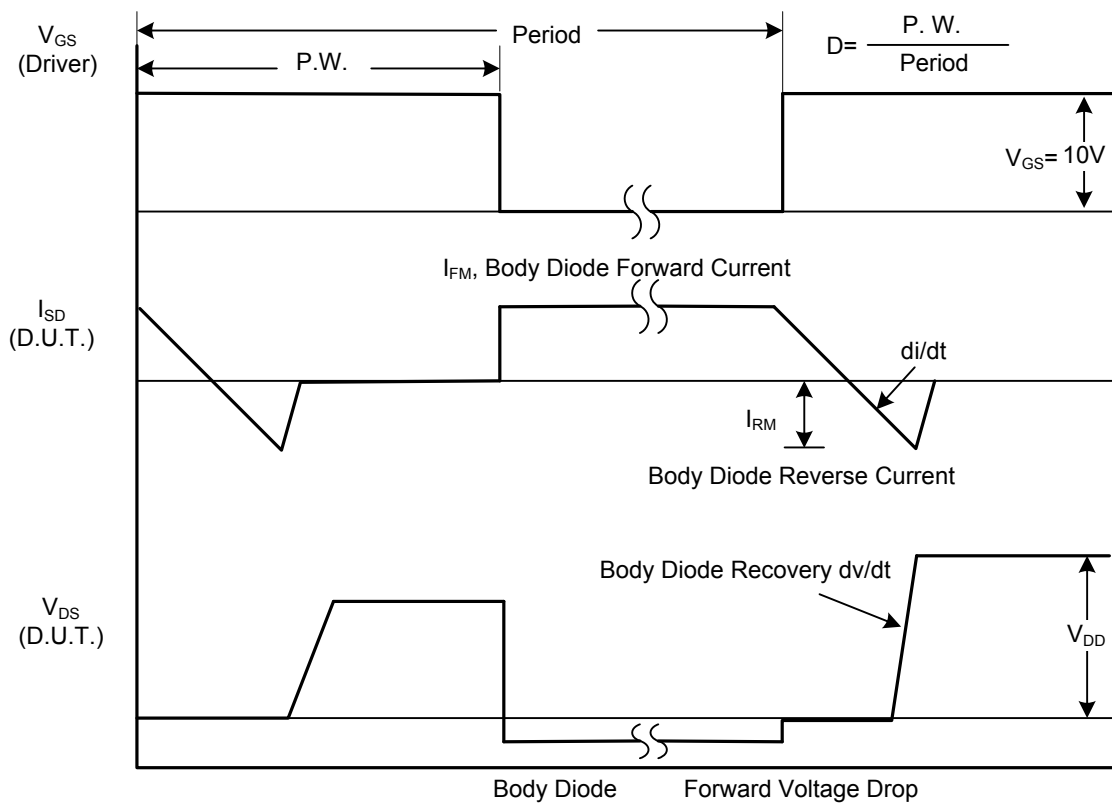
Notes: 1. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS

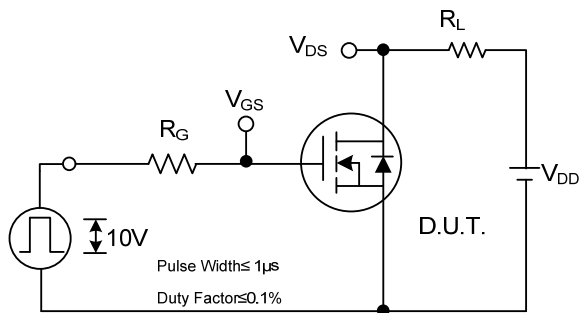


Peak Diode Recovery  $dv/dt$  Test Circuit

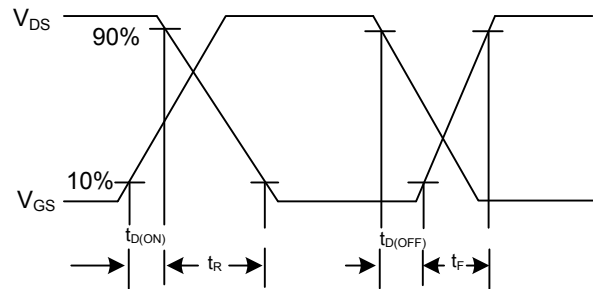


Peak Diode Recovery  $dv/dt$  Waveforms

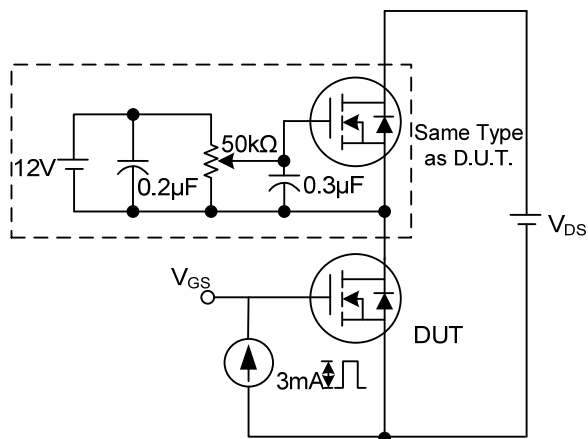
# TEST CIRCUITS AND WAVEFORMS



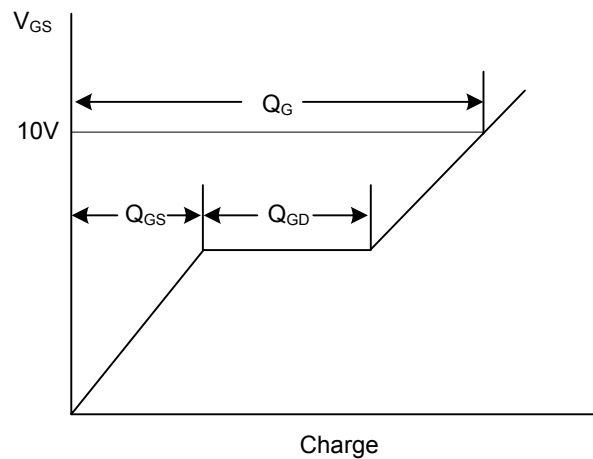
Switching Test Circuit



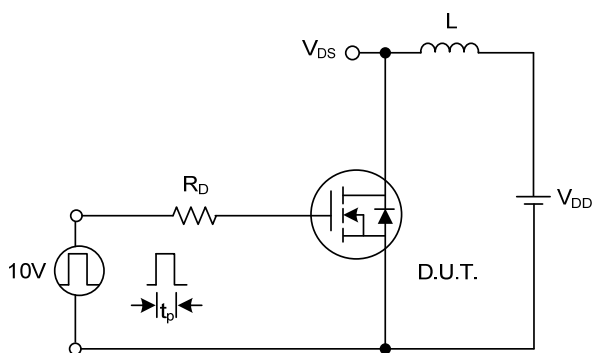
Switching Waveforms



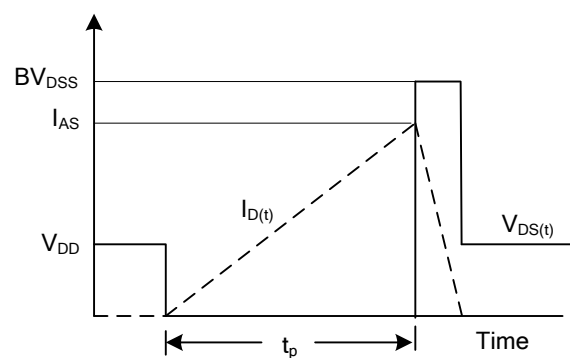
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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