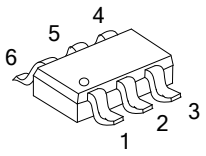
UGD9511

Preliminary ***LINEAR INTEGRATED CIRCUIT***

SINGLE-CHANNEL, HIGH-SPEED, LOW-SIDE GATE DRIVER



SOT-26

■ DESCRIPTION

UTC **UGD9511** single-channel, high speed, low-side gate-driver device can effectively drive MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, UGD9511 are capable of sourcing and sinking high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay, typically 13ns.

■ FEATURES

* Low-Cost Gate-Driver Device Offering Superior Replacement of NPN and PNP Discrete Solutions
* Strong Sink Current Offers Enhanced Immunity against Miller Turn on
* Split Output Configuration (Allows Easy and Independent Adjustment of Turn on and Turn off Speeds) in the **UGD9511** Saves 1 Diode
* Fast Propagation Delays (13-nsTypical)
* Fast Rise and Fall Times (9ns and 7ns Typical)
* 4.5V to 18V Single Supply Range
* Output Held Low When Input Pins Are Floating
* Outputs Held Low During V_{DD} UVLO (Ensures Glitch-Free Operation at Power Up and Power-Down)
* TTL and CMOS Compatible Input-Logic Threshold (Independent of Supply Voltage)
* Hysteretic-Logic Thresholds for High-Noise Immunity
* Dual-Input Design (Choice of an Inverting (IN–Pin) or Non inverting (IN+ Pin) Driver Configuration) Unused Input Pin can be Used for Enable or Disable Function
* Input Pin Absolute Maximum Voltage Levels Not Restricted by V_{DD} Pin Bias Supply Voltage

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UGD9511L-AG6-R	UGD9511G-AG6-R	SOT-26	Tape Reel

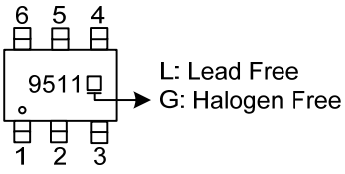
UGD9511G-AG6-R

(1)Packing Type — (1) R: Tape Reel

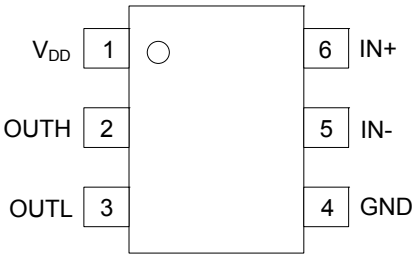
(2)Package Type — (2) AG6: SOT-26

(3)Green Package — (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



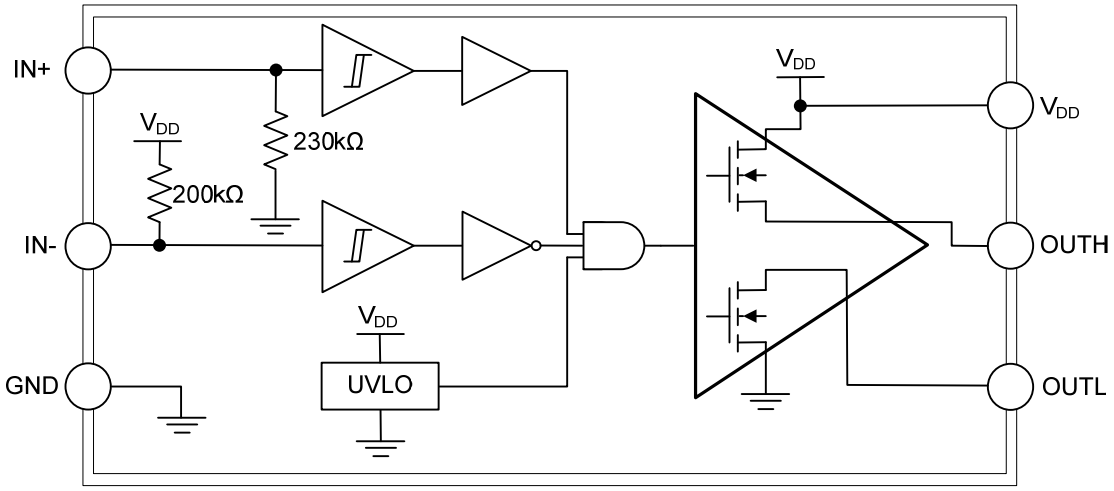
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	V_{DD}	I	Bias supply input.
2	OUTH	O	Sourcing current output of driver.
3	OUTL	O	Sinking current output of driver.
4	GND	-	Ground
5	IN-	I	Inverting input
6	IN+	I	Non inverting input

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	20	V
OUTH Voltage		V_{DD}	V
OUTL Voltage	DC	20	V
Output Continuous Current (OUTH Source Current and OUTL Sink Current)	I_{OUT_DC} (source)	0.3	A
	I_{OUT_DC} (sink)	0.6	A
Input voltage	IN+, IN-	20 (Note 2)	V

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Maximum voltage on input pins is not restricted by the voltage on the V_{DD} pin.

■ RECOMMENDED OPERATING CONDITIONS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD} Supply Voltage Range	V_{DD}		4.5	12	18	V
Input Voltage	IN+, IN-		0		18	V
Operating Junction Temperature Range	T_J		-40		+125	V

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, VINT)							
Startup Current	$I_{DD(off)}$	V_{DD}=3.4V	IN+=V_{DD}, IN-=GND	40	100	160	μA
			IN+=IN-=GND or IN+ =IN-=V_{DD}	25	75	145	μA
			IN+=GND, IN-=V_{DD}	20	60	115	μA
UNDER VOLTAGE LOCK OUT (UVLO)							
Supply Start Threshold	V_{ON}	T_A=25°C		3.91	4.20	4.5	V
		T_A=-40°C~140°C		3.70	4.20	4.65	V
Minimum Operating Voltage After Supply Start	V_{OFF}			3.45	3.9	4.35	V
Supply Voltage Hysteresis	V_{DD_H}			0.2	0.3	0.5	V
INPUTS (IN+,IN-)							
Input Signal High Threshold	V_{IN_H}	Output high for IN+ pin, Output low for IN–pin			2.6	2.8	V
Input Signal Low Threshold	V_{IN_L}	Output low for IN+ pin, Output high for IN–pin		1.0	1.2		V
Input Signal Hysteresis	V_{IN_HYS}				1.0		V
SOURCE / SINK CURRENT							
Source/Sink Peak Current	$I_{SRC/SNK}$	C_{LOAD}=0.22μF, F_{SW}=1kHz			-4/+8		A
OUTPUTS (OUTH, OUTL,OUT)							
High Output Voltage	V_{DD}-V_{OH}	V_{DD}=12V, I_{OUTH}= -10mA			50	90	mV
		V_{DD}=4.5V, I_{OUTH}=-10mA			60	130	mV
Low Output Voltage	V_{OL}	V_{DD}=12V, I_{OUTL}=10mA			5	6.5	mV
		V_{DD}=4.5V, I_{OUTL}=10mA			5.5	10	mV
Output Pull-up Resistance	R_{OH}	V_{DD}=12V, I_{OUTH} =- 10mA			5.0	7.5	Ω
		V_{DD}=4.5V, I_{OUTH}=-10mA			5.0	11.0	Ω
Output Pull-Down Resistance	R_{OL}	V_{DD}=12V, I_{OUTL}=10mA			0.375	0.650	Ω
		V_{DD}=4.5V I_{OUTL}=10mA			0.45	0.75	Ω

■ SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
						ns
Rise Time	t_R	V_{DD}=12V, C_{LOAD}=1.8nF, connected to OUTH and OUTL pins tied together		8	12	ns
		V_{DD}=4.5V, C_{LOAD}=1.8nF		16	22	ns
Fall Time	t_F	V_{DD}=12V, C_{LOAD}=1.8nF, connected to OUTH and OUTL pins tied together		7	11	ns
		V_{DD}=4.5V, C_{LOAD}=1.8nF		7	11	ns
IN+ to Output Propagation Delay	t_{D1}	V_{DD}=12V 5V input pulse C_{LOAD}=1.8nF, connected to OUTH and OUTL pins tied together	4	13	23	ns
		V_{DD}=4.5V, 5V input pulse C_{LOAD}=1.8nF,connected to OUTH and OUTL pins tied together	4	15	26	ns
IN- to Output Propagation Delay	t_{D2}	V_{DD}=12V, C_{LOAD}=1.8nF, connected to OUTH and OUTL pins tied together	4	13	23	ns
		V_{DD}=4.5V, C_{LOAD}=1.8nF, connected to OUTH and OUTL pins tied together	4	19	30	ns

■ DETAILED DESCRIPTION

Overview

The **UGD9511** single-channel high-speed low-side gate-driver device is capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, the **UGD9511** device is capable of sourcing and sinking high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay of 13 ns (typical).

The **UGD9511** device provides 4A source, 8A sink (asymmetrical drive) peak-drive current capability. Strong sink capability in asymmetrical drive boosts immunity against parasitic, Miller turn on effect. The **UGD9511** device also features a unique split output configuration where the gate-drive current is sourced through the OUTH pin and sunk through the OUTL pin. This unique pin arrangement allows the user to apply in dependent turn on and turn off resistors to the OUTH and OUTL pins (respectively) and easily control the switching slew rates.

Alternatively the OUTH and OUTL pins can be tied together, which results in a typical gate driver output configuration where the source and sink currents are delivered from the same pin. In case of **UGD9511** device, the state of the device's output is simply determined by the combined states of the OUTH and OUTL pins when tied together. Output high implies that OUTH pin is pulled close to V_{DD} pin bias voltage while OUTL pin is in high-impedance state. Similarly output low implies that OUTL pin is pulled close to the GND pin while OUTH pin is in high-impedance state. OUTH pulled to V_{DD}, while OUTL pulled to GND pin simultaneously is not a valid state for the device.

The **UGD9511** device is designed to operate over a wide V_{DD} range of 4.5 to 18V and wide temperature range of -40°C to 125°C. Internal under voltage lock out (UVLO) circuitry on the V_{DD} pin holds the output low outside V_{DD} operating range. The capability to operate at low voltage levels, such as below 5V, along with best-in-class switching characteristics, is especially suited for driving emerging wide band-gap power-switching devices such as GaN power-semiconductor devices.

The **UGD9511** device features a dual-input design which offers flexibility of implementing both inverting (IN–pin) and non inverting(IN+ pin) configuration with the same device. Either the IN+ or IN– pin can be used to control the state of the driver output. The unused input pin can be used for enable and disable functions. For system robustness, internal pull up and pull down resistors on the input pins ensure that outputs are held low when the input pins are in floating condition. Therefore the unused input pin is not left floating and must be properly biased to ensure that driver output is in enabled for normal operation.

The input pin threshold of the **UGD9511** device is based on TTL and CMOS-compatible low-voltage logic which is fixed and independent of the V_{DD} supply voltage. Wide hysteres is between the high and low thresholds offers excellent noise immunity.

■ FEATURE DESCRIPTION

In the following sections with respect to **UGD9511**, the term output, or OUT refers to the combined state that results when the OUTH pin is tied directly to the OUTL pin. As stated earlier, output high, or OUT high refers to the state when the OUTH pin is pulled close to V_{DD} pin bias voltage while the OUTL pin is in high-impedance state. Similarly output low or OUT low implies that the OUTL pin is pulled close to the GND pin while the OUTH pin is in high-impedance state.

■ TYPICAL APPLICATION CIRCUIT