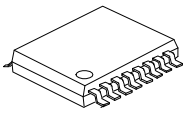
DUAL H-BRIDGE MOTOR DRIVER



TSSOP-16

■ DESCRIPTION

The **UMD9148** provides a dual H-bridge motor driver for home appliances and other mechatronic applications. The device can be used to drive one or two DC motors, a bipolar stepper motor, or other loads. A simple PWM interface allows easy inter facing to controller circuits.

The output block of each H-bridge driver consists of N-channel and P-channel power MOSFETs configured as full H-bridges to drive the motor windings. Each H-bridge includes circuitry to regulate the winding current using a fixed off-time chopping scheme. The **UMD9148** is capable of driving up to 2A of current from each output or 4A of current in parallel mode(with proper heat sinking, at 12V and T_A=25°C).

A low-power sleep mode is provided, which shuts down internal circuitry to achieve very-low quiescent current draw. This sleep mode can be set using a dedicated nSLEEP pin.

Internal protection functions are provided for UVLO, OCP, short-circuit protection, and over temperature. Fault conditions are indicated by an FAULT pin.

■ FEATURES

* Dual H-Bridge Motor Driver Single/Dual Brushed DC Stepper
* PWM Control Interface
* Optional Current Regulation With 20-μs Fixed Off-Time
* High Output Current per H-Bridge
  2A Maximum Driver Current at 12V and T_A=25°C
  Parallel Mode Available Capable of 4-A Maximum Driver Current at 12V and T_A=25°C
* 4 to 18V Operating Supply Voltage Range
* Low-Current3-μA sleep Mode
* Thermally-Enhanced Surface Mount Package
* Protection Features
  V_M Under voltage Lockout (UVLO)
  Over current Protection (OCP)
  Thermal Shutdown (TSD)
  Fault Condition Indication Pin (nFAULT)

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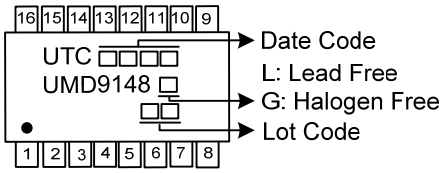
■ ORDERING INFORMATION

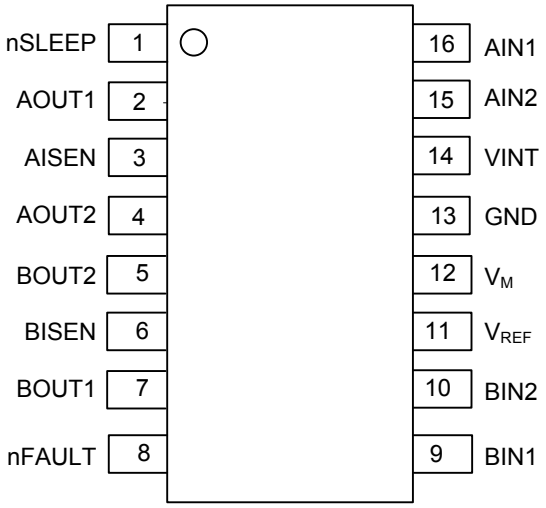
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UMD9148L-P16-R	UMD9148G-P16-R	TSSOP-16	Tape Reel

UMD9148G-P16-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) P16: TSSOP-16 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



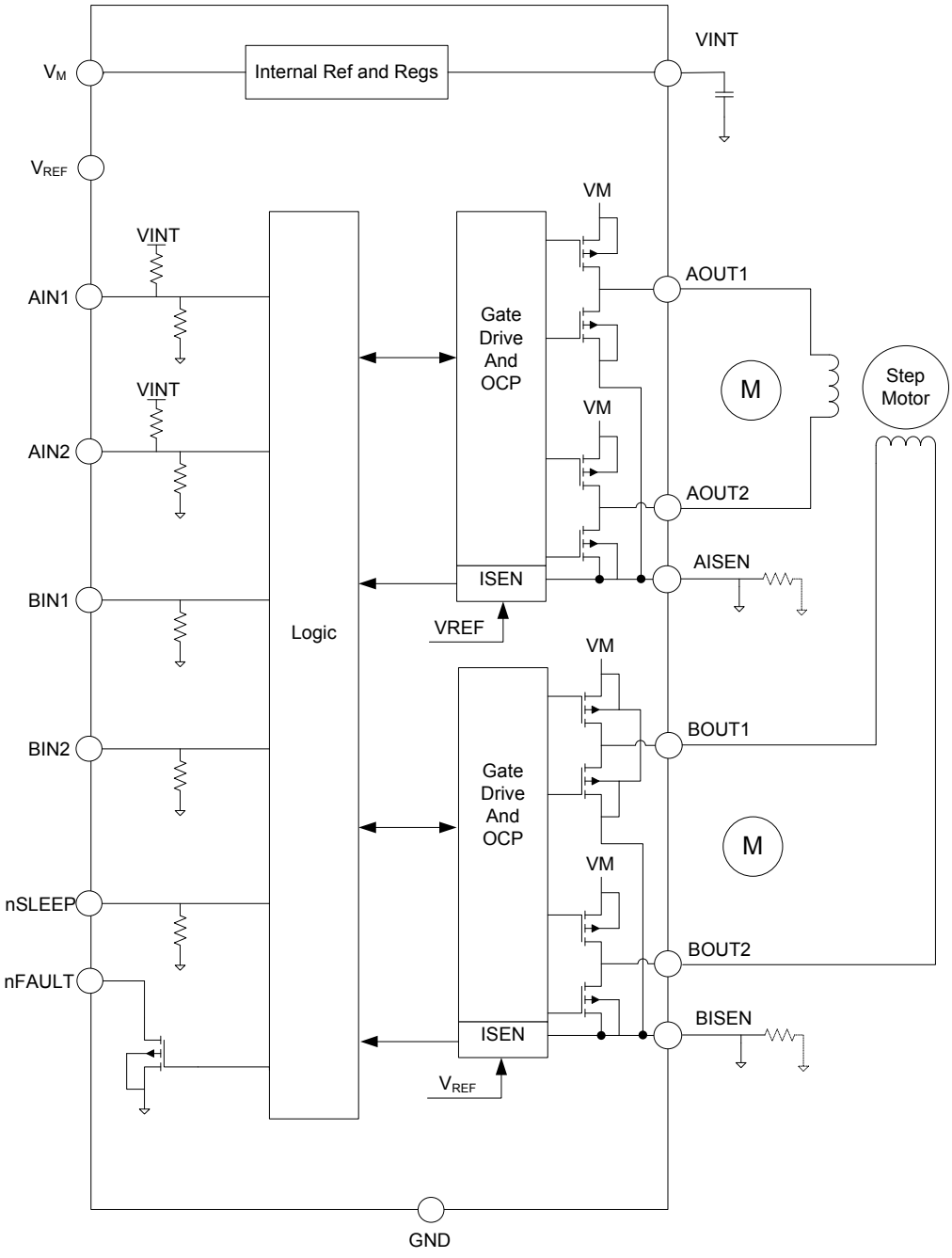
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	nSLEEP	I	Sleep mode input
2	AOUT1	O	Winding A output
3	AISEN	O	Winding A sense
4	AOUT2	O	Winding A output
5	BOUT2	O	Winding B output
6	BISEN	O	Winding B sense
7	BOUT1	O	Winding B output
8	nFAULT	OD	Fault indication pin
9	BIN1	I	Bridge B input 1
10	BIN2	I	Bridge B input 2
11	V_{REF}	I	Full-scale current reference input
12	V_M	PWR	Power supply
13	GND	PWR	Ground
14	VINT	-	Internal regulator
15	AIN2	I	Bridge A input 2
16	AIN1	I	Bridge A input 1

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

(Over operating free-air temperature range referenced with respect to GND, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Power supply Voltage	V_M	-0.3 ~ 20	V
Internal regulator voltage	V_{INT}	-0.3 ~ 3.6	V
Analog input pin voltage	V_{REF}	-0.3 ~ 3.6	V
Control pin voltage(AIN1, AIN2,BIN1,BIN2,nSLEEP,nFAULT)		-0.5 ~ 7	V
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1,BOUT2)		-0.3 ~ V_M+0.6	V
Continuous shunt amplifier input pin voltage (AISEN, BISEN)		-0.6 ~ 0.6	V
Peak drive current (AOUT1, AOUT2,BOUT1,BOUT2,AISEN,BISEN)		Internally limited	A
Operating junction temperature	T_J	-40 ~ +150	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VM operating voltage	V_M		4		18	V
Reference rms voltage range	V_{VREF}		1		3.3	mA
Applied STEP signal	f_{PWM}		0		250	uA
VINT external load current	I_{VINT}				1	mA
Motor rms current per H-bridge	I_{rms}		0		1	A
Operating ambient temperature	T_A		-40		85	ms

■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (V_M, V_{INT})						
V_M operating voltage	V_M		4		18	V
V_M operating supply current	I_{VM}	V_{VM}=12V, excluding winding current, nSLEEP=1	2.5	3.8	5.5	mA
V_M sleep mode supply current	I_{VMQ}	V_{VM}=12V, nSLEEP=0	0.5	1.2	3	uA
Sleep time	t_{SLEEP}	nSLEEP = 0 to sleep mode			1	ms
Wake time	t_{WAKE}	nSLEEP=1 to output transition			1	ms
Power-on time	t_{ON}	V_{VM}>V_{UVLO} rising to output transition			1	ms
V_{INT} voltage		V_{VM}>4V, I_{OUT}=0A to 1mA	3.13	3.3	3.47	V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC-LEVEL INPUTS (BIN1,BIN2,NSLEEP)						
Input logic low voltage	V_{IL}		0		0.7	V
Input logic high voltage	V_{IH}		1.6		5.5	V
Input logic hysteresis	V_{HYS}		100			mV
Input logic low current	I_{IL}	V_{IN}=0V	-1		1	uA
Input logic high current	I_{IH}	V_{IN}=5V	1		30	uA
Pull down resistance	RPD	B_{IN1}, B_{IN2}		200		kΩ
		nSLEEP		500		
Input deglitch time	t_{DEG}	A_{IN1} or A_{IN2}		400		ns
		B_{IN1} or B_{IN2}		200		ns
Propagation delay	t_{PROP}	A_{IN1} or A_{IN2} edge to output change		800		ns
		BIN1 or BIN2 edge to output change		400		ns
TRI-LEVEL INPUTS (AIN1,AIN2)						
Tri-level input logic low voltage	V_{IL}		0		0.7	V
Tri-level input Hi-Z voltage	V_{IZ}			1.1		V
Tri-level input logic high voltage	V_{IH}		1.6		5.5	V
Tri-level input hysteresis	V_{HYS}		100			mV
Tri-level input logic low current	I_{IL}	V_{IN}=0V	-30		-1	uA
Tri-level input logic high current	I_{IH}	V_{IN}=5V	1		30	uA
Tri-level pull down resistance	R_{PD}	To GND		170		kΩ
Tri-level pull up resistance	R_{PU}	To V_{INT}		340		kΩ
CONTROL OUTPUTS (NFAULT)						
Output logic low voltage	V_{OL}	I_O=5mA			0.5	V
Output logic high leakage	I_{OL}	V_O=3.3V	-1		1	uA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2,BOUT1,BOUT2)						
High-side FET on-resistance	$R_{DS(ON)}$	V_{VM}=12V,I=0.5A,T_J=25°C		550		mΩ
		V_{VM}=12V,I=0.5A,T_J=85°C		660		mΩ
Low-side FET on-resistance	$R_{DS(ON)}$	V_{VM}=12V,I=0.5A,T_J=25°C		350		mΩ
		V_{VM}=12V,I=0.5A,T_J=85°C		420		mΩ
Off-state leakage current	I_{OFF}	V_{VM}=5V,T_J=25°C	-1		1	uA
Output rise time	t_{RISE}			60		ns
Output fall time	t_{FALL}			60		ns
Output dead time	t_{DEAD}	Internal dead time		200		ns
PWM CURRENT CONTROL (VREF,AISEN,BISEN)						
Externally applied VREF input current	I_{REF}	V_{REF}=1 to 3.3V			1	uA
X ISEN trip voltage	V_{TRIP}	For 100% current step with V_{REF} =3.3V		500		mV
Current sense blanking time	t_{BLANK}			1.8		us
Current sense amplifier gain	A_{ISENSE}	Reference only		6.6		V/V
Current control constant off time	t_{OFF}			20		us
PROTECTION CIRCUITS						
VM under voltage lock out	V_{UVLO}	V_{VM} falling; UVLO report			2.9	V
		V_{VM} rising; UVLO recovery			3	
Over current protection trip level	I_{OCP}		2			A
Over current deglitch time	t_{DEG}			2.8		us
Over current protection period	t_{OCP}			1.6		ms
Thermal shutdown temperature	T_{TSD}	Die temperature T_J	150	160	180	
Thermal shutdown hysteresis	T_{HYS}	Die temperature T_J		50		

■ DETAILED DESCRIPTION

Overview

The **UMD9148** is an integrated motor driver solution for two DC motors or a bipolar stepper motor. The device integrates two H-bridges that use NMOS low-side drivers and PMOS high-side drivers and current sense regulation circuitry. The **UMD9148** can be powered with a supply range between 4 to 18V and is capable of providing an output current to 1A rms.

A simple PWM interface allows easy interfacing to the controller circuit.

The current regulation uses a fixed off-time (t_{OFF}) PWM scheme. The current regulation trip point is controlled by the value of the sense resistor and the voltage applied to V_{REF}.

A low-power sleep mode is included, which allows the system to save power when not driving the motor.

■ FEATURE DESCRIPTION

PWM Motor Drivers

UMD9148 contains two identical H-bridge motor drivers with current-control PWM circuitry.

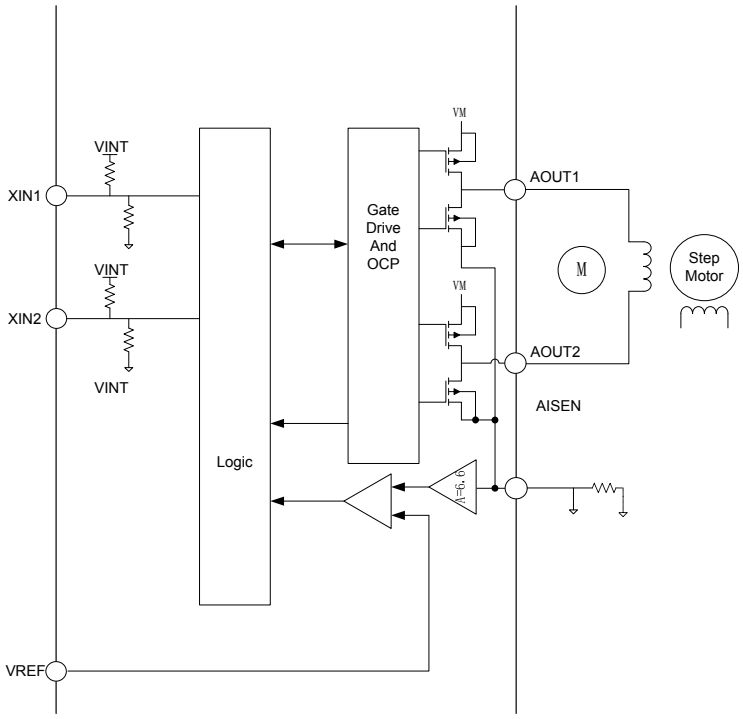


Figure 1. PWM Motor Driver Circuitry

Bridge Control

Table. 1 Shows the logic for the inputs xIN1 and xIN2.

xIN1	xIN2	xOUT1	xOUT2	Function(DCMotor)
0	0	Z	Z	Coast(fast decay)
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake(slow decay)

Pins A_{IN1} and A_{IN2} are tri-level, so when they are left Hi-Z, they are not internally pulled to logic low. When A_{IN1}or A_{IN2} are set to Hi-Z and not in parallel mode, the output driver maintains the previous state.

■ PARALLEL OPERATION

Parallel Operation

The two drivers can be used in parallel to deliver twice the current to a single motor. To enter parallel mode, AIN1 and AIN2 must be left Hi-Z during power-up or when exiting sleep mode (nSLEEP toggling from 0 to 1). BIN1 and BIN2 are used to control the drivers. Tie AISEN and BISEN to a single sense resistor if current control is desired. To exit parallel mode, AIN1 and AIN2 must be driven high or low and the device must be powered-up or exit sleep mode.

Current Regulation

The current through the motor windings is regulated by a fixed-off-time PWM current regulation circuit. With DC brushed motors, current regulation can be used to limit the stall current (which is also the start up current) of the motor.

Current regulation works as follows:

When an H-bridge is enabled, current rises through the winding at a rate dependent on the supply voltage and inductance of the winding. If the current reaches the current chopping threshold, the bridge disables the current for a time t_{OFF} before starting the next PWM cycle. Note that immediately after the current is enabled, the voltage on the xISEN pin is ignored for a period of time (t_{BLANK}) before enabling the current sense circuitry. This blanking time also sets the minimum on-time of the PWM cycle.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor, connected to the xISEN pin, with a reference voltage. The reference voltage is derived from the voltage applied to the V_{REF} pin and it is V_{REF}/ 6.6. The V_{REF} pin can be tied, on board, to the 3.3V–VINT pin, or it can be externally forced to a desired V_{REF} voltage.

Current Recirculation and Decay Modes

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached.

After the chopping current threshold is reached, the drive current is interrupted, but due to the inductive nature of the motor, current must continue to flow for some period of time. This is called recirculation current. To handle this recirculation current, the **UMD9148** H-bridge operates in mixed decay mode.

Mixed decay is a combination of fast and slow decay modes. In fast decay mode, the opposite drivers are turned on to allow the current to decay. If the winding current approaches zero, while in fast decay, the bridge is disabled to prevent any reverse current flow. In slow decay mode, winding current is recirculated by enabling both of the low-side FETs in the bridge. Mixed decay starts with fast decay, then goes to slow decay. In **UMD9148**, the mixed decay ratio is 25% fast decay and 75% slow decay.

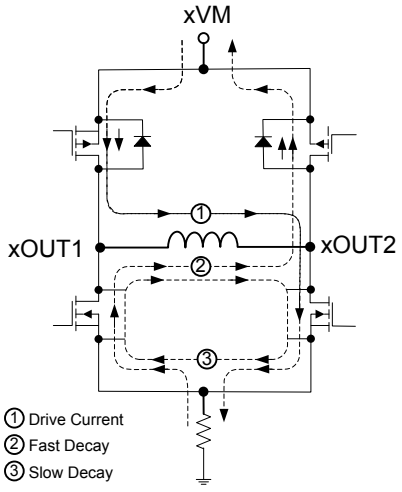


Figure 2. Decay Modes

■ PARALLEL OPERATION (Cont.)

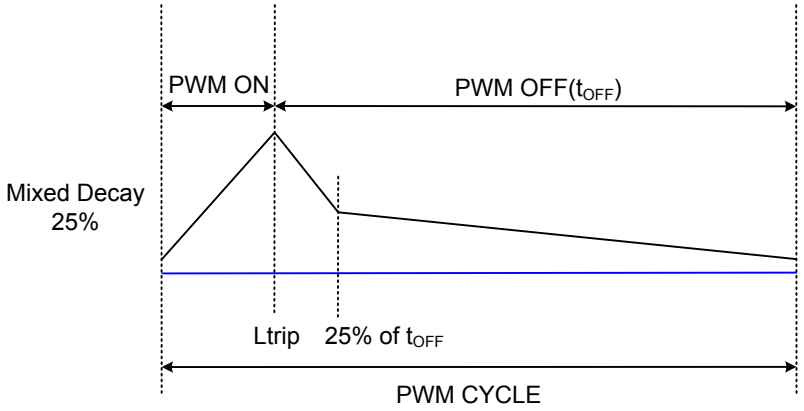


Figure 3. Mixed Decay

Protection Circuits

The **UMD9148** is fully protected against under voltage, over current, and over temperature events.

OCP

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time t_{OCP}, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. The device remains disabled until the retry time t_{RETRY} occurs. The OCP is independent for each H-bridge.

Over current conditions are detected independently on both high-side and low-side devices; that is, a short to ground, supply, or across the motor winding all result in an OCP event. Note that OCP does not use the current sense circuitry used for PWM current control, so OCP functions even without presence of the xISEN resistors.

TSD

If the die temperature exceeds safe limits T_{TSD}, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. After the die temperature has fallen to a safe level, operation automatically resumes. The nFAULT pin is released after operation has resumed.

UVLO

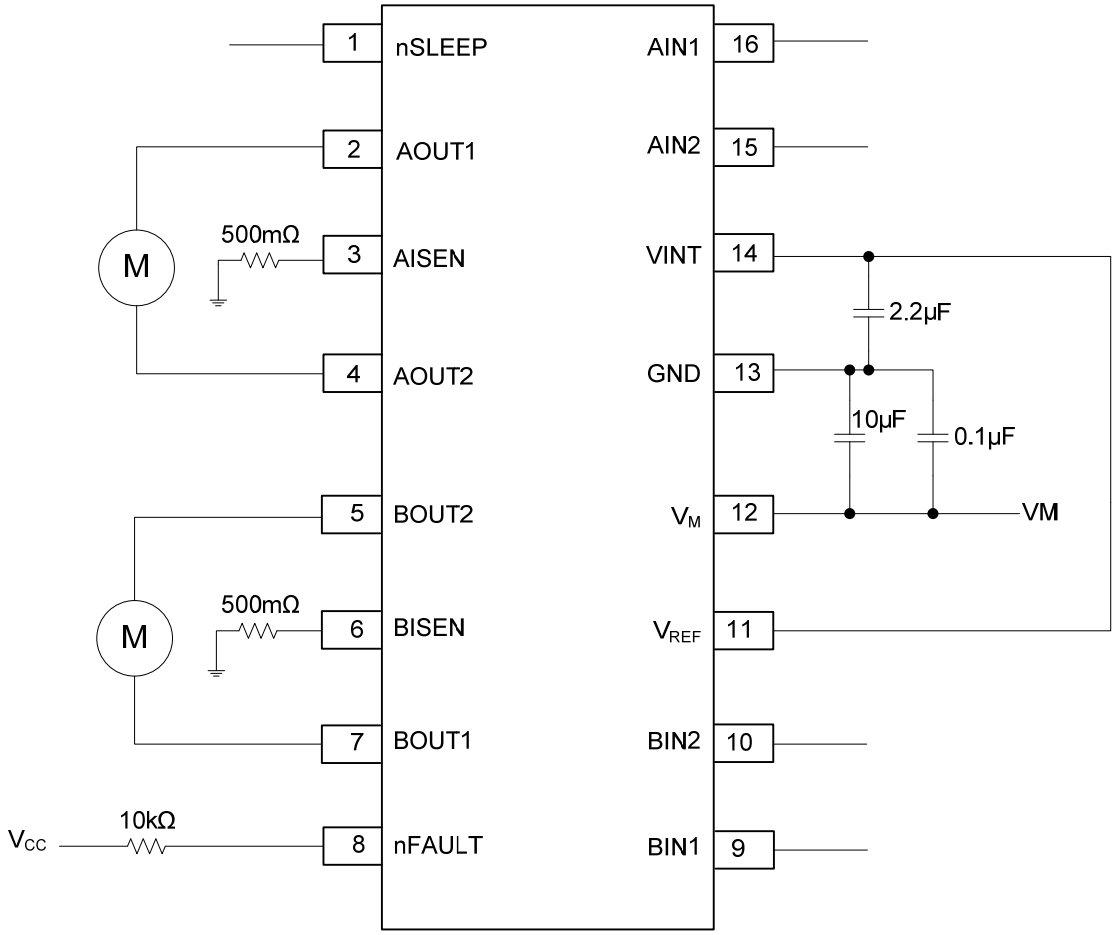
If at any time the voltage on the V_M pin falls below the UVLO falling threshold voltage, VUVLO, all circuitry in the device is disabled, and all internal logic is reset. Operation resumes when V_{VM} rises above the UVLO rising threshold. The nFAULT pin is driven low during an under voltage condition and is released after operation has resumed.

Device Functional Modes

The **UMD9148** is active unless the nSLEEP pin is brought logic low. In sleep mode, the VINT regulator is disabled and the H-bridge FETs are disabled Hi-Z. Note that t_{SLEEP} must elapse after a falling edge on the nSLEEP pin before the device is in sleep mode. The UMD9148 is brought out of sleep mode automatically if nSLEEP is brought logic high. Note that t_{WAKE} must elapse before the output change state after wake-up.

When V_{VM} falls below the V_M UVLO threshold (VUVLO), the output driver, internal logic, and VINT regulator are reset.

■ TYPICAL APPLICATION CIRCUIT



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