

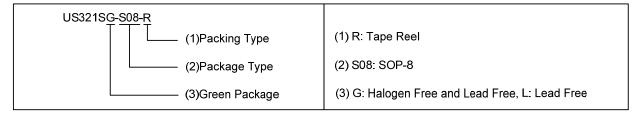
UNISONIC TECHNOLOGIES CO., LTD

US321S Advance **CMOS IC PWM CONTROLLER** DESCRIPTION Featured Device, UTC US321S, is a PWM controller with innovative technology. The controller can work in high voltage with a high voltage MOS in PCB. UTC US321S provides several protection features. It includes a cycle-by-cycle current limit to the power switch; output over-voltage protection; V_{DD} UVLO protection. SOP-8 **FEATURES** * Integrated 650V HV start-up circuit * Low standby power dissipation

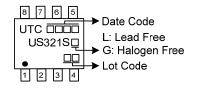
 * Under-voltage lockout (UVLO) with hysteresis
 * Provides complete protection functions Cycle-by-cycle current limit Output over-voltage Protection

ORDERING INFORMATION

Ordering Number		Daekaga	Deaking	
Lead Free	Halogen Free	Package	Packing	
US321SL-S08-R	US321SG-S08-R	SOP-8	Tape Reel	

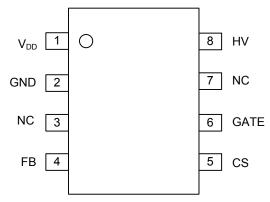


MARKING



US321S

PIN CONFIGURATION

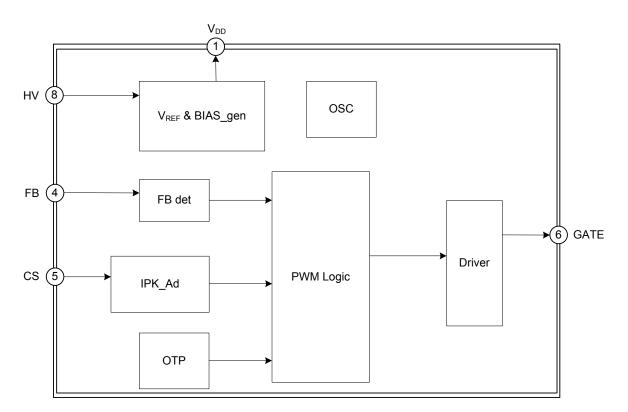


PIN DESCRIPTION

PIN NO.	PIN NAME	I/O (Note 1)	DESCRIPTION	
1	V _{CC}	V _{DD}	Power supply	
2	VB	GND	Power ground	
3, 7	НО	NC	No connection	
4	Vs	FB	Output feedback	
5	HIN	CS	Sensed current of power mos	
6	LIN	GATE	Gate driver for power mos	
8	COM	HV	HV input	

Note: I=Input, O=Output

BLOCK DIAGRAM





■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
HV Pin Voltage	HV	-0.3 ~ 650	V
V _{DD} Pin Voltage	V _{DD}	30	V
FB, CS, GATE Pin Voltage		-0.3 ~ 7	V
Maximum Operating Junction Temperature	TJ	+150	°C
Storage Temperature	T _{STG}	-55 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATINGS	UNIT
Switch Frequency	fsw	40 ~ 60	kHz
Operation Ambient Temperature	T _A	-40 ~ +85	°C
Operating Junction Temperature	TJ	+125	°C

THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	165	°C/W

Note: Not to exceed the maximum junction temperature of the IC, which relates to the operating power of the IC and the thermal resistance of the IC/package as above. The operation power of the IC can be calculated by $P_D = V_{DD_IN} \times I_{IN}$, where V_{DD_IN} represents the input voltage at the V_{DD} pin of the IC and I_{IN} represents the current flow into the V_{DD} pin of the IC.

■ ELECTRICAL CHARACTERISTICS (T_A=25°C unless additional specified)

			r			
SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Supply Voltage						
I_HV			2		mA	
I _{VDD ST}			100	300	uA	
I _{VDD_OP}			800		uA	
IV_{DD_Q}			200		uA	
V_{DD_ON}			7.5		V	
V_{DD_OFF}			7		V	
V _{DD_OVP}			28		V	
V _{DD_CLAMP}			30		V	
V _{DD_reg1}		11.8	12	12.2	V	
V_{FB_REF}		1.97	2	2.03	V	
V_{FB_OVP}			2.4		V	
V_{FB_OLP}			1.87		V	
T_LEB			350		ns	
V_IPK		0.5	0.55	0.6	V	
V_AOCP			0.9		V	
T _{OFF_MIN}			16		uS	
T _{OFF_MAX}			1.4		mS	
T _{ON_MAX}			12		uS	
T_ _{AUR}			500		mS	
	I_HV IVDD ST IVDD_OP IVDD_OP VDD_ON VDD_OFF VDD_OFF VDD_CLAMP VDD_CLAMP VDD_reg1 VFB_REF VFB_OVP VFB_OVP VFB_OVP VFB_OVP VFB_OLP T_LEB V_IPK V_AOCP	I_HV Ivdd_op Ivdd_op IV_DD_Q V_DD_ON V_DD_OFF V_DD_OFF V_DD_CLAMP V_DD_reg1 VFB_REF VFB_OVP VFB_OVP VFB_OVP VFB_OVP VFB_OVP T_LEB V_IPK V_AOCP T_OFF_MAX T_ON_MAX	I_HV I Ivdd_op I IVdd_op I IVdd_op I Vbd_on I Vbd_on I Vbd_orff I Vbd_ovp I VFB_REF I VFB_OVP I VFB_OVP I VFB_OVP I V_IPK 0.5 V_AOCP I Toff_MAX I Ton_MAX I	I_HV 2 Ivdd St 100 Ivdd OP 800 IVdd OP 800 IVdd OP 200 Vdd OP 200 Vdd OP 7.5 Vdd OFF 7 Vdd OVP 28 Vdd OVP 24 VFB_REF 1.97 VFB_OVP 2.4 VFB_OVP 2.4 VFB_OUP 1.87 T 0.5 V_IPK 0.5 V_AOCP 0.9 TOFF_MAX 1.4 TON MAX 12	I_HV 2 Ivdd str 100 300 Ivdd op 800 100 300 Ivdd op 800 200 200 Vdd op 7.5 28 28 Vdd ovp 28 30 200 Vdd ovp 24 12 12 VFB_OVP 2.4 350 350 V_IPK 0.5 0.55 0.6 V_AOCP 0.9 116 10 TOFF_MAX 1.4 14 14	



FUNCTIONAL DESCRIPTION

Refer to both the Block Diagram and a reference design circuit for the following discussions. All parameters mentioned below are typical values.

Start-up Circuit

Applying power to the input port in Figure 4, initiates the operation. V_{DD} voltage is lower than V_{DD_OFF} pwm logic is off and output voltage cannot keep at a constant value.

After V_{DD} voltage is over V_{DD_ON} normal operation starts. PWM logic is running and output voltage goes to pre-set value gradually.

Output voltage Setting

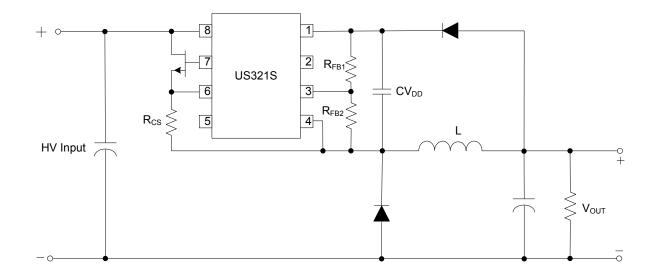
Output voltage can be set by two divided-resistors. Reference voltage in the chip is 2V. The output voltage can be calculated by

 $V_{OUT} = (1 + R_{FB1}/R_{FB2}) \times 2 + V_{D1}.$

 V_{D1} is forward voltage drop of a diode, 0.6V typically.



TYPICAL APPLICATION CIRCUIT



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