



UPG15N60

Preliminary

Insulated Gate Bipolar Transistor

600V, SMPS N-CHANNEL IGBT

DESCRIPTION

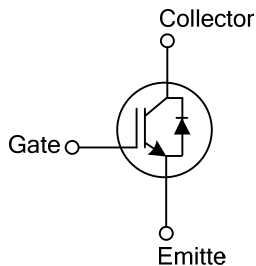
This UPG15N60 is a Insulated Gate Bipolar Transistor (IGBT) features a robust and cost effective Non-Punch Through (NPT) Trench construction, and provides superior performance in demanding switching applications.

Offering both low on state voltage and minimal switching loss, the IGBT is well suited for motor drive control and other hard switching applications.

FEATURES

- * $V_{CE(SAT)} \leq 1.7V$ @ $I_C=15A$, $V_{GE}=15V$
- * 600V Switching SOA Capability
- * Low Saturation Voltage Resulting in Low Conduction Loss
- * Low Switching Loss in Higher Frequency Applications
- * 5 μs Short Circuit Capability
- * Excellent Current

SYMBOL



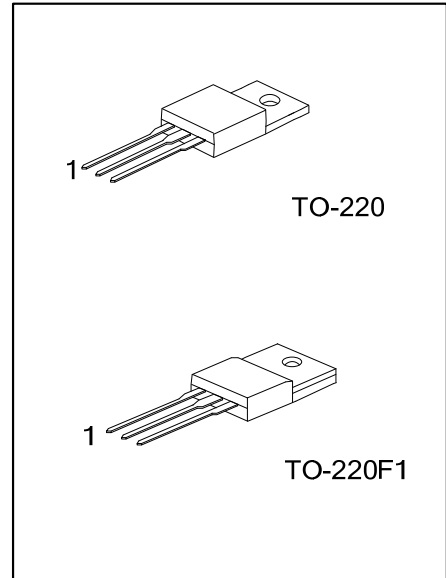
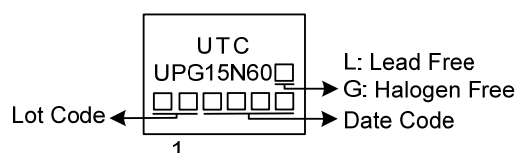
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UPG15N60L-TA3-T	UPG15N60G-TA3-T	TO-220	G	C	E	Tube
UPG15N60L-TF1-T	UPG15N60G-TF1-T	TO-220F1	G	C	E	Tube

Note: Pin Assignment: G: Gate C: Collector E: Emitter

<p>UPG15N60G-TA3-T</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) T: Tube</p> <p>(2) TA3: TO-220, TF1: TO-220F1</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Collector-Emitter Voltage	V_{CES}	600	V
Gate to Emitter Voltage Continuous	V_{GES}	± 20	V
Continuous Collector Current	I_C	$T_C=25^{\circ}\text{C}$	A
		$T_C=100^{\circ}\text{C}$	A
Collector Current Pulsed (Note 2)	I_{CM}	60	A
Peak Diode Recovery dv/dt (Note 3)	dv/dt	6.4	V/ns
Power Dissipation	P_D	TO-220	W
		TO-220F1	W
Junction Temperature	T_J	$-55 \sim +150$	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	$-55 \sim +150$	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $I_F \leq 8\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{CC} \leq BV_{CES}$, Starting $T_J=25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Case	θ_{JC}	TO-220	$^{\circ}\text{C}/\text{W}$
		TO-220F1	$^{\circ}\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C=250\mu\text{A}$, $V_{GE}=0\text{V}$	600			V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE}=600\text{V}$, $V_{GE}=0\text{V}$			200	μA
Gate to Emitter Leakage Current	I_{GES}	$V_{GE}=20\text{V}$, $V_{CE}=0\text{V}$			± 400	nA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C=15\text{A}$, $V_{GE}=15\text{V}$	$T_J=25^{\circ}\text{C}$	2	2.5	V
			$T_J=125^{\circ}\text{C}$	2.4		V
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C=250\mu\text{A}$, $V_{CE}=V_{GE}$	4.0	5.7	7.0	V
Input Capacitance	C_{IES}	$V_{CE}=30\text{V}$, $V_{GE}=0\text{V}$, $f=1\text{MHz}$		1230		pF
Output Capacitance	C_{OES}			160		pF
Reverse Transfer Capacitance	C_{RES}			28		pF
Total Gate Charge	Q_G	$V_{CE}=480\text{V}$, $V_{GE}=15\text{V}$, $I_C=15\text{A}$		48		nC
Gate-Emitter Charge	Q_{GE}			15		nC
Gate-Collector Charge	Q_{GC}			23		nC
Current Turn-On Delay Time	$t_{D(ON)}$	$V_{CE}=100\text{V}$, $V_{GE}=15\text{V}$, $I_C=15\text{A}$, $R_G=24\Omega$		32		ns
Current Rise Time	t_R			38		ns
Current Turn-Off Delay Time	$t_{D(OFF)}$			100		ns
Current Fall Time	t_F			58		ns

SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS

Forward Voltage Drop	V_{FM}	$I_F=12\text{A}$	$T_J=25^{\circ}\text{C}$		1.9	2.6	V
			$T_J=125^{\circ}\text{C}$		1.5		V
Reverse Recovery Time	t_{rr}	$I_F=12\text{A}$, $di/dt=100\text{A}/\mu\text{S}$, $V_{CC}=50\text{V}$		75			ns
Reverse Recovery Charge	Q_{rr}			170			nC

Note: Pulse Test: Pulse width $\leq 50\mu\text{s}$.

■ TEST CIRCUIT AND WAVEFORMS

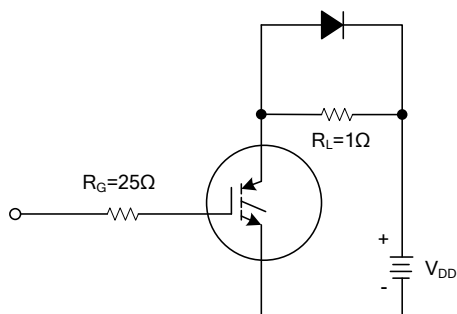


Fig 1. INDUCTIVE SWITCHING TEST CIRCUIT

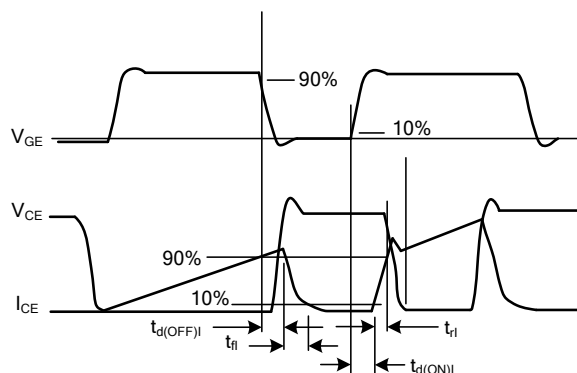


Fig 2. SWITCHING TEST WAVEFORMS

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