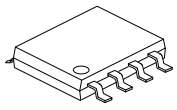
2-BIT BIDIRECTIONAL VOLTAGE-LEVEL TRANSLATOR WITH AUTO DIRECTION SENSING



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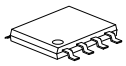


MSOP-8

CDFN2030-8

■ DESCRIPTION

The **UTXB0102** device is a 2-bit noninverting translator that uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2V to 3.6V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65V to 5.5V. This allows for universal low-voltage bidirectional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, and 5V voltage nodes. V_{CCA} must not exceed V_{CCB}.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

This device is fully specified for partial-power-down applications using I_{OFF}. The I_{OFF} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

OE must be tied to GND through a pull-down resistor to assure the high-impedance state during power up or power down; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

■ FEATURES

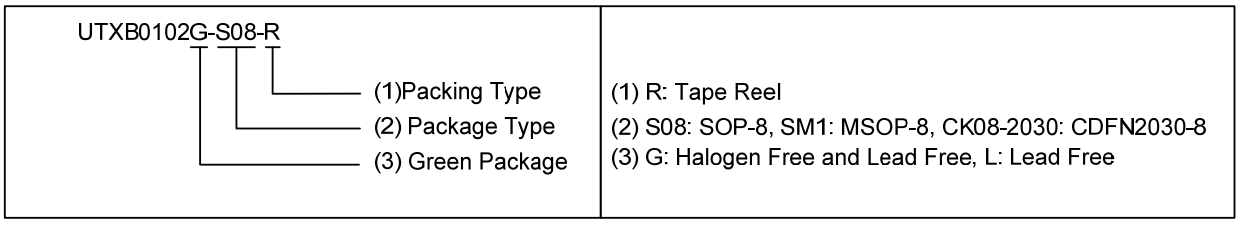
* 1.2V to 3.6V on A Port and 1.65V to 5.5V on B Port ($V_{CCA} \leq V_{CCB}$)
* V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, All Outputs Are in the High-Impedance State
* OE Input Circuit Referenced to V_{CCA}
* Low Power Consumption, 4μA Max I_{CC}
* I_{OFF} Supports Partial-Power-Down Mode Operation

■ APPLICATION

* Handset
* Smartphone
* Tablet
* Desktop PC

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UTXB0102L-S08-R	UTXB0102G-S08-R	SOP-8	Tape Reel
UTXB0102L-SM1R	UTXB0102G-SM1-R	MSOP-8	Tape Reel
UTXB0102L-CK08-2030-R	UTXB0102G-CK08-2030-R	CDFN2030-8	Tape Reel



■ MARKING

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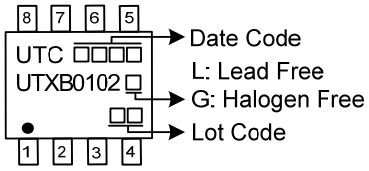
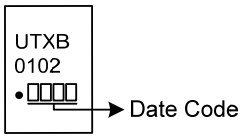
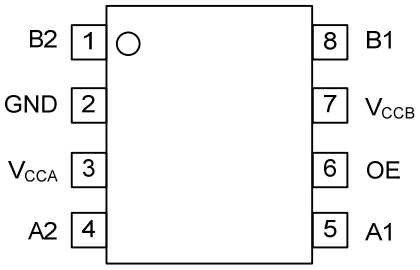
	

■ PIN CONFIGURATION



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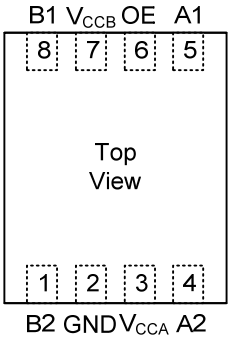


CDFN2030-8

■ PIN DESCRIPTION

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	B2	I/O	Input/output B2. Referenced to V_{CCB}
2	GND		Ground
3	V_{CCA}		A-Port supply voltage 1.2V ≤ V_{CCA} ≤ 3.6V, V_{CCA} ≤ V_{CCB}
4	A2	I/O	Input/output A2. Referenced to V_{CCA}
5	A1	I/O	Input/output A1. Referenced to V_{CCA}
6	OE	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}
7	V_{CCB}		B-Port supply voltage 1.65V ≤ V_{CCB} ≤ 5.5V
8	B1	I/O	Input/output B1. Referenced to V_{CCB}

Note: I=Input, O=Output, I/O=Input and Output.

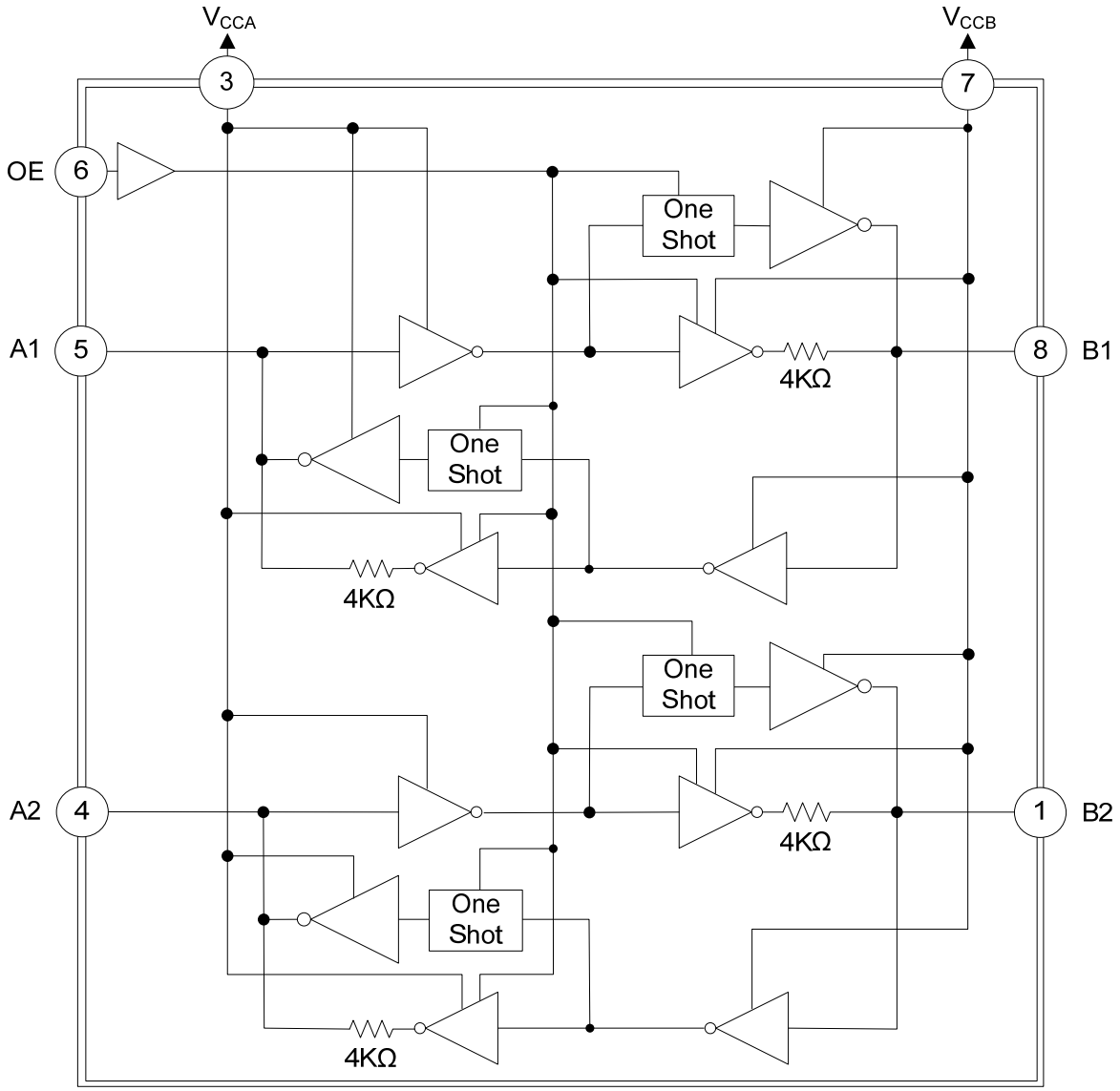
■ FUNCTION TABLE

SUPPLY VOLTAGE		INPUTS	INPUTS/OUTPUT	
V_{CCA}	V_{CCB}	OE	An	Bn
1.2V ~ V_{CCB}	1.65V ~ 5.5V	L	Z	Z
1.2V ~ V_{CCB}	1.65V ~ 5.5V	H	Input or Output	Output or Input
GND (Note 2)	GND (Note 2)	X	Z	Z

Notes: 1. H = High voltage level；L = Low voltage level；Z : High impedance OFF-state；X = Don't care.

2. When either V_{CCA} or V_{CCB} is at GND level, the device goes into Power-down mode.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply voltage		V_{CCA}	-0.5 ~ 4.6	V
Supply voltage		V_{CCB}	-0.5 ~ 6.5	V
Input voltage	A Port	V_{IN}	-0.5 ~ 4.6	V
	B port		-0.5 ~ 6.5	V
Voltage range applied to any output in the high-impedance or power-off state	A port	V_{OUT}	-0.5 ~ 4.6	V
	B Port		-0.5 ~ 6.5	V
Voltage range applied to any output in the high or low state	A Port	V_{OUT}	-0.5 ~ V_{CCA}+0.5	V
	B Port		-0.5 ~ V_{CCB}+0.5	V
Input clamp current	V_{IN}<0	I_{IK}	-50	mA
Output clamp current	V_{OUT}<0	I_{OK}	-50	mA
Continuous output current		I_{OUT}	±50	mA
Continuous current through V_{CCA}, V_{CCB}, or GND		I_{CC} / I_{GND}	±100	mA
Storage Temperature		T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS (Unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Supply Voltage		V_{CCA}			1.2		3.6	V
Supply Voltage		V_{CCB}			1.65		5.5	V
Input Voltage		V_{IN}			0		V_{CCI}	V
Output Voltage	A Port	V_{OUT}	V_{CCA}=1.2V~3.6V, V_{CCB}=1.65V~5.5V		0		3.6	V
	B Port		V_{CCA}=1.2V~3.6V, V_{CCB}=1.65V~5.5V		0		5.5	V
High-Level Input Voltage	Data Inputs	V_{IH}	V_{CCA}=1.2V~3.6V, V_{CCB}=1.65V~5.5V		V_{CCI} ×0.65 (Note 3)		V_{CCI}	V
	OE				V_{CCA} ×0.65		5.5	V
Low-Level Input Voltage	Data Inputs	V_{IL}	V_{CCA}=1.2V~3.6V, V_{CCB}=1.65V~5.5V		0		V_{CCI} ×0.35 (Note 3)	V
	OE				0		V_{CCA} ×0.35	V
Input Transition Rise or Fall Rate	A Port Inputs	Δt/Δv	V_{CCA}=1.2V~3.6V	V_{CCB}=1.65V~5.5V			40	ns/V
	B Port Inputs			V_{CCB}=1.65V~1.95V			40	ns/V
				V_{CCB}=4.5V~5.5V			30	ns/V
Operating Temperature		T_A			-40		+125	°C

Notes: 1. The A and B sides of an unused data I/O pair must be held in the same state, that is, both at V_{CCI} or both at GND.
2. V_{CCA} must be less than or equal to V_{CCB} and must not exceed 3.6V.
3. V_{CCI} is the supply voltage associated with the input port.

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Port A Output High Voltage		V_{OHA}	V_{CCA}=1.2V, I_{OH}=-20μA			1.1		V
			V_{CCB}=1.4V~3.6V, I_{OH}=-20μA		V_{CCA} -0.4			V
Port A Output Low Voltage		V_{OLA}	V_{CCA}=1.2V, I_{OL}=20μA			0.3		V
			V_{CCB}=1.4V~3.6V, I_{OL}=20μA				0.4	V
Port B Output High Voltage		V_{OHB}	V_{CCB}=1.65V~5.5V, I_{OH}=-20μA		V_{CCB} -0.4			V
Port B Output Low Voltage		V_{OLB}	V_{CCB}=1.65V~5.5V, I_{OL}=20μA				0.4	V
Input Leakage Current	OE	$I_{I(LEAK)}$	V_I=V_{CCI} or GND, V_{CCA}=1.2V~3.6V, V_{CCB}=1.65V~5.5V				±1	μA
Power OFF Leakage Current	A Port	I_{OFF}	V_I or V_{OUT}=0~3.6V, V_{CCA}=0V, V_{CCB}=0V~5.5V				±1	μA
	B Port		V_I or V_{OUT}=0~5.5V, V_{CCA}=0V~3.6V, V_{CCB}=0V				±1	μA
High-Impedance State Output Current	A or B Port	I_{OZ}	V_{CCA}=1.2V~3.6V, V_{CCB}=1.65V~5.5V, OE=GND				±1	μA
Quiescent Supply Current		I_{CCA}	V_I=V_{CCI} or GND I_O=0A	V_{CCA}=1.2V, V_{CCB}=1.65V~5.5V		0.06		μA
				V_{CCA}=1.4V~3.6V, V_{CCB}=1.65V~5.5V			3	μA
				V_{CCA}=3.6V, V_{CCB}=0V			2	μA
				V_{CCA}=0V, V_{CCB}=5.5V			-2	μA
		I_{CCB}		V_{CCA}=1.2V, V_{CCB}=1.65V~5.5V		3.4		μA
				V_{CCA}=1.4V~3.6V, V_{CCB}=1.65V~5.5V			5	μA
				V_{CCA}=3.6V, V_{CCB}=0V			-2	μA
				V_{CCA}=0V, V_{CCB}=5.5V			2	μA
		I_{CCA}+I_{CCB}		V_{CCA}=1.2V, V_{CCB}=1.65V~5.5V		3.5		μA
				V_{CCA}=1.4V~3.6V, V_{CCB}=1.65V~5.5V			8	μA
		I_{CCZA}		V_{CCA}=1.2V, V_{CCB}=1.65V~5.5V OE=GND		0.05		μA
				V_{CCA}=1.2V, V_{CCB}=1.4V~3.6V OE=GND			3	μA
		I_{CCZB}		V_{CCA}=1.2V, V_{CCB}=1.65V~5.5V OE=GND		3.3		μA
				V_{CCA}=1.2V, V_{CCB}=1.4V~3.6V OE=GND			5	μA
Input Capacitance	OE	C_{IN}	V_{CCA}=1.2V~3.6V, V_{CCB}=1.65V~5.5V			2.5		pF
Output Capacitance	A Port	C_{IO}				5		pF
	B Port					11		pF

Notes: 1. V_{CCI} is the supply voltage associated with the input port.
2. V_{CCO} is the supply voltage associated with the output port.
3. V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6V.

■ SWITCHING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delay From Input (A) to Output (B)	t_{PD}	V_{CCA}=1.2V	V_{CCB}=1.8V		7.9		ns
			V_{CCB}=2.5V		6.7		ns
			V_{CCB}=3.3V		6.3		ns
			V_{CCB}=5V		6.5		ns
		V_{CCA}=1.5V±0.1V	V_{CCB}=1.8V±0.15V	1.4		13.9	ns
			V_{CCB}=2.5V±0.2V	1.2		11.1	ns
			V_{CCB}=3.3V±0.3V	1.1		11	ns
			V_{CCB}=5V±0.5V	0.8		10.9	ns
		V_{CCA}=1.8V±0.15V	V_{CCB}=1.8V±0.15V	1.6		12	ns
			V_{CCB}=2.5V±0.2V	1.4		8.7	ns
			V_{CCB}=3.3V±0.3V	1.3		7.8	ns
			V_{CCB}=5V±0.5V	1.2		7.5	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=2.5V±0.2V	1.1		7.3	ns
			V_{CCB}=3.3V±0.3V	1.0		6.2	ns
			V_{CCB}=5V±0.5V	0.9		5.7	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=3.3V±0.3V	0.9		5.7	ns
			V_{CCB}=5V±0.5V	0.8		5.0	ns
Propagation Delay From Input (B) to Output (A)		V_{CCA}=1.2V	V_{CCB}=1.8V		8.4		ns
			V_{CCB}=2.5V		7.4		ns
			V_{CCB}=3.3V		7.0		ns
			V_{CCB}=5V		6.8		ns
		V_{CCA}=1.5V±0.1V	V_{CCB}=1.8V±0.15V	0.9		15.2	ns
			V_{CCB}=2.5V±0.2V	0.7		13	ns
			V_{CCB}=3.3V±0.3V	0.4		12.7	ns
			V_{CCB}=5V±0.5V	0.3		14.7	ns
		V_{CCA}=1.8V±0.15V	V_{CCB}=1.8V±0.15V	1.5		13	ns
			V_{CCB}=2.5V±0.2V	1.3		9.4	ns
			V_{CCB}=3.3V±0.3V	1.0		8.6	ns
			V_{CCB}=5V±0.5V	0.9		8.1	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=2.5V±0.2V	1.2		7.6	ns
			V_{CCB}=3.3V±0.3V	1.1		6.1	ns
			V_{CCB}=5V±0.5V	0.9		5.4	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=3.3V±0.3V	1.0		5.9	ns
			V_{CCB}=5V±0.5V	0.9		5.5	ns
Enable Time From Input (OE) to Output (A or B)	t_{en}	V_{CCA}=1.2V	V_{CCB}=1.8V		1		µs
			V_{CCB}=2.5V		1		µs
			V_{CCB}=3.3V		1		µs
			V_{CCB}=5V		1		µs
		V_{CCA}=1.5V±0.1V	V_{CCB}=1.8V±0.15V			1	µs
			V_{CCB}=2.5V±0.2V			1	µs
			V_{CCB}=3.3V±0.3V			1	µs
			V_{CCB}=5V±0.5V			1	µs
		V_{CCA}=1.8V±0.15V	V_{CCB}=1.8V±0.15V			1	µs
			V_{CCB}=2.5V±0.2V			1	µs
			V_{CCB}=3.3V±0.3V			1	µs
			V_{CCB}=5V±0.5V			1	µs
		V_{CCA}=2.5V±0.2V	V_{CCB}=2.5V±0.2V			1	µs
			V_{CCB}=3.3V±0.3V			1	µs
			V_{CCB}=5V±0.5V			1	µs
		V_{CCA}=3.3V±0.3V	V_{CCB}=3.3V±0.3V			1	µs
			V_{CCB}=5V±0.5V			1	µs

■ SWITCHING CHARACTERISTICS (Cont.)

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Disable Time From Input (OE) to Output (A)		t_{dis}	V_{CCA}=1.2V	V_{CCB}=1.8V		28		ns
				V_{CCB}=2.5V		25		ns
				V_{CCB}=3.3V		24		ns
				V_{CCB}=5V		24		ns
			V_{CCA}=1.5V±0.1V	V_{CCB}=1.8V±0.15V	5.9		41	ns
				V_{CCB}=2.5V±0.2V	5.7		35.9	ns
				V_{CCB}=3.3V±0.3V	5.6		33	ns
				V_{CCB}=5V±0.5V	5.7		32.4	ns
			V_{CCA}=1.8V±0.15V	V_{CCB}=1.8V±0.15V	5.9		41	ns
				V_{CCB}=2.5V±0.2V	5.1		31.3	ns
				V_{CCB}=3.3V±0.3V	5.0		29.3	ns
				V_{CCB}=5V±0.5V	5.0		27.4	ns
			V_{CCA}=2.5V±0.2V	V_{CCB}=2.5V±0.2V	5.1		31.3	ns
				V_{CCB}=3.3V±0.3V	4.6		25.2	ns
				V_{CCB}=5V±0.5V	4.6		23.2	ns
			V_{CCA}=3.3V±0.3V	V_{CCB}=3.3V±0.3V	4.6		25.2	ns
				V_{CCB}=5V±0.5V	4.6		22.1	ns
Disable Time From Input (OE) to Output (B)			V_{CCA}=1.2V	V_{CCB}=1.8V		30		ns
				V_{CCB}=2.5V		27		ns
				V_{CCB}=3.3V		26		ns
				V_{CCB}=5V		26		ns
			V_{CCA}=1.5V±0.1V	V_{CCB}=1.8V±0.15V	5.4		40.3	ns
				V_{CCB}=2.5V±0.2V	4.9		32.8	ns
				V_{CCB}=3.3V±0.3V	4.8		30	ns
				V_{CCB}=5V±0.5V	4.9		29.5	ns
			V_{CCA}=1.8V±0.15V	V_{CCB}=1.8V±0.15V	5.4		40.3	ns
				V_{CCB}=2.5V±0.2V	4.4		30.8	ns
				V_{CCB}=3.3V±0.3V	4.2		27.9	ns
				V_{CCB}=5V±0.5V	4.3		26.3	ns
			V_{CCA}=2.5V±0.2V	V_{CCB}=2.5V±0.2V	4.4		30.8	ns
				V_{CCB}=3.3V±0.3V	3.8		26	ns
				V_{CCB}=5V±0.5V	3.9		23.9	ns
			V_{CCA}=3.3V±0.3V	V_{CCB}=3.3V±0.3V	3.8		26	ns
				V_{CCB}=5V±0.5V	3.4		23.2	ns
Rise and Fall Time	A Port Rise And Fall Times	t_{rA}, t_{fA}	V_{CCA}=1.2V	V_{CCB}=1.8V		5.2		ns
				V_{CCB}=2.5V		5.2		ns
				V_{CCB}=3.3V		5.2		ns
				V_{CCB}=5V		5.2		ns
			V_{CCA}=1.5V±0.1V	V_{CCB}=1.8V±0.15V	1.4		6.1	ns
				V_{CCB}=2.5V±0.2V	1.4		6.1	ns
				V_{CCB}=3.3V±0.3V	1.4		6.1	ns
				V_{CCB}=5V±0.5V	1.4		6.1	ns
			V_{CCA}=1.8V±0.15V	V_{CCB}=1.8V±0.15V	1.0		5.2	ns
				V_{CCB}=2.5V±0.2V	1.1		5.1	ns
				V_{CCB}=3.3V±0.3V	1.1		5.1	ns
				V_{CCB}=5V±0.5V	1.1		5.1	ns
			V_{CCA}=2.5V±0.2V	V_{CCB}=2.5V±0.2V	0.8		4.0	ns
				V_{CCB}=3.3V±0.3V	0.8		4.0	ns
				V_{CCB}=5V±0.5V	0.8		4.0	ns
			V_{CCA}=3.3V±0.3V	V_{CCB}=3.3V±0.3V	0.7		3.5	ns
				V_{CCB}=5V±0.5V	0.7		3.5	ns

■ SWITCHING CHARACTERISTICS (Cont.)

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Rise and Fall Time	B Port Rise And Fall Times	t_{rB}, t_{fB}	V_{CCA}=1.2V	V_{CCB}=1.8V		3.1		ns
				V_{CCB}=2.5V		2.5		ns
				V_{CCB}=3.3V		2.2		ns
				V_{CCB}=5V		2.1		ns
			V_{CCA}=1.5V±0.1V	V_{CCB}=1.8V±0.15V	0.9		5.5	ns
				V_{CCB}=2.5V±0.2V	0.6		4.2	ns
				V_{CCB}=3.3V±0.3V	0.5		3.8	ns
				V_{CCB}=5V±0.5V	0.4		3.7	ns
			V_{CCA}=1.8V±0.15V	V_{CCB}=1.8V±0.15V	0.9		5.5	ns
				V_{CCB}=2.5V±0.2V	0.6		4.2	ns
				V_{CCB}=3.3V±0.3V	0.5		3.8	ns
				V_{CCB}=5V±0.5V	0.4		3.7	ns
			V_{CCA}=2.5V±0.2V	V_{CCB}=2.5V±0.2V	0.7		4.0	ns
				V_{CCB}=3.3V±0.3V	0.5		3.8	ns
				V_{CCB}=5V±0.5V	0.4		3.7	ns
			V_{CCA}=3.3V±0.3V	V_{CCB}=3.3V±0.3V	0.5		3.3	ns
				V_{CCB}=5V±0.5V	0.4		3.7	ns
Data Rate		f_{data}	V_{CCA}=1.2V, V_{CCB}=1.8V~5V			20		Mbps
			V_{CCA}=1.5V±0.1V, V_{CCB}=1.65V~5.5V				40	Mbps
			V_{CCA}=1.8V±0.15V, V_{CCB}=1.65V~5.5V				60	Mbps
			V_{CCA}=2.5V±0.2V, V_{CCB}=2.3V~5.5V				100	Mbps
			V_{CCA}=3.3V±0.3V, V_{CCB}=3.0V~5.5V				100	Mbps
Pulse Duration	Data Inputs	t_W	V_{CCA}=1.2V, V_{CCB}=1.8V~5V			50		ns
			V_{CCA}=1.5V±0.1V, V_{CCB}=1.65V~5.5V		25			ns
			V_{CCA}=1.8V±0.15V, V_{CCB}=1.65V~5.5V		17			ns
			V_{CCA}=2.5V±0.2V, V_{CCB}=2.3V~5.5V		10			ns
			V_{CCA}=3.3V±0.3V, V_{CCB}=3.0V~5.5V		10			ns

■ OPERATING CHARACTERISTICS (Unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	A Port Input B Port Output	C_{PDA}	C_L=0, f=10MHz t_r=t_f=1nS OE=V_{CCA} (Output Enabled)	V_{CCA}=1.2V V_{CCB}=5V		7.8		pF
				V_{CCA}=1.2V V_{CCB}=1.8V		8.0		pF
				V_{CCA}=1.5V V_{CCB}=1.8V		8.0		pF
				V_{CCA}=1.8V V_{CCB}=1.8V		7.0		pF
				V_{CCA}=2.5V V_{CCB}=2.5V		7.0		pF
				V_{CCA}=2.5V V_{CCB}=5V		8.0		pF
				V_{CCA}=3.3V V_{CCB}=3.3~5V		8.0		pF
	B Port Input A Port Output			V_{CCA}=1.2V V_{CCB}=5V		12		pF
				V_{CCA}=1.2V V_{CCB}=1.8V		11		pF
				V_{CCA}=1.5V V_{CCB}=1.8V		11		pF
				V_{CCA}=1.8V V_{CCB}=1.8V		11		pF
				V_{CCA}=2.5V V_{CCB}=2.5V		11		pF
				V_{CCA}=2.5V V_{CCB}=5V		11		pF
				V_{CCA}=3.3V V_{CCB}=3.3~5V		11		pF
	A Port Input B Port Output		C_L=0, f=10MHz t_r=t_f=1nS OE=GND (Output Disabled)	V_{CCA}=1.2V V_{CCB}=5V		0.01		pF
				V_{CCA}=1.2V V_{CCB}=1.8V		0.01		pF
				V_{CCA}=1.5V V_{CCB}=1.8V		0.01		pF
				V_{CCA}=1.8V V_{CCB}=1.8V		0.01		pF
				V_{CCA}=2.5V V_{CCB}=2.5V		0.01		pF
				V_{CCA}=2.5V V_{CCB}=5V		0.01		pF
				V_{CCA}=3.3V V_{CCB}=3.3~5V		0.01		pF

■ OPERATING CHARACTERISTICS (Cont.)

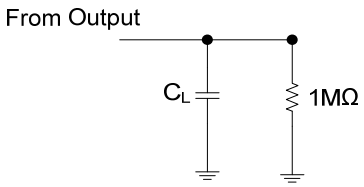
PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	B Port Input A Port Output	C_{PDA}	C_L=0, f=10MHz t_r=t_f=1nS OE=GND (Output Disabled)	V_{CCA}=1.2V V_{CCB}=5V		0.01		pF
				V_{CCA}=1.2V V_{CCB}=1.8V		0.01		pF
				V_{CCA}=1.5V V_{CCB}=1.8V		0.01		pF
				V_{CCA}=1.8V V_{CCB}=1.8V		0.01		pF
				V_{CCA}=2.5V V_{CCB}=2.5V		0.01		pF
				V_{CCA}=2.5V V_{CCB}=5V		0.01		pF
				V_{CCA}=3.3V V_{CCB}=3.3~5V		0.01		pF
	A Port Input B Port Output	C_{PDB}	C_L=0, f=10MHz t_r=t_f=1nS OE=V_{CCA} (Output Enabled)	V_{CCA}=1.2V V_{CCB}=5V		38.1		pF
				V_{CCA}=1.2V V_{CCB}=1.8V		29		pF
				V_{CCA}=1.5V V_{CCB}=1.8V		29		pF
				V_{CCA}=1.8V V_{CCB}=1.8V		29		pF
				V_{CCA}=2.5V V_{CCB}=2.5V		29		pF
				V_{CCA}=2.5V V_{CCB}=5V		30		pF
				V_{CCA}=3.3V V_{CCB}=3.3~5V		30		pF
	B Port Input A Port Output			V_{CCA}=1.2V V_{CCB}=5V		25.4		pF
				V_{CCA}=1.2V V_{CCB}=1.8V		19		pF
				V_{CCA}=1.5V V_{CCB}=1.8V		18		pF
				V_{CCA}=1.8V V_{CCB}=1.8V		18		pF
				V_{CCA}=2.5V V_{CCB}=2.5V		18		pF
				V_{CCA}=2.5V V_{CCB}=5V		21		pF
				V_{CCA}=3.3V V_{CCB}=3.3~5V		21		pF

■ OPERATING CHARACTERISTICS (Cont.)

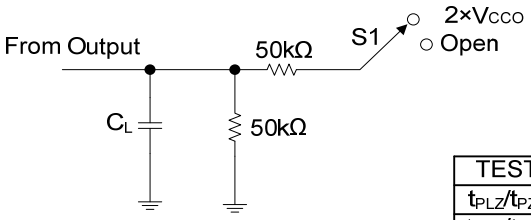
PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	A Port Input B Port Output	C_{PDB}	C_L=0, f=10MHz t_r=t_f=1nS OE=GND (Output Disabled)	V_{CCA}=1.2V V_{CCB}=5V		0.01		pF
				V_{CCA}=1.2V V_{CCB}=1.8V		0.01		pF
				V_{CCA}=1.5V V_{CCB}=1.8V		0.01		pF
				V_{CCA}=1.8V V_{CCB}=1.8V		0.01		pF
				V_{CCA}=2.5V V_{CCB}=2.5V		0.01		pF
				V_{CCA}=2.5V V_{CCB}=5V		0.01		pF
				V_{CCA}=3.3V V_{CCB}=3.3~5V		0.02		pF
	B Port Input A Port Output			V_{CCA}=1.2V V_{CCB}=5V		0.01		pF
				V_{CCA}=1.2V V_{CCB}=1.8V		0.01		pF
				V_{CCA}=1.5V V_{CCB}=1.8V		0.01		pF
				V_{CCA}=1.8V V_{CCB}=1.8V		0.01		pF
				V_{CCA}=2.5V V_{CCB}=2.5V		0.01		pF
				V_{CCA}=2.5V V_{CCB}=5V		0.02		pF
				V_{CCA}=3.3V V_{CCB}=3.3~5V		0.03		pF

■ TEST CIRCUIT AND WAVEFORMS

Load Circuit

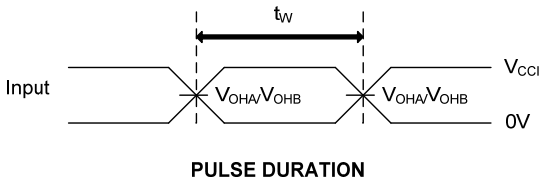


MAX DATA RATE, PULSE DURATION PROPAGATION DELAY OUTPUT RISE AND FALL TIME MEASUREMENT

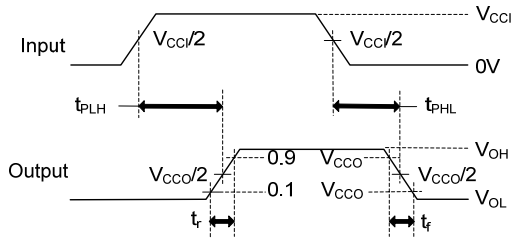


TEST	S1
t_{PLZ}/t_{PZL}	2×V_{CCO}
t_{PHZ}/t_{PZH}	Open

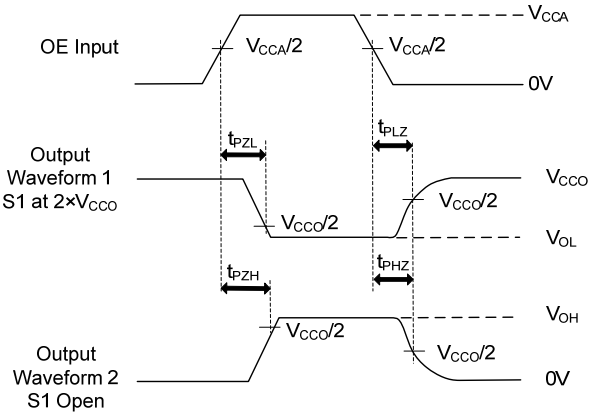
ENABLE/DISABLE TIME MEASUREMENT



PULSE DURATION



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.
2. The outputs are measured one at a time, with one transition per measurement.
3. t_{PLH} and t_{PHL} are the same as t_{PD}.
4. V_{CCI} is the V_{CC} associated with the input port.
5. V_{CCO} is the V_{CC} associated with the output port.
6. All parameters and waveforms are not applicable to all devices.

■ DETAILED DESCRIPTION

Overview

The **UTXB0102** device is a 2-bit directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.2V to 3.6V, while the B port can accept I/O voltages from 1.65V to 5.5V. The device is a buffered architecture with edge rate accelerators (one shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. For open drain signal translation, see UTC UTXS010X products.

Architecture

The **UTXB0102** architecture (see Figure 1) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a DC state, the output drivers of the **UTXB0102** can maintain a high or low, but are designed to be weak, so that the drivers can be overdriven by an external driver when data on the bus starts flowing the opposite direction. The output one shots detect rising or falling edges on the A or B ports.

During a rising edge, the one shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70Ω at V_{CCO}=1.2V to 1.8V, 50Ω at V_{CCO}=1.8V to 3.3V and 40Ω at V_{CCO}=3.3V to 5V.

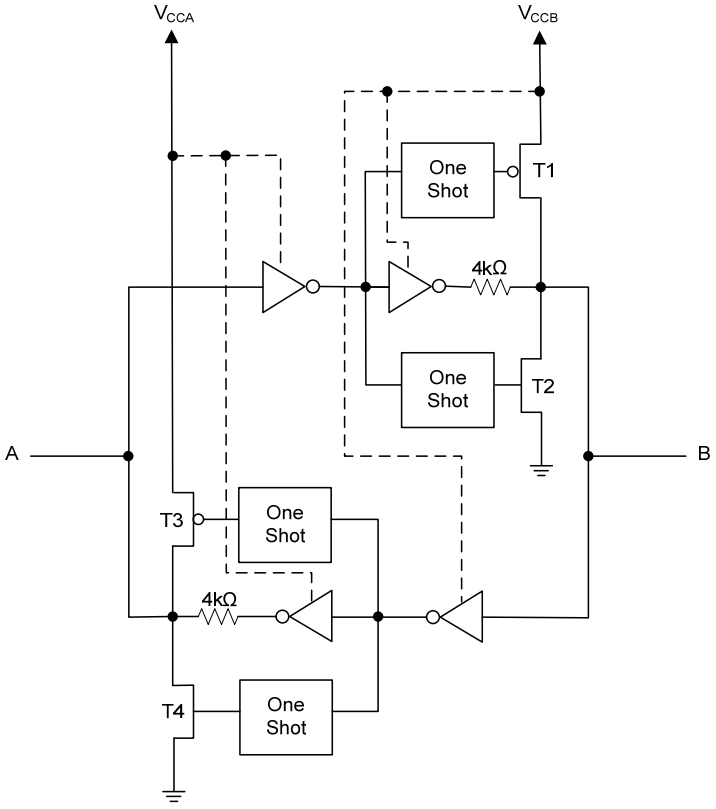


Figure 1. Architecture of UTXB0102 I/O Cell

■ DETAILED DESCRIPTION (Cont.)

Power-Up

During operation, assure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The **UTXB0102** device has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B}$=0V). The (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To assure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pull-down resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pull-down resistor to ground is determined by the current-sourcing capability of the driver.

Enable and Disable

The **UTXB0102** has an output-enable (OE) input that is used to disable the device by setting OE=low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

Pull-up or Pull-down Resistors on I/O Lines

The **UTXB0102** is designed to drive capacitive loads of up to 70pF. The output drivers of the **UTXB0102** have low DC drive strength. If pull-up or pull-down resistors are connected externally to the data I/Os, their values must be kept higher than 50kΩ to assure that they do not contend with the output drivers of the **UTXB0102**.

For the same reason, the **UTXB0102** device must not be used in applications such as I^2C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the UTC UTXS01xx series of level translators.

Device Functional Modes

The **UTXB0102** device has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high enables the device.

Output Load Considerations

Recommends careful printed-circuit board (PCB) layout practices with short PCB trace lengths to avoid excessive capacitive loading and to assure that proper O.S. triggering takes place. PCB signal trace-lengths must be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by assuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 10ns. The maximum capacitance of the lumped load that is driven also depends directly on the one-shot duration. With heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic I_{CC}, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the **UTXB0102** output sees, so recommends that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

■ TYPICAL APPLICATION CIRCUIT