



4N50-LC

Preliminary

Power MOSFET

4A, 500V N-CHANNEL POWER MOSFET

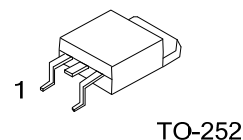
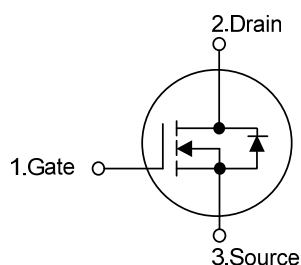
DESCRIPTION

The UTC **4N50-LC** is a high voltage power MOSFET designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and high rugged avalanche characteristics. This power MOSFET is usually used in high speed switching applications of switching power supplies and adaptors.

FEATURES

- * $R_{DS(ON)} \leq 1.9 \Omega$ @ $V_{GS}=10V$, $I_D=2.0A$
- * Fast switching capability
- * Avalanche energy tested
- * Improved dv/dt capability, high ruggedness

SYMBOL



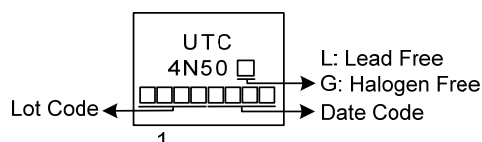
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
4N50L-TN3-R	4N50G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>4N50G-TN3-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) TN3: TO-252 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V _{DSS}	500	V
Gate-Source Voltage		V _{GSS}	±30	V
Continuous Drain Current		I _D	4	A
Pulsed Drain Current (Note 2)		I _{DM}	8	A
Avalanche Energy	Single Pulsed (Note 3)	E _{AS}	135	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.5	V/ns
Power Dissipation		P _D	45	W
Junction Temperature		T _J	+150	°C
Storage Temperature		T _{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 30\text{mH}$, $I_{AS} = 3.0\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 4.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.7 (Note)	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

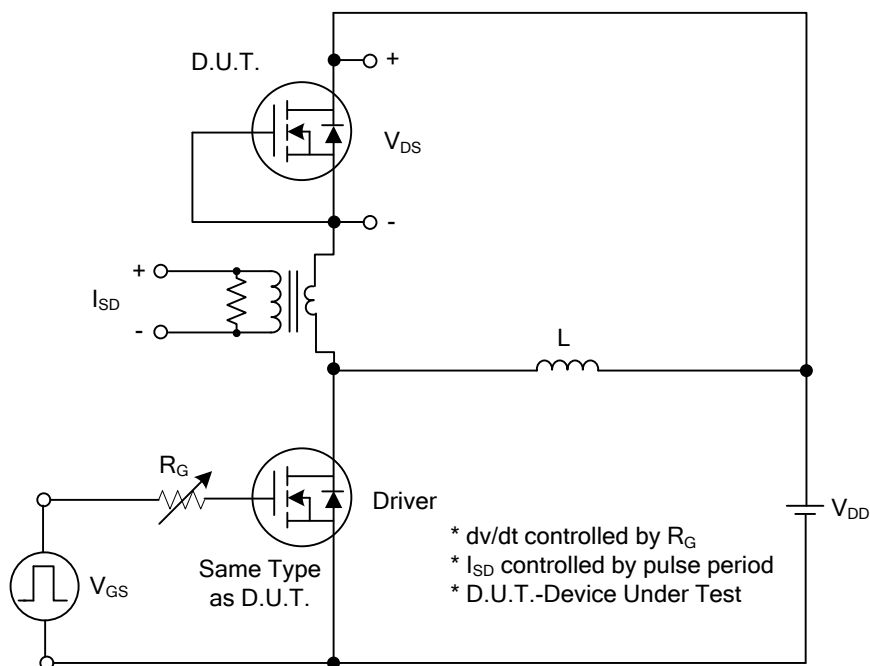
■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	500			V
Drain-Source Leakage Current		I_{DSS}	$V_{DS} = 500V, V_{GS} = 0V$			10	μA
Gate- Source Leakage Current	Forward	I_{GSS}	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
	Reverse		$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0		4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 2.0A$			1.9	Ω
DYNAMIC CHARACTERISTICS							
Input Capacitance		C_{ISS}	$V_{DS}=25V, V_{GS}=0V, f=1.0MHz$		446		pF
Output Capacitance		C_{OSS}			52		pF
Reverse Transfer Capacitance		C_{RSS}			5.2		pF
SWITCHING CHARACTERISTICS							
Total Gate Charge (Note 1)		Q_G	$V_{DS}=400V, V_{GS}=10V, I_D=4A$ $I_G=1mA$ (Note 1, 2)		15.4		nC
Gate-Source Charge		Q_{GS}			4.3		nC
Gate-Drain Charge		Q_{GD}			3.1		nC
Turn-On Delay Time (Note 1)		$t_{D(ON)}$	$V_{DS}=100V, V_{GS}=10V, I_D=4A,$ $R_G=25\Omega$ (Note 1, 2)		5		ns
Turn-On Rise Time		t_R			16		ns
Turn-Off Delay Time		$t_{D(OFF)}$			36		ns
Turn-Off Fall Time		t_F			24		ns
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
Maximum Continuous Drain-Source Diode Forward Current		I_S				4	A
Maximum Pulsed Drain-Source Diode Forward Current		I_{SM}				8	A
Drain-Source Diode Forward Voltage (Note 1)		V_{SD}	$I_S=4.0A, V_{GS}=0V$			1.4	V
Reverse Recovery Time (Note 1)		t_{rr}	$I_S=4.0A, V_{GS}=0V$		210		ns
Reverse Recovery Charge		Q_{rr}	$di/dt=100A/\mu s$		3		μC

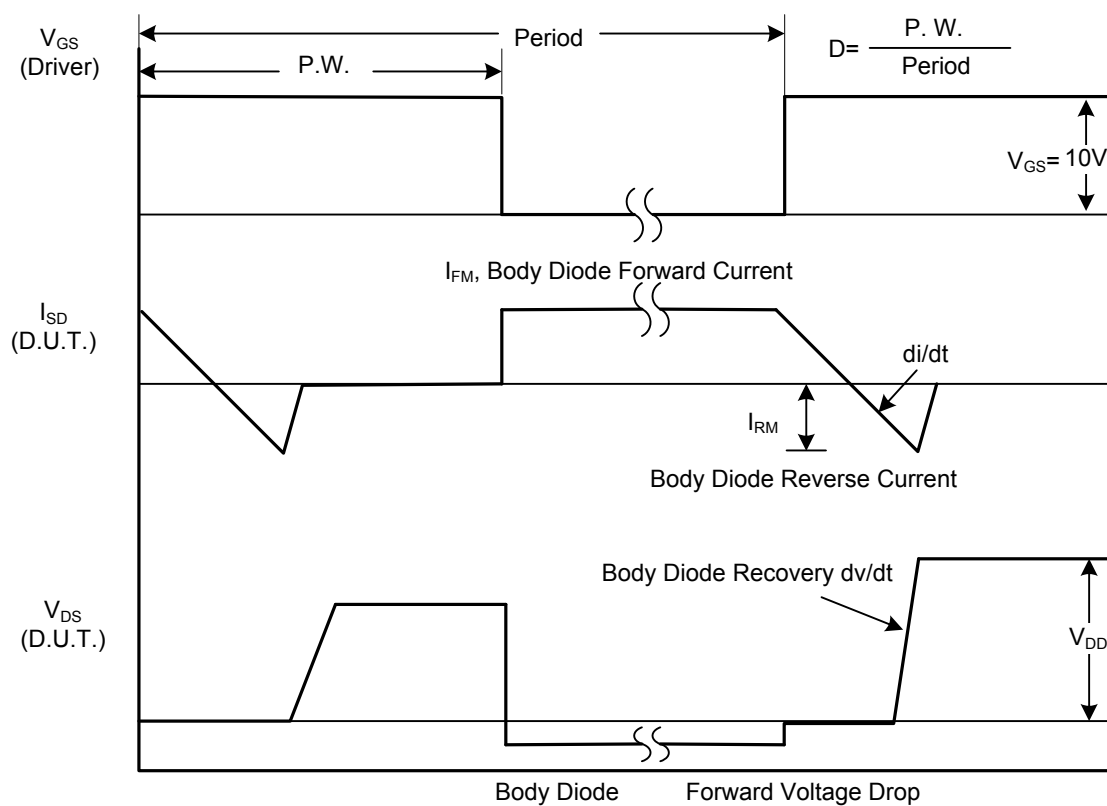
Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

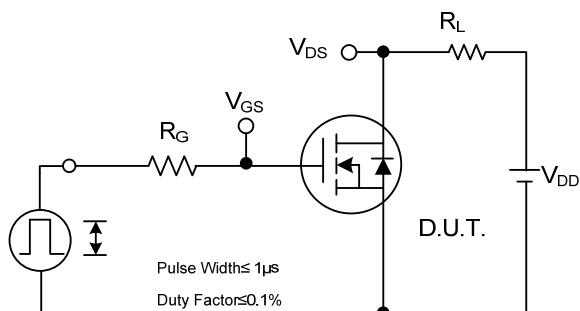


Peak Diode Recovery dv/dt Test Circuit

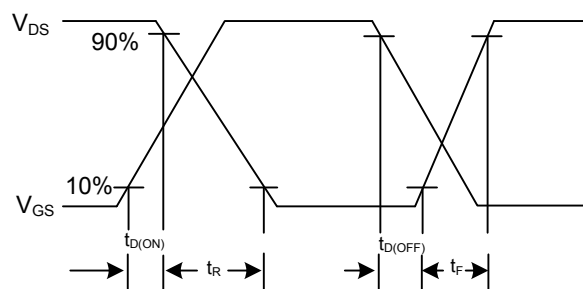


Peak Diode Recovery dv/dt Waveforms

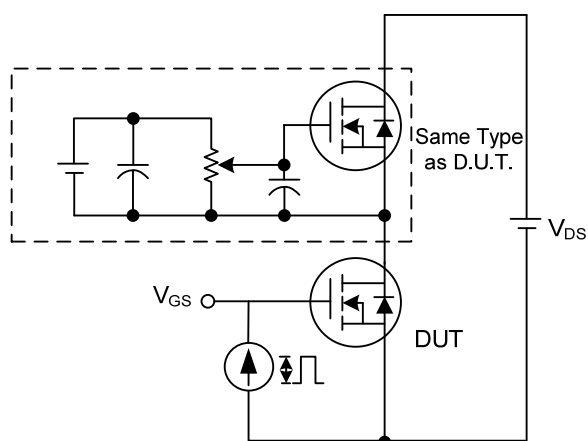
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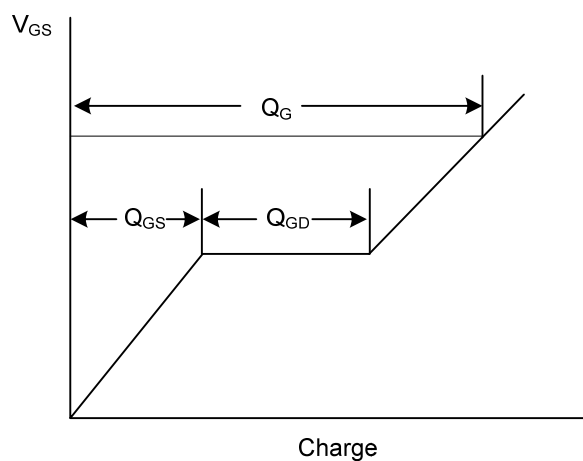
Switching Test Circuit



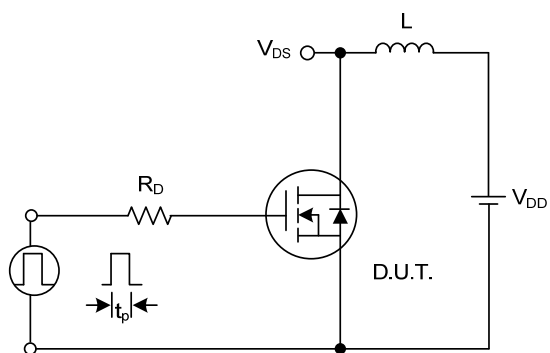
Switching Waveforms



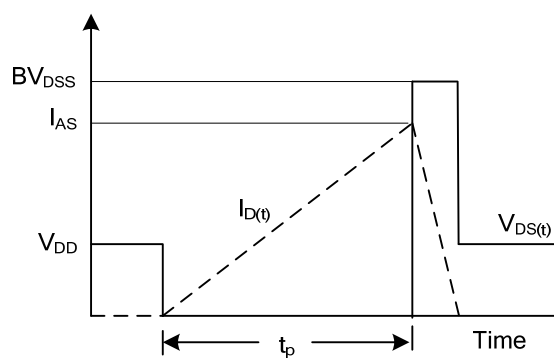
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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