



80A, 90V N-CHANNEL POWER TRENCH MOSFET

DESCRIPTION

The UTC **UTT80N09M** is an N-channel enhancement MOSFET, it uses UTC's advanced technology to provide the customers with perfect $R_{DS(ON)}$, high switching speed, high current capacity and low gate charge.

The UTC **UTT80N09M** is suitable for DC-DC converters, Off-Line UPS, High Voltage Synchronous Rectifier, Primary Switch for 48V and 24V Systems, etc.

FEATURES

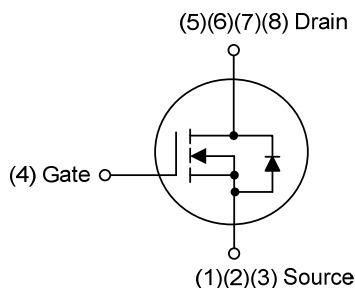
* $R_{DS(ON)} \leq 13.5 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=40\text{A}$

$R_{DS(ON)} \leq 15.5 \text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=40\text{A}$

* High Switching Speed

* High Current Capacity

SYMBOL

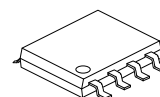


ORDERING INFORMATION

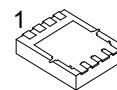
Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UTT80N09ML-S08-R	UTT80N09MG-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
UTT80N09ML-P5060-R	UTT80N09MG-P5060-R	PDFN5×6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UTT80N09MG-S08-R		(1) Packing Type	(1) R: Tape Reel
		(2) Package Type	(2) S08: SOP-8, P5060: PDFN5×6
		(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free



SOP-8



PDFN5×6

■ MARKING

SOP-8	PDFN5×6
Diagram of SOP-8 marking: The package is marked with 'UTC' and 'UTT80N09M'. Pin numbers 1 through 8 are indicated. A date code (four digits) is located at the top right, and a lot code (two digits) is located at the bottom right.	Diagram of PDFN5×6 marking: The package is marked with 'UTC' and 'UTT80N09M'. A date code (four digits) is located at the top right, and a lot code (two digits) is located at the bottom left.

■ **ABSOLUTE MAXIMUM RATING** ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	90	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous	I_{D}	80	A
	Pulsed	I_{DM}	160	A
Avalanche Energy	Single Pulsed (Note 4)	E_{AS}	40	mJ
Peak Diode Recovery dv/dt (Note 5)		dv/dt	12.3	V/ns
Power Dissipation (Note 3)	SOP-8	P_{D}	7	W
	PDFN5×6		50	W
Junction Temperature		T_{J}	+150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=0.1\text{mH}$, $I_{\text{AS}}=28.2\text{A}$, $V_{\text{DD}}=20\text{V}$, $R_{\text{G}}=25\ \Omega$, Starting $T_{\text{J}} = 25^{\circ}\text{C}$

4. $I_{\text{SD}}\leq 30\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{\text{DD}}\leq BV_{\text{DSS}}$, Starting $T_{\text{J}} = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-8	θ_{JA}	125	$^{\circ}\text{C}/\text{W}$
	PDFN5×6		65	$^{\circ}\text{C}/\text{W}$
Junction to Case	SOP-8	θ_{JC}	17.8	$^{\circ}\text{C}/\text{W}$
	PDFN5×6		2.5	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

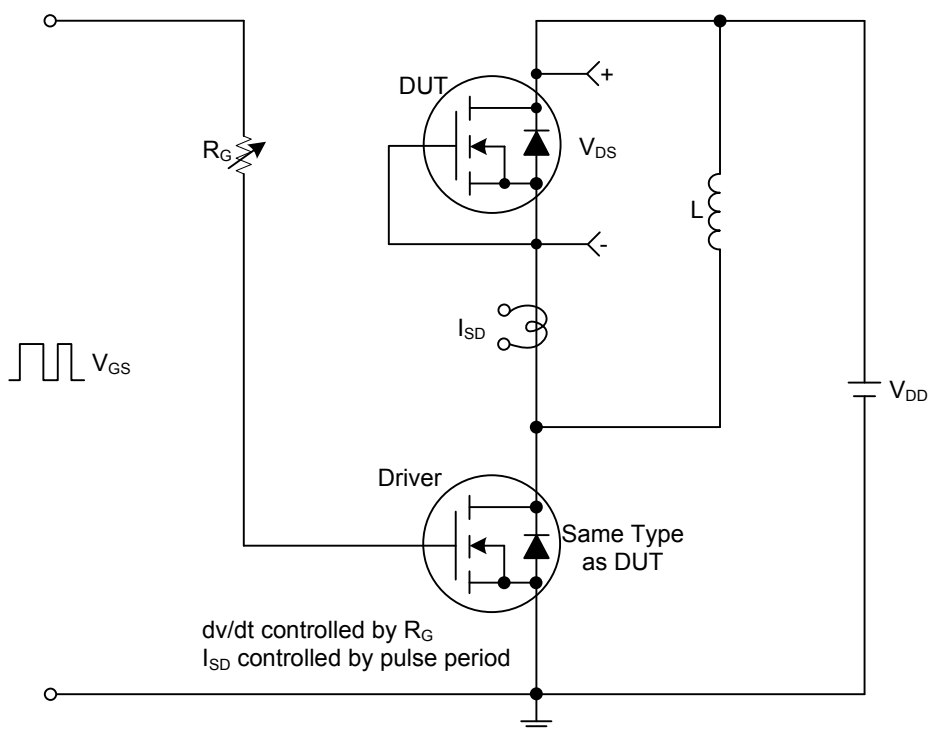
■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	90			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =90V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse		V _{GS} =-20V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =40A			13.5	mΩ
			V _{GS} =4.5V, I _D =40A			15.5	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		3080		pF
Output Capacitance		C _{OSS}			241.2		pF
Reverse Transfer Capacitance		C _{RSS}			219.6		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DS} =72V, V _{GS} =10V, I _D =80A I _G =1mA (Note 1, 2)		95.6		nC
Gate to Source Charge		Q _{GS}			23		nC
Gate to Drain Charge		Q _{GD}			15.6		nC
Turn-on Delay Time (Note 1)		t _{D(ON)}	V _{DD} =45V, V _{GS} =10V, I _D =80A, R _G =3.3Ω (Note 1, 2)		8.8		ns
Rise Time		t _R			17.3		ns
Turn-off Delay Time		t _{D(OFF)}			60.8		ns
Fall-Time		t _F			27		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I _S				80	A
Maximum Body-Diode Pulsed Current		I _{SM}				160	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =80A, V _{GS} =0V			1.4	V
Reverse Recovery Time		t _{rr}	I _S =80A, V _{GS} =0V,		64		ns
Reverse Recovery Charge		Q _{rr}	dI _F /dI _t =100A/μs		143		nC

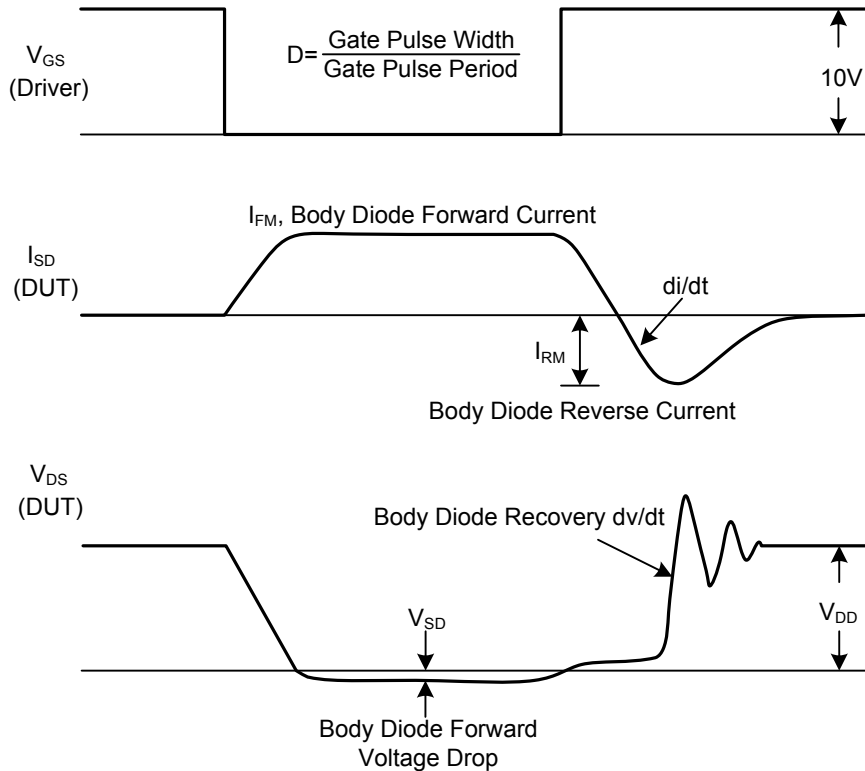
Notes: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



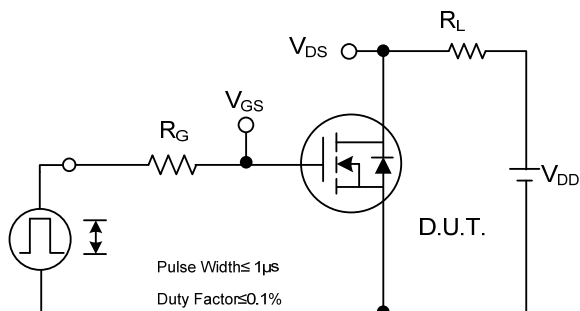
Peak Diode Recovery dv/dt Test Circuit



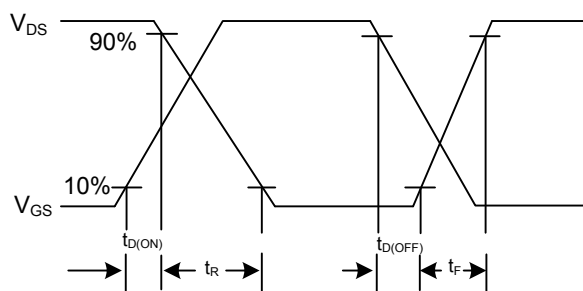
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

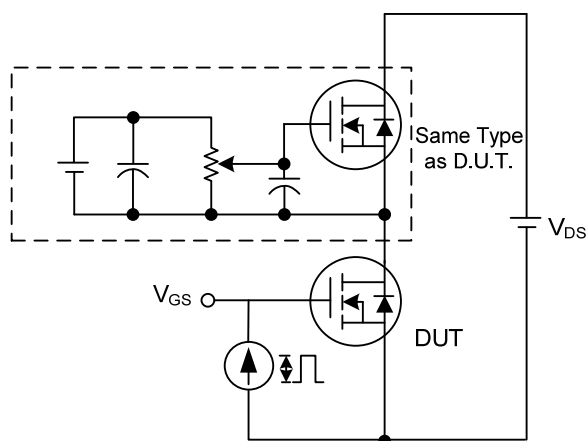
■ TEST CIRCUITS AND WAVEFORMS



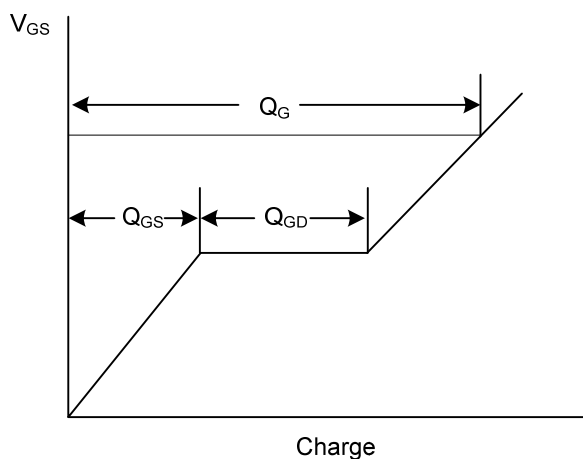
Switching Test Circuit



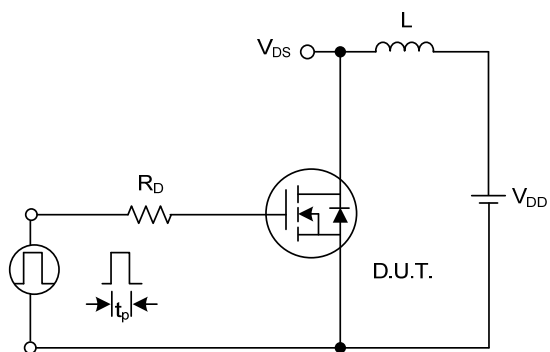
Switching Waveforms



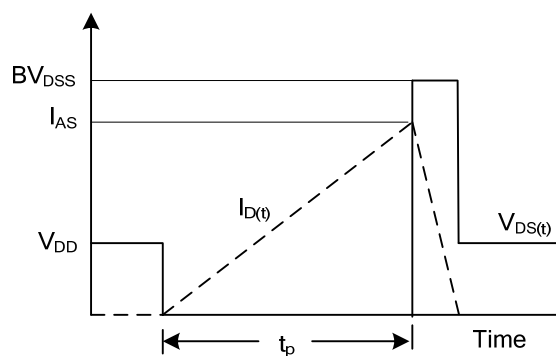
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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