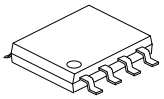
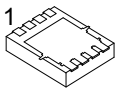
UTT80N09M **Preliminary** ***POWER MOSFET***

80A, 90V N-CHANNEL POWER TRENCH MOSFET



SOP-8



PDFN5×6

■ DESCRIPTION

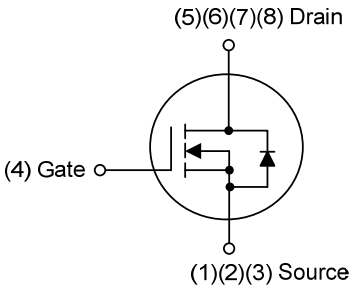
The UTC **UTT80N09M** is an N-channel enhancement MOSFET, it uses UTC's advanced technology to provide the customers with perfect $R_{DS(ON)}$, high switching speed, high current capacity and low gate charge.

The UTC **UTT80N09M** is suitable for DC-DC converters, Off-Line UPS, High Voltage Synchronous Rectifier, Primary Switch for 48V and 24V Systems, etc.

■ FEATURES

* $R_{DS(ON)} \leq 13.5\ m\Omega$ @ V_{GS}=10V, I_D=40A
  $R_{DS(ON)} \leq 15.5\ m\Omega$ @ V_{GS}=4.5V, I_D=40A
* High Switching Speed
* High Current Capacity

■ SYMBOL



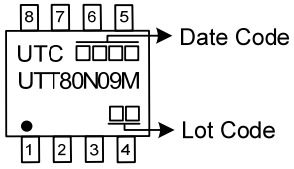
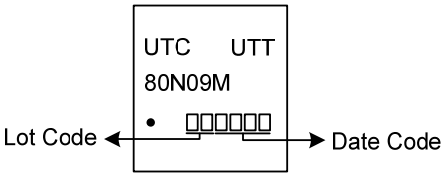
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UTT80N09ML-S08-R	UTT80N09MG-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
UTT80N09ML-P5060-R	UTT80N09MG-P5060-R	PDFN5×6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UTT80N09MG-S08-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S08: SOP-8, P5060: PDFN5×6 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

SOP-8	PDFN5×6
	

■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	90	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	Continuous	I_D	80	A
	Pulsed	I_{DM}	160	A
Avalanche Energy	Single Pulsed (Note 4)	E_{AS}	40	mJ
Peak Diode Recovery dv/dt (Note 5)		dv/dt	12.3	V/ns
Power Dissipation (Note 3)	SOP-8	P_D	7	W
	PDFN5×6		50	W
Junction Temperature		T_J	+150	°C
Storage Temperature Range		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. L=0.1mH, I_{AS}=28.2A, V_{DD}=20V, R_G=25 Ω, Starting T_J = 25°C
4. I_{SD}≤30A, di/dt≤200A/μs, V_{DD}≤ BV_{DSS}, Starting T_J = 25°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-8	θ_{JA}	125	°C/W
	PDFN5×6		65	°C/W
Junction to Case	SOP-8	θ_{JC}	17.8	°C/W
	PDFN5×6		2.5	°C/W

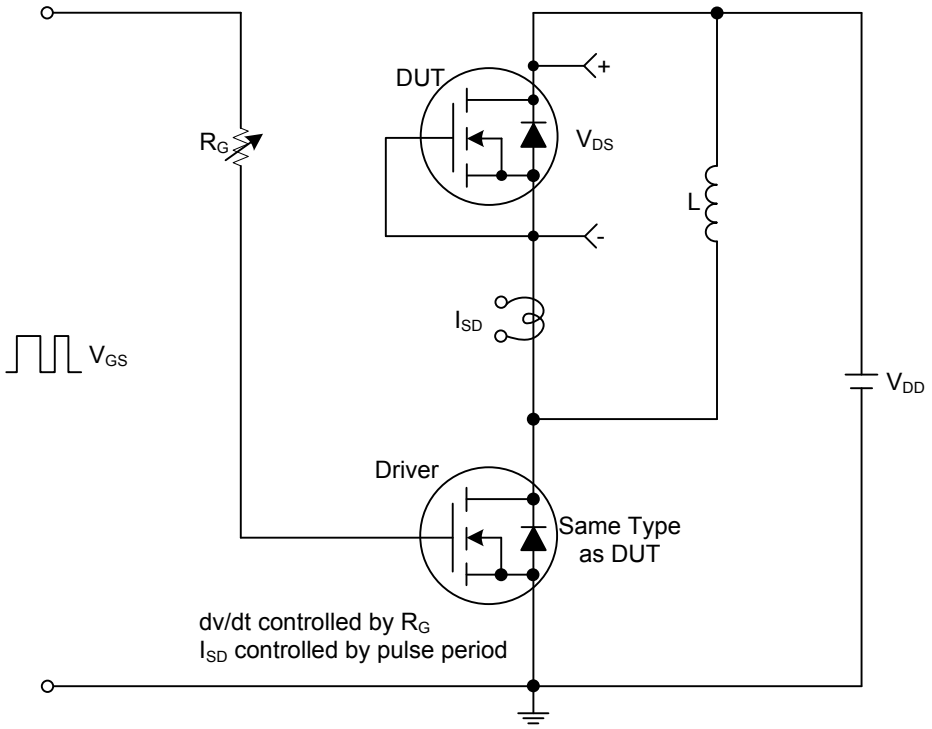
Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

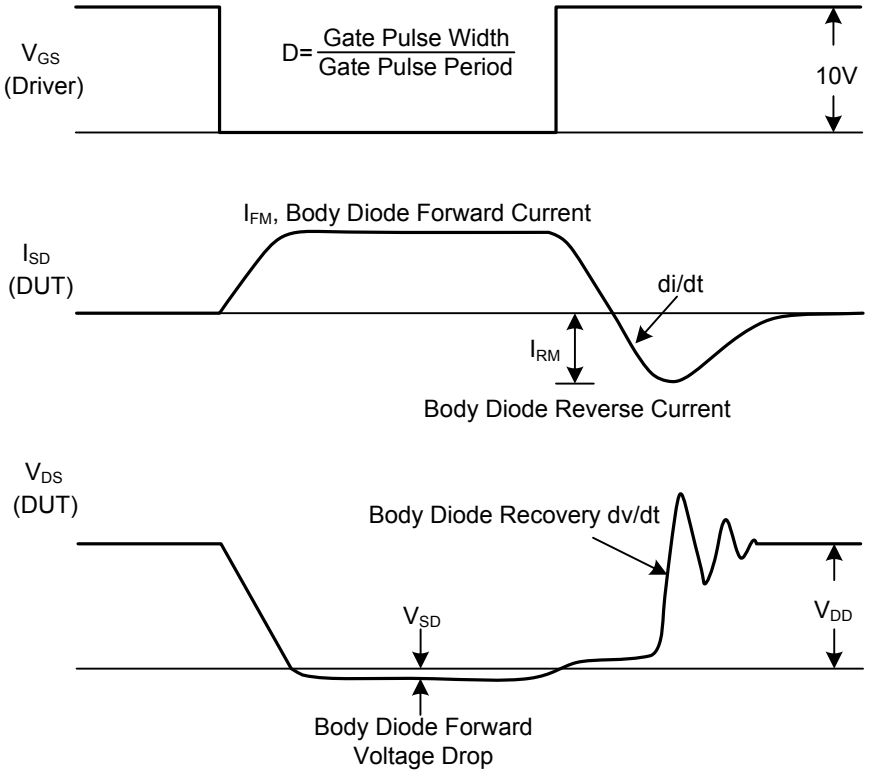
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	90			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=90V, V_{GS}=0V			10	μA
Gate-Source Leakage Current	Forward	I_{GSS}	V_{GS}=+20V, V_{DS}=0V			+100	nA
	Reverse		V_{GS}=-20V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	1.0		3.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=40A			13.5	mΩ
			V_{GS}=4.5V, I_D=40A			15.5	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1.0MHz		3080		pF
Output Capacitance		C_{OSS}			241.2		pF
Reverse Transfer Capacitance		C_{RSS}			219.6		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q_G	V_{DS}=72V, V_{GS}=10V, I_D=80A I_G=1mA (Note 1, 2)		95.6		nC
Gate to Source Charge		Q_{GS}			23		nC
Gate to Drain Charge		Q_{GD}			15.6		nC
Turn-on Delay Time (Note 1)		$t_{D(ON)}$	V_{DD}=45V, V_{GS}=10V, I_D =80A, R_G =3.3Ω (Note 1, 2)		8.8		ns
Rise Time		t_R			17.3		ns
Turn-off Delay Time		$t_{D(OFF)}$			60.8		ns
Fall-Time		t_F			27		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				80	A
Maximum Body-Diode Pulsed Current		I_{SM}				160	A
Drain-Source Diode Forward Voltage (Note 1)		V_{SD}	I_S=80A, V_{GS}=0V			1.4	V
Reverse Recovery Time		t_{rr}	I_S=80A, V_{GS}=0V, d_{IF}/d_t=100A/μs		64		ns
Reverse Recovery Charge		Q_{rr}			143		nC

Notes: 1. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



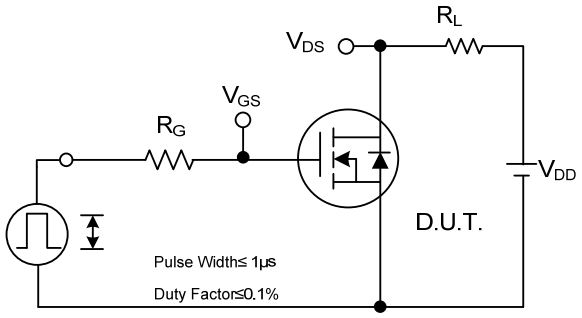
Peak Diode Recovery dv/dt Test Circuit



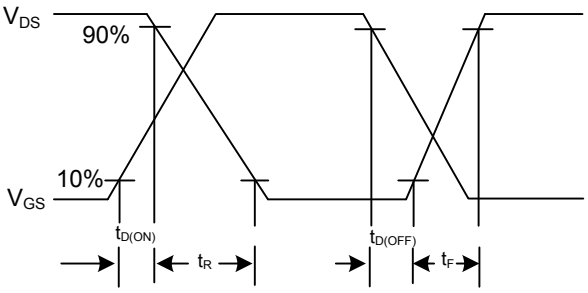
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

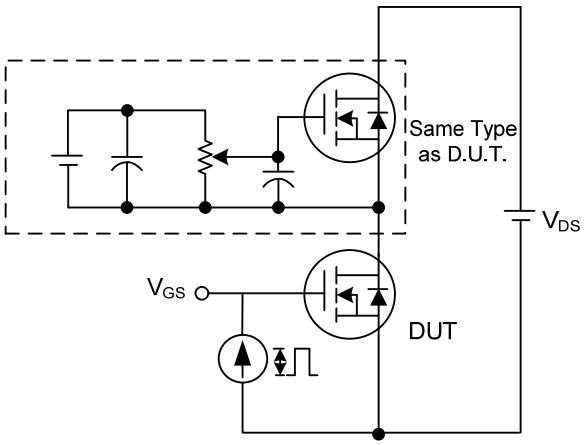
■ TEST CIRCUITS AND WAVEFORMS



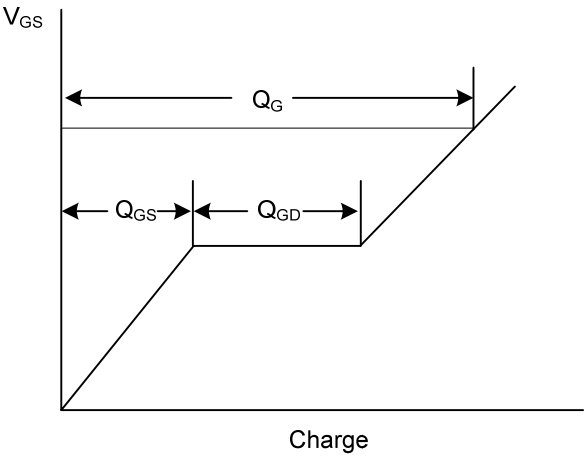
Switching Test Circuit



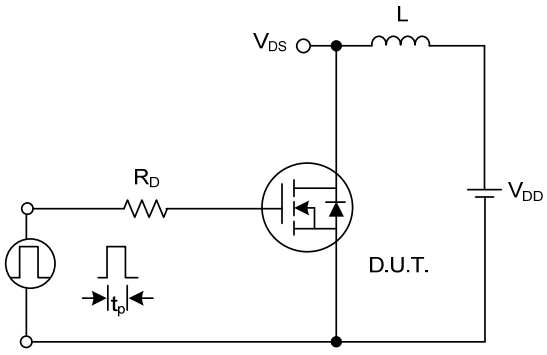
Switching Waveforms



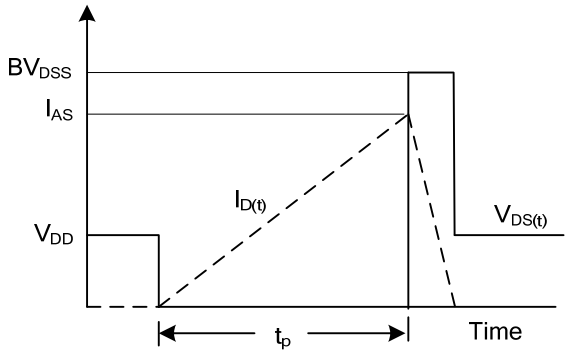
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms