

3N70-HC1

Preliminary

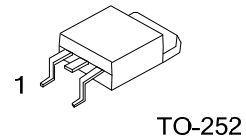
Power MOSFET

3A, 700V N-CHANNEL POWER MOSFET

■ DESCRIPTION

The UTC **3N70-HC1** is an N-channel power MOSFET using UTC's advanced technology to provide customers with a minimum on-state resistance and superior switching performance.

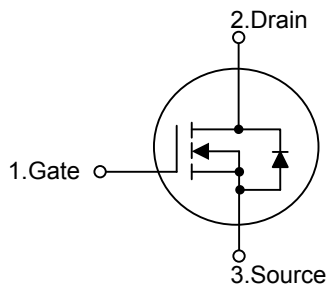
The UTC **3N70-HC1** is generally applied in low power switching mode power appliances and electronic ballast.



■ FEATURES

- * $R_{DS(ON)} \leq 6.0 \Omega$ @ $V_{GS}=10V$, $I_D=1.5A$
- * High Switching Speed
- * 100% Avalanche Tested

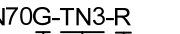
■ SYMBOL



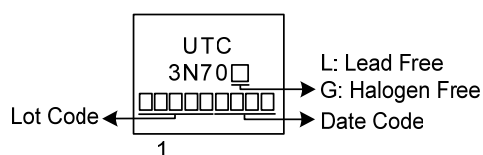
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
3N70L-TN3-R	3N70G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

 <p>3N70G-TN3-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	700	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	3	A
	Pulsed (Note 2)	I_{DM}	6	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	44.1	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	3.6	V/ns
Power Dissipation		P_D	45	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 10\text{mH}$, $I_{AS} = 2.9\text{A}$, $V_{DD} = 70\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 3.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	110	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.78 (Note)	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

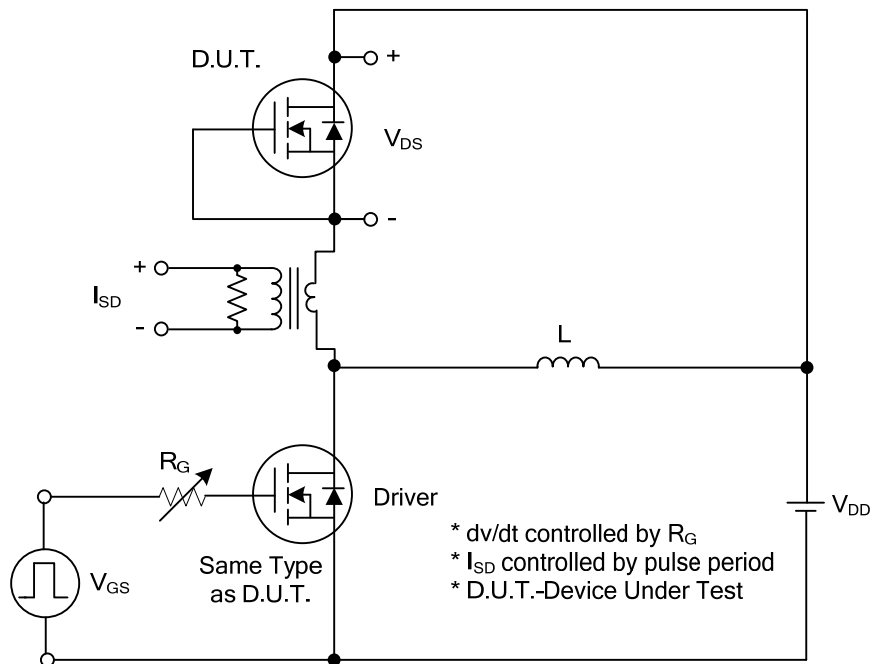
■ ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	$I_D=250\mu A, V_{GS}=0V$	700			V
Drain-Source Leakage Current		I_{DSS}	$V_{DS}=700V, V_{GS}=0V$			10	μA
Gate- Source Leakage Current	Forward	I_{GSS}	$V_{GS}=+30V, V_{DS}=0V$			+100	nA
	Reverse		$V_{GS}=-30V, V_{DS}=0V$			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0		4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	$V_{GS}=10V, I_D=1.5A$			6.0	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	$V_{GS}=0V, V_{DS}=25V, f=1.0MHz$		315.7		pF
Output Capacitance		C_{OSS}			36		pF
Reverse Transfer Capacitance		C_{RSS}			4.5		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q_G	$V_{DS}=560V, V_{GS}=10V, I_D=3A$ $I_G=1mA$ (Note 1, 2)		14.5		nC
Gate to Source Charge		Q_{GS}			5		nC
Gate to Drain Charge		Q_{GD}			2.6		nC
Turn-ON Delay Time (Note 1)		$t_{D(ON)}$	$V_{DD}=100V, V_{GS}=10V,$ $I_D=3A, R_G=25\Omega$ (Note 1, 2)		5		ns
Rise Time		t_R			15.2		ns
Turn-OFF Delay Time		$t_{D(OFF)}$			33.6		ns
Fall-Time		t_F			30.1		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				3	A
Maximum Body-Diode Pulsed Current (Note 1)		I_{SM}				6	A
Drain-Source Diode Forward Voltage (Note 1)		V_{SD}	$I_S=3A, V_{GS}=0V$			1.4	V
Body Diode Reverse Recovery Time		t_{rr}	$I_S=3A, V_{GS}=0V,$		263		ns
Body Diode Reverse Recovery Charge		Q_{rr}	$dI_F/dt=100A/\mu s$		3.2		μC

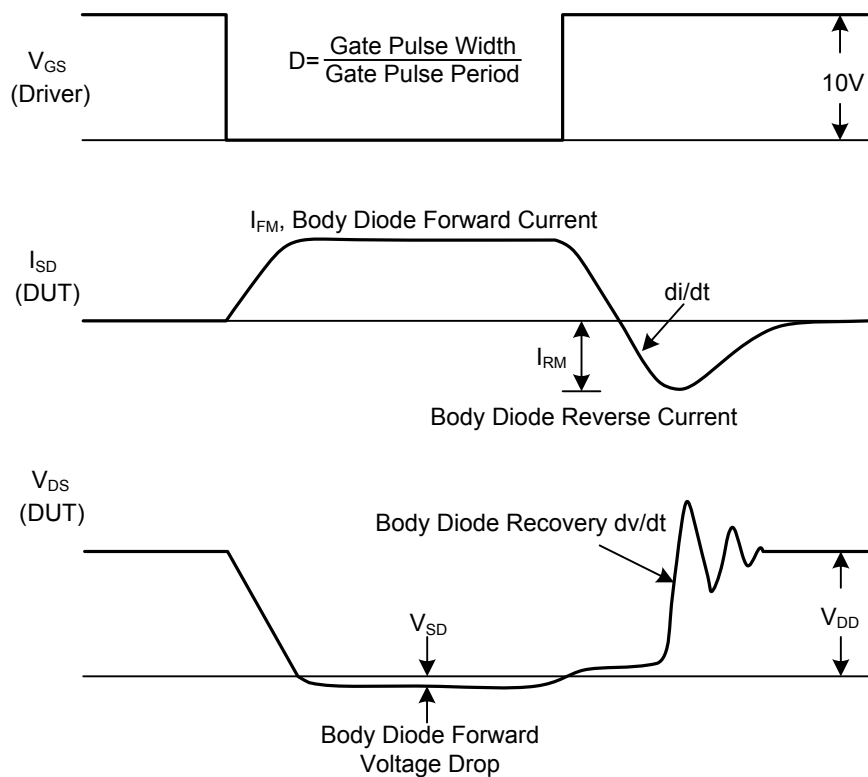
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

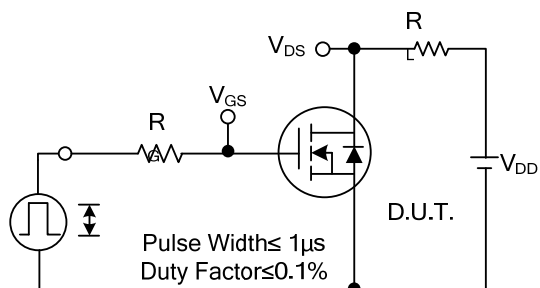


Peak Diode Recovery dv/dt Test Circuit

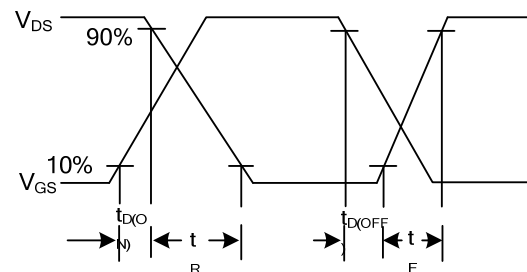


Peak Diode Recovery dv/dt Waveforms

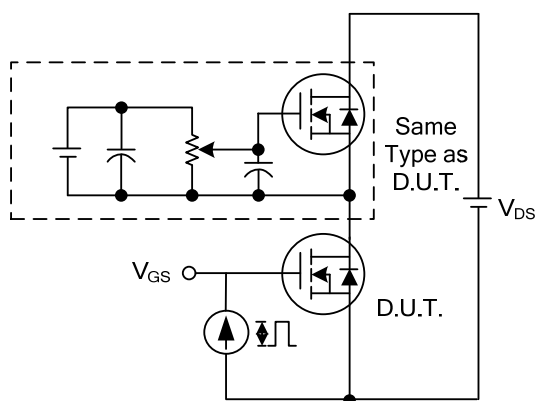
■ TEST CIRCUITS AND WAVEFORMS



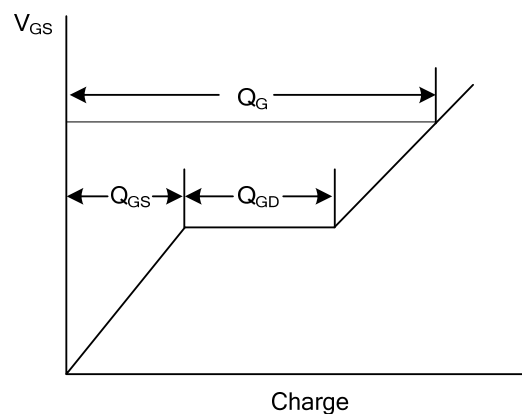
Switching Test Circuit



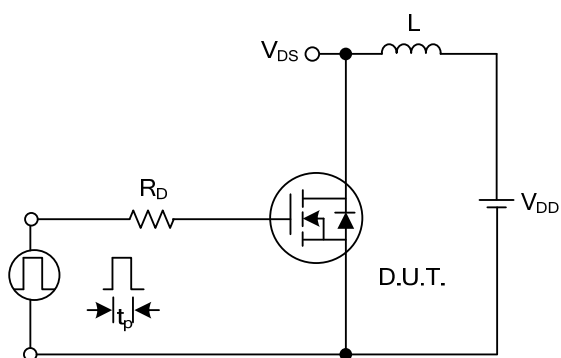
Switching Waveforms



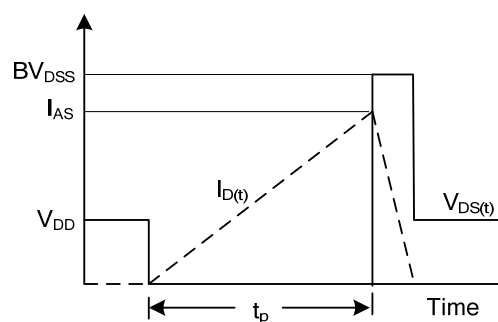
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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