



UT5N12

Preliminary

Power MOSFET

5A, 120V N-CHANNEL POWER MOSFET

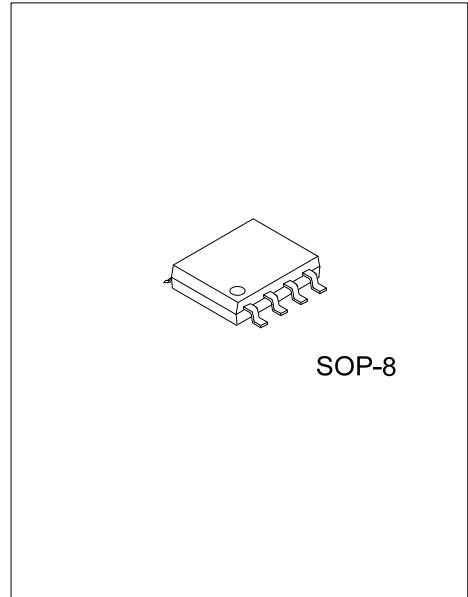
DESCRIPTION

The UTC **UT5N12** is an N-channel power MOSFET using UTC's advanced technology to provide customers with a minimum on-state resistance and superior switching performance.

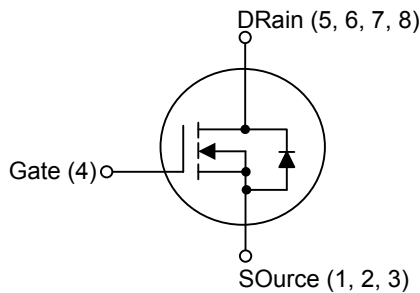
The UTC **UT5N12** is generally applied in low power switching mode power appliances and electronic ballast.

FEATURES

- * $R_{DS(ON)} \leq 140 \text{ m}\Omega @ V_{GS}=10V, I_D=2.5A$
- * $R_{DS(ON)} \leq 150 \text{ m}\Omega @ V_{GS}=4.5V, I_D=1.0A$
- * High Switching Speed
- * 100% Avalanche Tested



SYMBOL



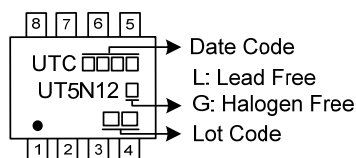
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment						Packing		
Lead Free	Halogen Free		1	2	3	4	5	6		7	8
UT5N12L-S08-R	UT5N12G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: S: Source G: Gate D: Drain

<p>UT5N12G-S08-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) S08: SOP-8</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	120	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current	Continuous	I_D	5	A
	Pulsed (Note 2)	I_{DM}	10	A
Peak Diode Recovery dv/dt (Note 4)		dv/dt	3.15	V/ns
Power Dissipation ($T_C=25^\circ\text{C}$)		P_D	1.6	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $I_{SD} \leq 5.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA (NOTE)

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	125	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	78	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

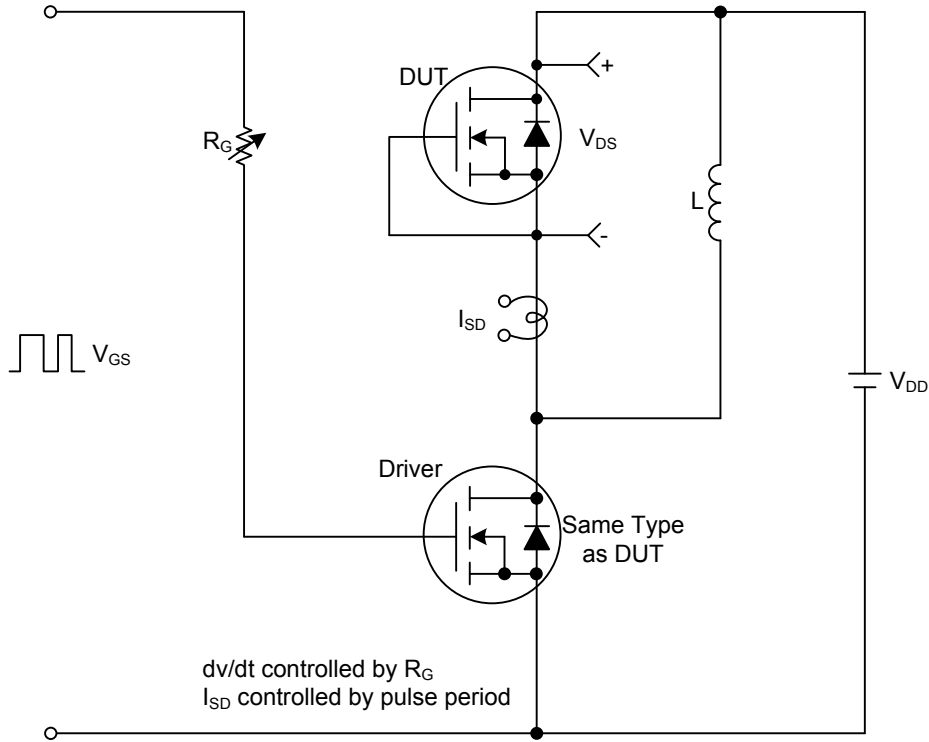
■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	120			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=120\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate- Source Leakage Current	Forward Reverse	I_{GSS} $V_{GS}=+20\text{V}$, $V_{DS}=0\text{V}$ $V_{GS}=-20\text{V}$, $V_{DS}=0\text{V}$			+100	nA
					-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.0		3.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=2.5\text{A}$			140	m Ω
		$V_{GS}=4.5\text{V}$, $I_D=1.0\text{A}$			150	m Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		578		pF
Output Capacitance	C_{OSS}			42		pF
Reverse Transfer Capacitance	C_{RSS}			30		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=50\text{V}$, $V_{GS}=10\text{V}$, $I_D=1.6\text{A}$, $I_G=1\text{mA}$ (Note 1, 2)		23		nC
Gate to Source Charge	Q_{GS}			2.8		nC
Gate to Drain Charge	Q_{GD}			3.8		nC
Turn-ON Delay Time (Note 1)	$t_{D(ON)}$	$V_{DD}=50\text{V}$, $V_{GS}=10\text{V}$, $I_D=1.6\text{A}$, $R_G=25\Omega$ (Note 1, 2)		3.6		ns
Rise Time	t_R			17.3		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			84		ns
Fall-Time	t_F			41		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				5	A
Maximum Body-Diode Pulsed Current (Note 1)	I_{SM}				10	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=5.0\text{A}$, $V_{GS}=0\text{V}$			1.4	V
Reverse Recovery Time	t_{rr}	$I_S=5.0\text{A}$, $V_{GS}=0\text{V}$		36		ns
Reverse Recovery Charge	Q_{rr}	$dI_F/dt=100\text{A}/\mu\text{s}$ (Note 1)		7.5		nC

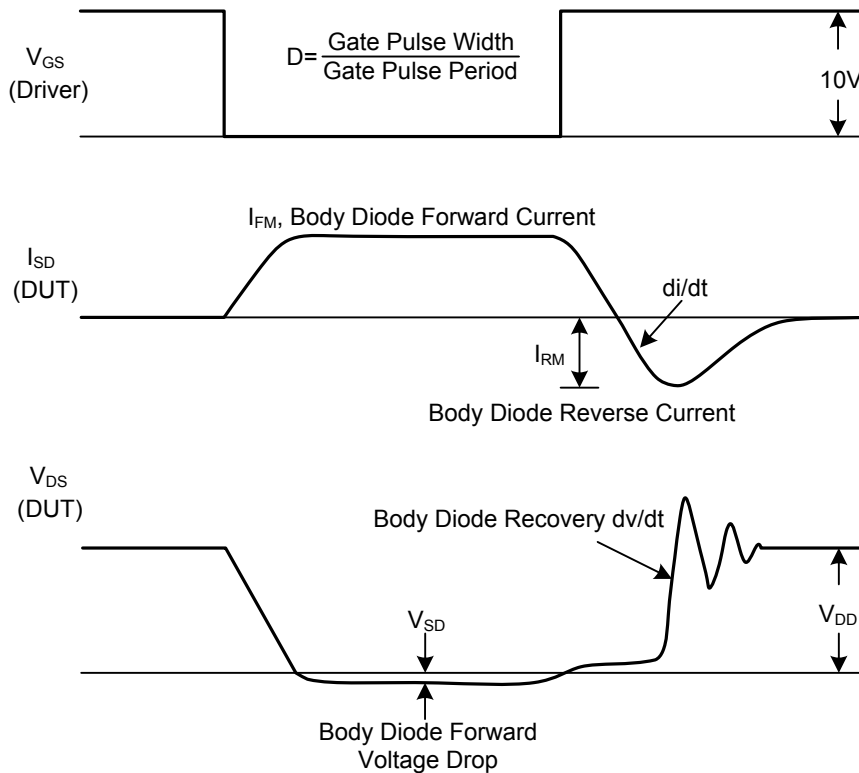
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

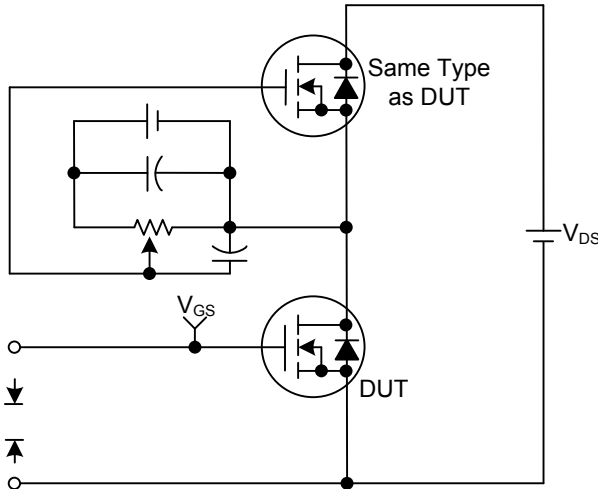


Peak Diode Recovery dv/dt Test Circuit & Waveforms

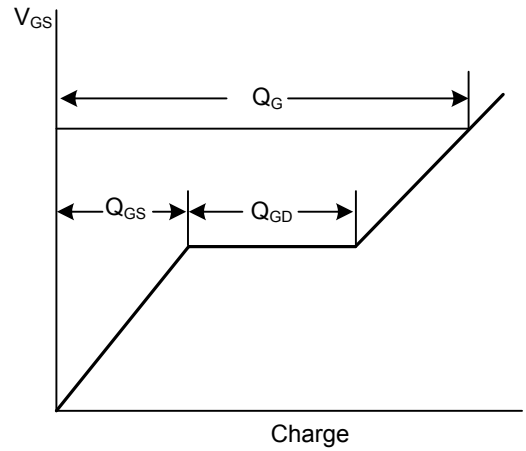


Peak Diode Recovery dv/dt Waveforms

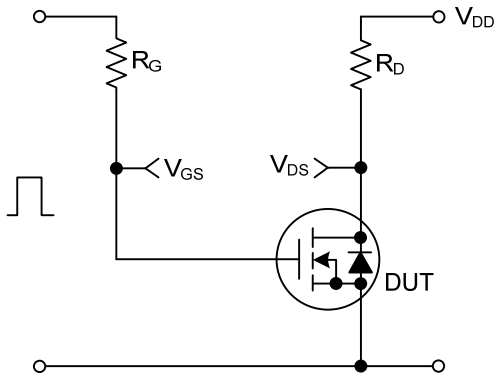
■ TEST CIRCUITS AND WAVEFORMS



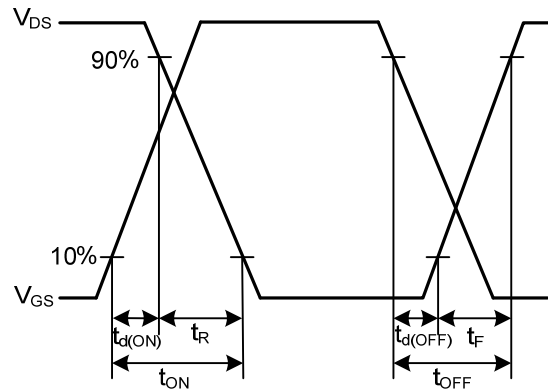
Gate Charge Test Circuit



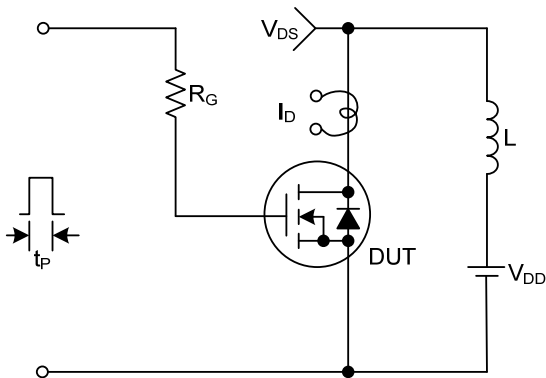
Gate Charge Waveforms



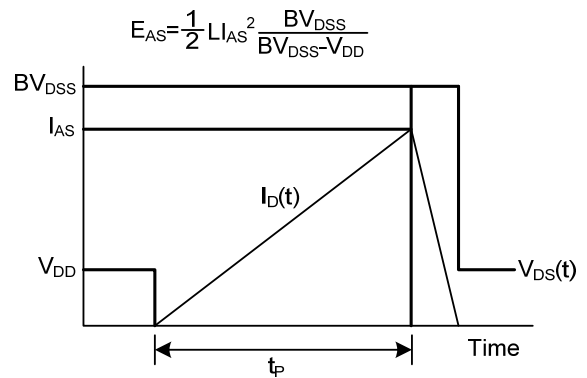
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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