



DUAL ENHANCEMENT MODE (N-CHANNEL / P-CHANNEL)

DESCRIPTION

The UTC **UT8NP04** incorporates a N-channel MOSFET and a P-channel MOSFET, it uses UTC's advanced technology to provide customers a minimum on-state resistance, high switching speed, low gate charge and cost effectiveness.

The UTC **UT8NP04** is universally applied in low voltage applications.

FEATURES

*N-CHANNEL

$R_{DS(on)} \leq 18 \text{ m}\Omega @ V_{GS}=10\text{V}, I_D=4.0\text{A}$

$R_{DS(on)} \leq 30 \text{ m}\Omega @ V_{GS}=4.5\text{V}, I_D=4.0\text{A}$

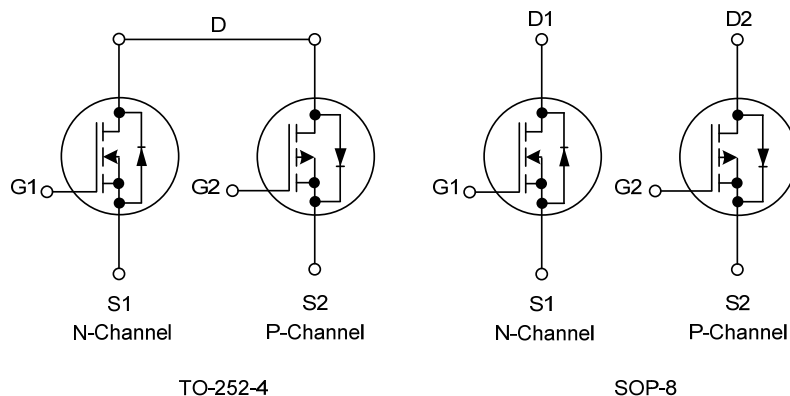
*P-CHANNEL

$R_{DS(on)} \leq 50 \text{ m}\Omega @ V_{GS}=-10\text{V}, I_D=-4.0\text{A}$

$R_{DS(on)} \leq 68 \text{ m}\Omega @ V_{GS}=-4.5\text{V}, I_D=-4.0\text{A}$

* High switching speed

SYMBOL



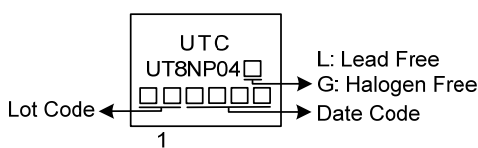
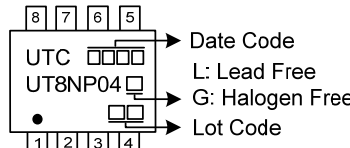
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT8NP04L-TN4-R	UT8NP04G-TN4-R	TO-252-4	S1	G1	D	S2	G2	-	-	-	Tape Reel
UT8NP04L-S08-R	UT8NP04G-S08-R	SOP-8	S1	G1	S2	G2	D2	D2	D1	D1	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT8NP04G-TN4-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) TN4: TO-252-4, S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING

TO-252-4	SOP-8
 Diagram of TO-252-4 marking: The package is a small rectangle. The top row contains 'UTC' and 'UT8NP04' followed by a small square. Below this, there are four small squares. An arrow points from the left to the first square, labeled 'Lot Code'. An arrow points from the right to the last square, labeled 'Date Code'. Below the squares is the number '1'. To the right of the package, there are three labels: 'L: Lead Free', 'G: Halogen Free', and 'Date Code'.	 Diagram of SOP-8 marking: The package is a small rectangle. The top row contains 'UTC' and 'UT8NP04' followed by a small square. Below this, there are four small squares. An arrow points from the right to the first square, labeled 'Date Code'. An arrow points from the right to the last square, labeled 'Lot Code'. Below the squares is the number '1'. To the right of the package, there are three labels: 'L: Lead Free', 'G: Halogen Free', and 'Lot Code'.

■ **ABSOLUTE MAXIMUM RATINGS** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER			SYMBOL	RATINGS		UNIT
				N-CHANNEL	P-CHANNEL	
Drain-Source Voltage			V _{DSS}	40	-40	V
Gate-Source Voltage			V _{GSS}	±20	±20	V
Drain Current	Continuous	TO-252-4	I _D	16	-16	A
		SOP-8		8	-8	A
	Pulsed (Note 1)	TO-252-4	I _{DM}	32	-32	A
		SOP-8		16	-16	A
Avalanche Energy, Single Pulse (Note 3)			E _{AS}	23	25.5	mJ
Power Dissipation		TO-252-4	P _D	43		W
		SOP-8		1.6		W
Junction Temperature			T _J	-55 ~ +150		°C
Storage Temperature Range			T _{STG}	-55 ~ +150		°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3. N-Channel: $L=0.1\text{mH}$, $I_{AS}=21.4\text{A}$, $V_{DD}=30\text{V}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$

P-Channel: $L=0.1\text{mH}$, $I_{AS}=-22.5\text{A}$, $V_{DD}=-30\text{V}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$

■ **THERMAL DATA (NOTE)**

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-252-4	θ_{JA}	110	$^{\circ}\text{C/W}$
	SOP-8		90	$^{\circ}\text{C/W}$
Junction to Case	TO-252-4	θ_{JC}	2.9	$^{\circ}\text{C/W}$
	SOP-8		78	$^{\circ}\text{C/W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

N-Channel

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	40			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =40V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{GS} =+20V			+100	nA
	Reverse		V _{GS} =-20V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance (Note 2)		R _{DS(ON)}	V _{GS} =10V, I _D =4.0A			18	mΩ
			V _{GS} =4.5V, I _D =4.0A			30	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =20V, f=1.0MHz		678.9		pF
Output Capacitance		C _{OSS}			91.9		pF
Reverse Transfer Capacitance		C _{RSS}			75.9		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 2)		Q _G	V _{DS} =32V, V _{GS} =10V, I _D =8.0A, I _G =1mA (Note 1, 2)		23.8		nC
Gate to Source Charge		Q _{GS}			3.4		nC
Gate to Drain Charge		Q _{GD}			6.6		nC
Turn-ON Delay Time (Note 2)		t _{D(ON)}	V _{DS} =20V, V _{GS} =10V, I _D =8.0A, R _G =6Ω (Note 1, 2)		4.9		ns
Rise Time		t _R			16.3		ns
Turn-OFF Delay Time		t _{D(OFF)}			22.5		ns
Fall-Time		t _F			18.7		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Drain-Source Diode Forward Voltage(Note 2)		V _{SD}	I _S =8.0A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time		t _{rr}	I _S =8.0A, V _{GS} =0V,		39		nS
Body Diode Reverse Recovery Charge		Q _{rr}	dI _F /dt=100A/μs		40		nC

■ ELECTRICAL CHARACTERISTICS (Cont.)

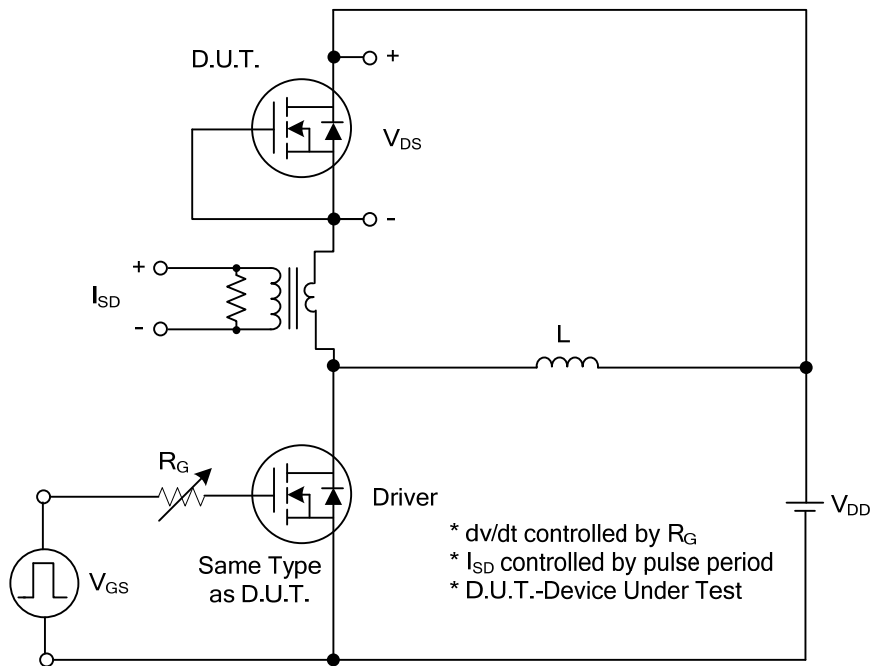
P-Channel

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	$I_D=-250\mu A, V_{GS}=0V$	-40			V
Drain-Source Leakage Current		I_{DSS}	$V_{DS}=-40V, V_{GS}=0V$			-1	μA
Gate-Source Leakage Current	Forward	I_{GSS}	$V_{GS}=+20V$			+100	nA
	Reverse		$V_{GS}=-20V$			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0		-3.0	V
Static Drain-Source On-State Resistance (Note 2)		$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-4.0A$			50	m Ω
			$V_{GS}=-4.5V, I_D=-4.0A$			68	m Ω
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	$V_{GS}=0V, V_{DS}=-20V, f=1.0MHz$		784.7		pF
Output Capacitance		C_{OSS}			111.9		pF
Reverse Transfer Capacitance		C_{RSS}			91.5		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 2)		Q_G	$V_{DS}=-32V, V_{GS}=-10V, I_D=-8.0A, I_G=-1mA$ (Note 1, 2)		23.2		nC
Gate to Source Charge		Q_{GS}			3		nC
Gate to Drain Charge		Q_{GD}			6.7		nC
Turn-ON Delay Time (Note 2)		$t_{D(ON)}$	$V_{DS}=-20V, V_{GS}=-10V, I_D=-8.0A, R_G=6\Omega$ (Note 1, 2)		5.5		ns
Rise Time		t_R			16.7		ns
Turn-OFF Delay Time		$t_{D(OFF)}$			32.2		ns
Fall-Time		t_F			21		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Drain-Source Diode Forward Voltage(Note 2)		V_{SD}	$I_S=-8.0A, V_{GS}=0V$			-1.4	V
Body Diode Reverse Recovery Time		t_{rr}	$I_S=-8.0A, V_{GS}=0V,$		56.6		nS
Body Diode Reverse Recovery Charge		Q_{rr}	$dI_F/dt=100A/\mu s$		130		nC

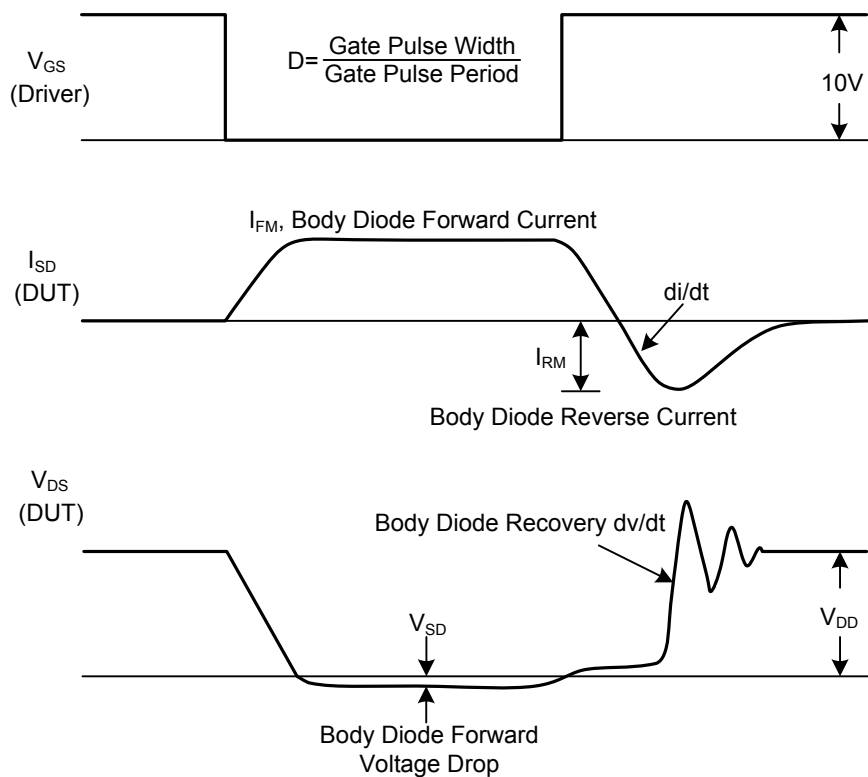
Notes: 1. Pulse width limited by maximum junction temperature

2. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$

■ TEST CIRCUITS AND WAVEFORMS

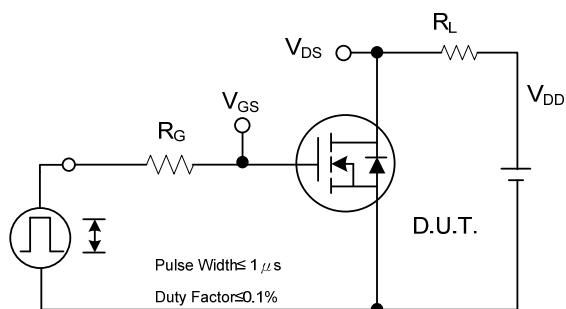


Peak Diode Recovery dv/dt Test Circuit

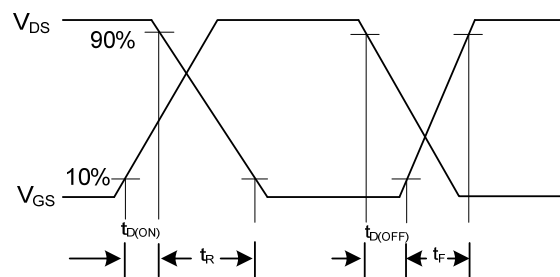


Peak Diode Recovery dv/dt Waveforms

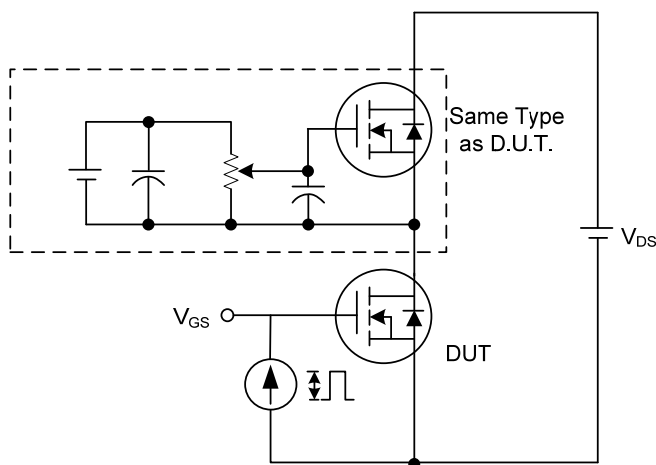
■ TEST CIRCUITS AND WAVEFORMS



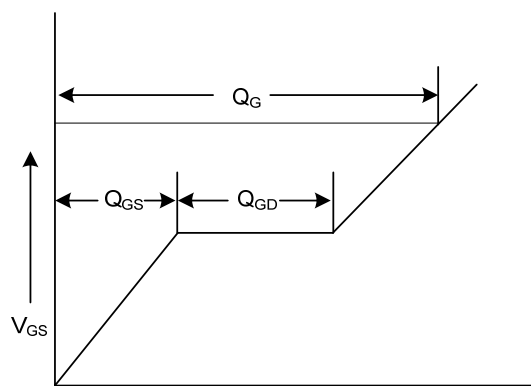
Switching Test Circuit



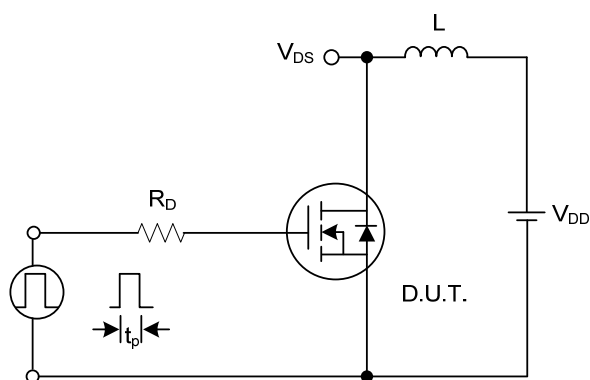
Switching Waveforms



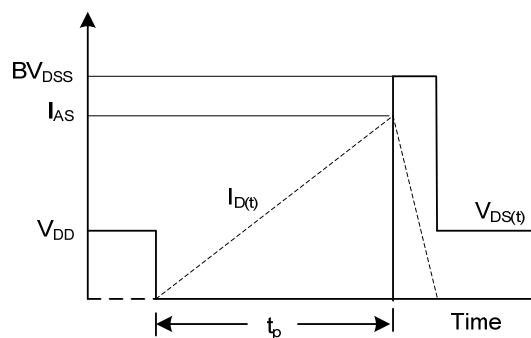
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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