

# USG60N10

**POWER MOSFET**

**60A, 100V N-CHANNEL  
ENHANCEMENT MODE  
TRENCH POWER MOSFET**

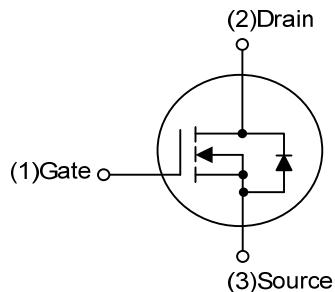
**■ DESCRIPTION**

The UTC **USG60N10** is a N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low  $R_{DS(ON)}$  characteristic by high cell density trench technology.

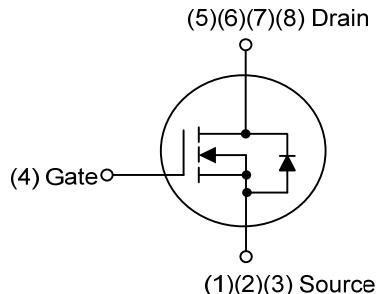
The UTC **USG60N10** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

**■ FEATURES**

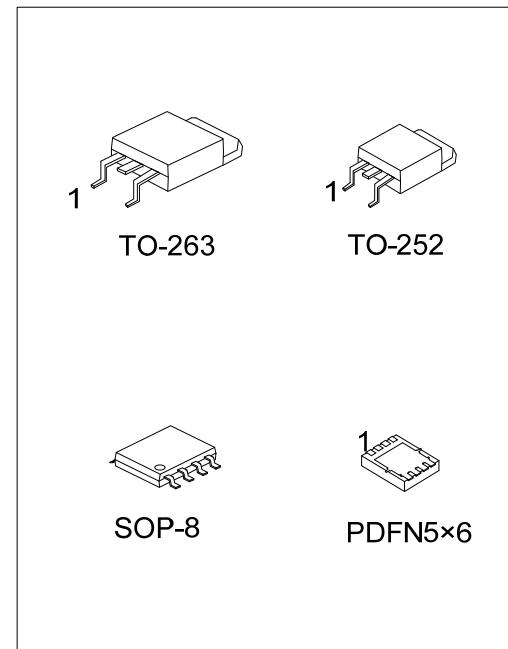
- \*  $R_{DS(ON)} \leq 10.5 \text{ m}\Omega$  @  $V_{GS}=10\text{V}$ ,  $I_D=30\text{A}$
- \*  $R_{DS(ON)} \leq 15 \text{ m}\Omega$  @  $V_{GS}=4.5\text{V}$ ,  $I_D=20\text{A}$
- \* Optimized for high speed switching, Logic level
- \* Enhanced Body diode dv/dt capability
- \* Enhanced Avalanche Ruggednessy

**■ SYMBOL**

TO-252/TO-263



SOP-8/PDFN5x6



### ■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
USG60N10L-TN3-R	USG60N10G-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
USG60N10L-TQ2-T	USG60N10G-TQ2-T	TO-263	G	D	S	-	-	-	-	-	Tube
USG60N10L-TQ2-R	USG60N10G-TQ2-R	TO-263	G	D	S	-	-	-	-	-	Tape Reel
USG60N10L-S08-R	USG60N10G-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
USG60N10L-P5060-R	USG60N10G-P5060-R	PDFN5×6	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

 USG60N10G-TN3-R	(1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel, T: Tube (2) TN3: TO-252, TQ2: TO-263, S08: SOP-8, P5060: PDFN5×6 (3) G: Halogen Free and Lead Free, L: Lead Free
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### ■ MARKING

Package	Marking
TO-252 TO-263	 Lot Code ← → Date Code 1
SOP-8	 Date Code ← → L: Lead Free G: Halogen Free Lot Code [1] [2] [3] [4]
PDFN5×6	 UTC    USG 60N10 •    [ ] [ ] [ ] [ ] Lot Code ← → Date Code

■ ABSOLUTE MAXIMUM RATING ( $T_c=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	100	V
Gate-Source Voltage		$V_{GSS}$	$\pm 20$	V
Drain Current	Continuous	$I_D$	60	A
	Pulsed (Note 2)	$I_{DM}$	100	A
Avalanche Energy	Single Pulsed (Note 3)	$E_{AS}$	3.7	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.83	V/ns
Power Dissipation	TO-252	$P_D$	65	W
	TO-263		80	W
	SOP-8		6	W
	PDFN5x6		58	W
Junction Temperature		$T_J$	+150	$^\circ\text{C}$
Storage Temperature Range		$T_{STG}$	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3.  $L = 0.1\text{mH}$ ,  $I_{AS} = 8.6\text{A}$ ,  $V_{DD} = 50\text{V}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$ .

4.  $I_{SD} \leq 30\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J = 25^\circ\text{C}$ .

## ■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-252	$\theta_{JA}$	110	$^\circ\text{C/W}$
	TO-263		62.5	$^\circ\text{C/W}$
	SOP-8		90 (Note)	$^\circ\text{C/W}$
	PDFN5x6		65 (Note)	$^\circ\text{C/W}$
Junction to Case	TO-252	$\theta_{JC}$	1.92 (Note)	$^\circ\text{C/W}$
	TO-263		1.56	$^\circ\text{C/W}$
	SOP-8		20.8 (Note)	$^\circ\text{C/W}$
	PDFN5x6		2.15 (Note)	$^\circ\text{C/W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

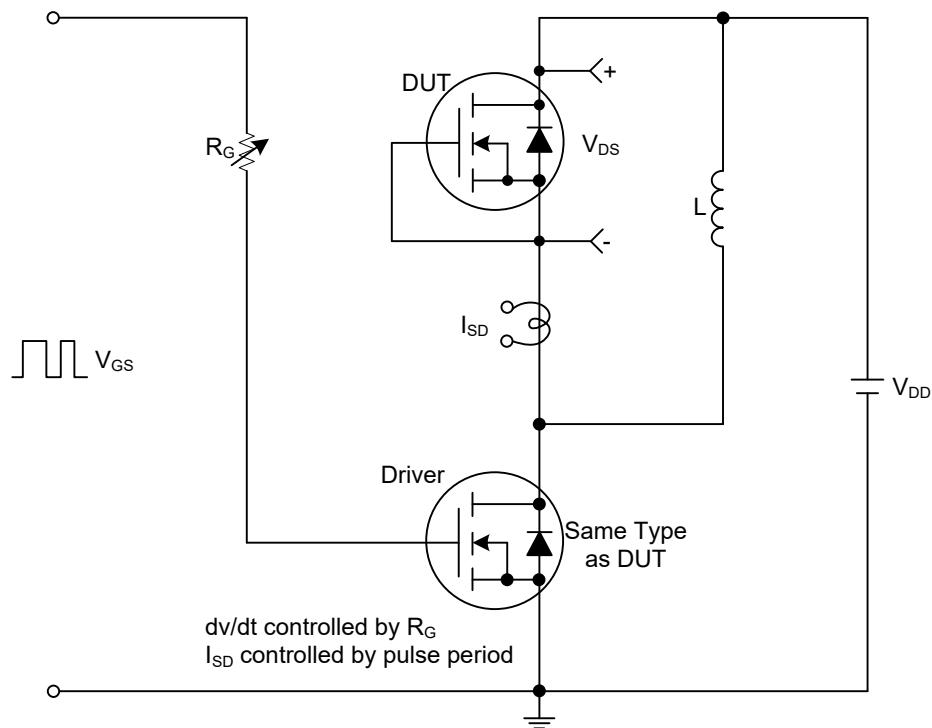
■ ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$I_D=250\mu\text{A}, V_{\text{GS}}=0\text{V}$	100			V
Drain-Source Leakage Current	$I_{\text{DSS}}$	$V_{\text{DS}}=100\text{V}, V_{\text{GS}}=0\text{V}$			1	$\mu\text{A}$
Gate-Source Leakage Current	Forward	$V_{\text{GS}}=+20\text{V}, V_{\text{DS}}=0\text{V}$			+100	nA
	Reverse	$V_{\text{GS}}=-20\text{V}, V_{\text{DS}}=0\text{V}$			-100	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{\text{GS}(\text{TH})}$	$V_{\text{DS}}=V_{\text{GS}}, I_D=250\mu\text{A}$	1.0		3.0	V
Static Drain-Source On-State Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=10\text{V}, I_D=30\text{A}$			10.5	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_D=20\text{A}$			15	$\text{m}\Omega$
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	$C_{\text{ISS}}$	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=25\text{V}, f=1.0\text{MHz}$		2048		pF
Output Capacitance	$C_{\text{OSS}}$			944		pF
Reverse Transfer Capacitance	$C_{\text{RSS}}$			95		pF
<b>SWITCHING PARAMETERS</b>						
Total Gate Charge (Note 1)	$Q_G$	$V_{\text{DS}}=80\text{V}, V_{\text{GS}}=10\text{V}, I_D=60\text{A}, I_G=1\text{mA}$ (Note 1, 2)		44		nC
Gate to Source Charge	$Q_{\text{GS}}$			9		nC
Gate to Drain Charge	$Q_{\text{GD}}$			12		nC
Turn-on Delay Time (Note 1)	$t_{\text{D}(\text{ON})}$	$V_{\text{DD}}=50\text{V}, V_{\text{GS}}=10\text{V}, I_D=60\text{A}, R_G=3.3\Omega$ (Note 1, 2)		10		ns
Rise Time	$t_R$			16		ns
Turn-off Delay Time	$t_{\text{D}(\text{OFF})}$			30		ns
Fall-Time	$t_F$			20		ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Body-Diode Continuous Current	$I_S$				60	A
Maximum Body-Diode Pulsed Current	$I_{\text{SM}}$				120	A
Drain-Source Diode Forward Voltage (Note 1)	$V_{\text{SD}}$	$I_S=60\text{A}, V_{\text{GS}}=0\text{V}$			1.2	V
Reverse Recovery Time (Note 1)	$t_{\text{rr}}$	$I_S=30\text{A}, V_{\text{GS}}=0\text{V}, dI_F/dt = 100\text{A}/\mu\text{s}$		60		nS
Reverse Recovery Charge	$Q_{\text{rr}}$			225		nC

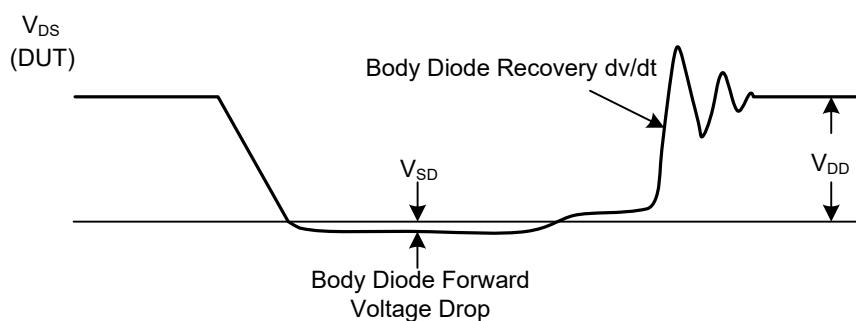
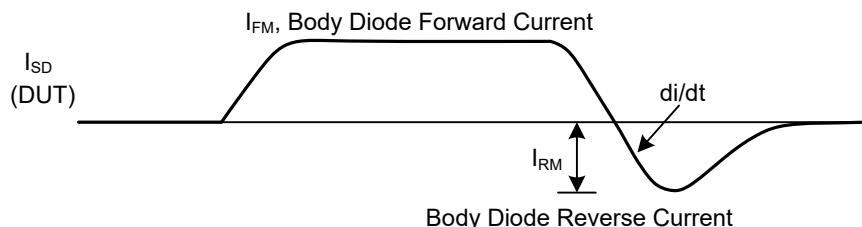
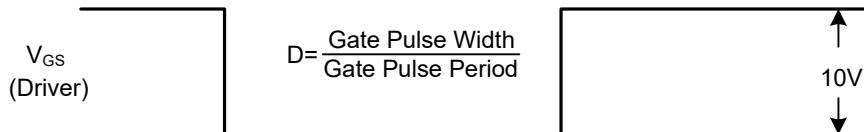
Notes: 1. Pulse Test : Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$ .

2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS



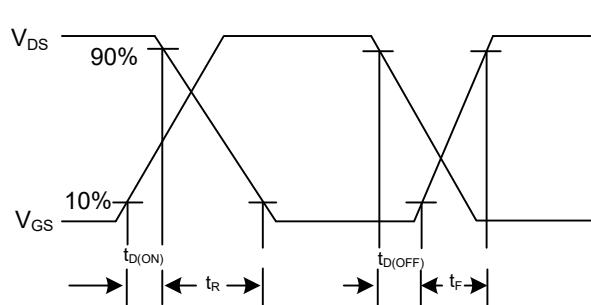
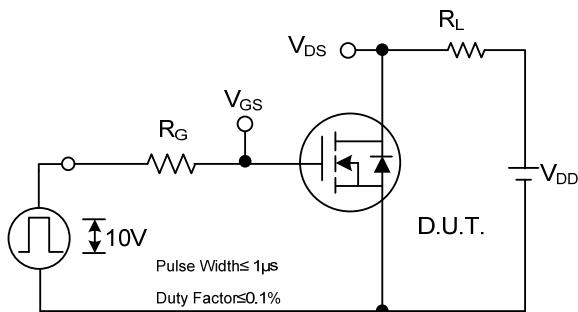
**Peak Diode Recovery dv/dt Test Circuit**



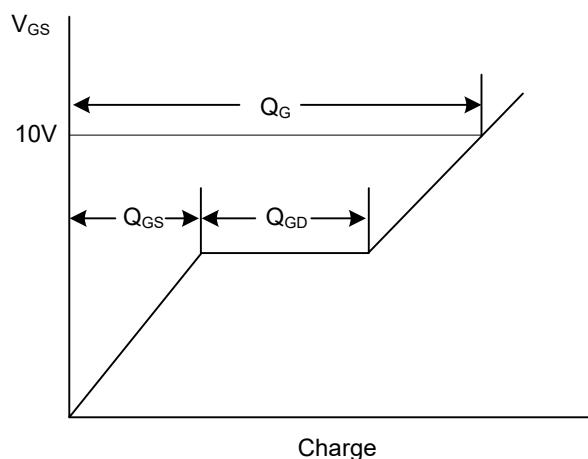
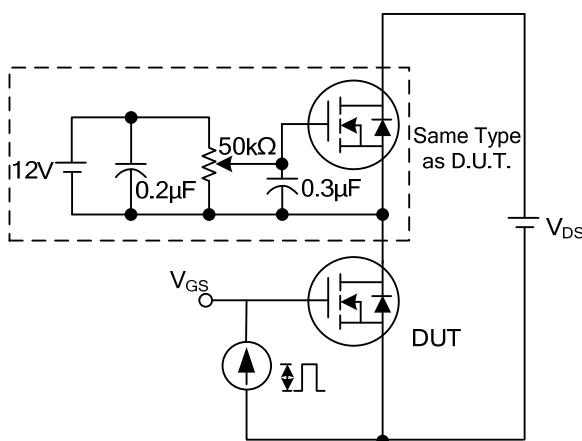
**Peak Diode Recovery dv/dt Test Circuit and Waveforms**

**Peak Diode Recovery dv/dt Waveforms**

### ■ TEST CIRCUITS AND WAVEFORMS

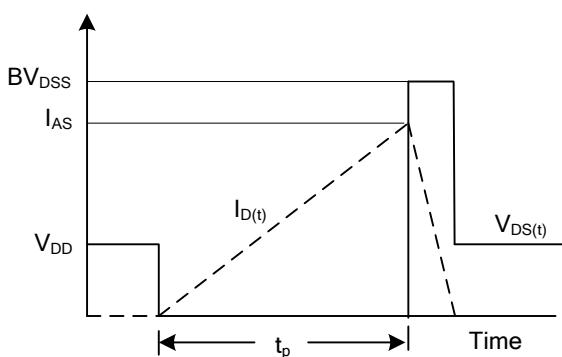
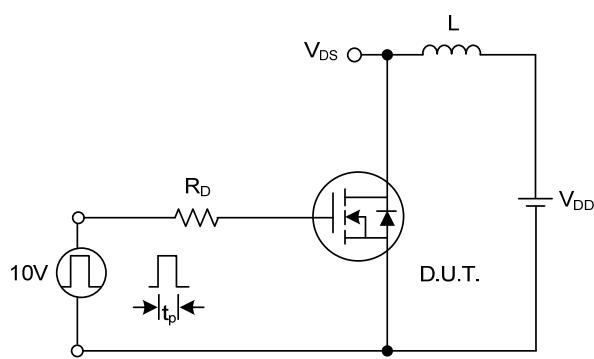


**Switching Test Circuit**



**Gate Charge Test Circuit**

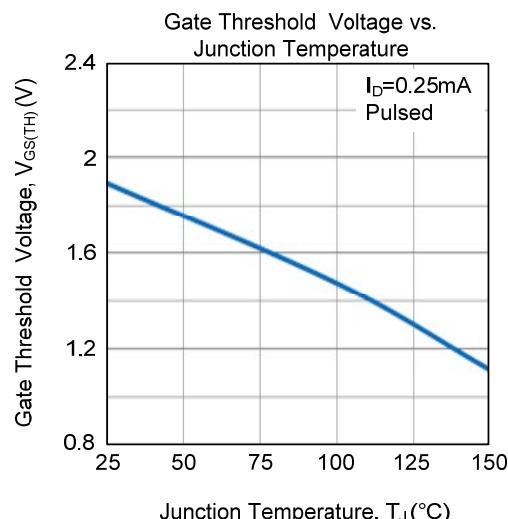
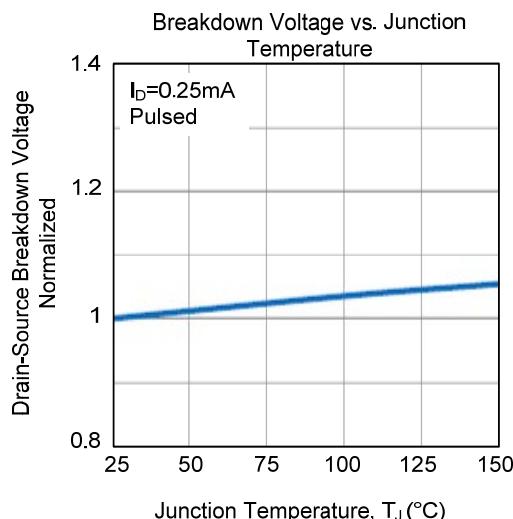
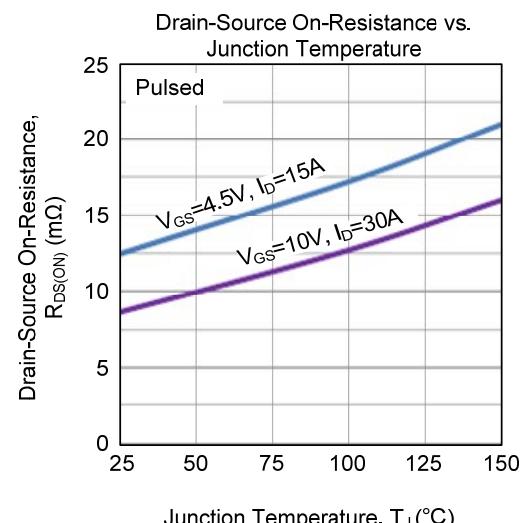
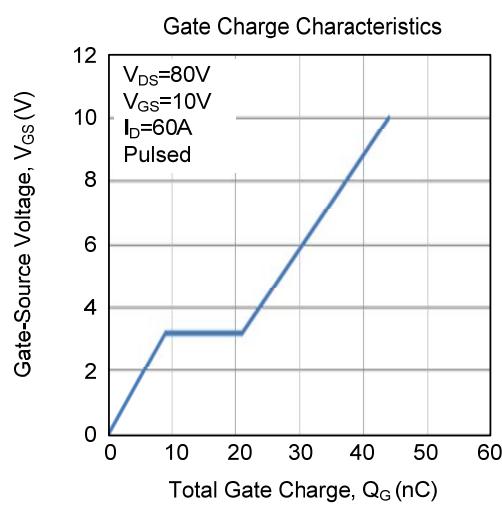
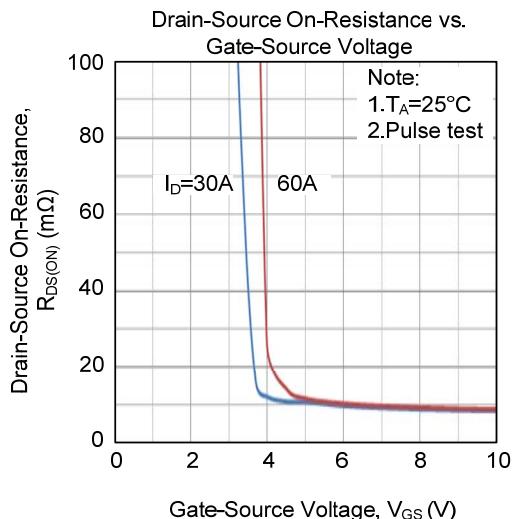
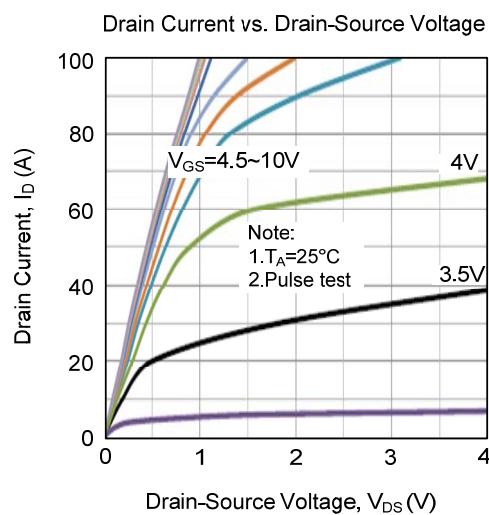
**Gate Charge Waveform**



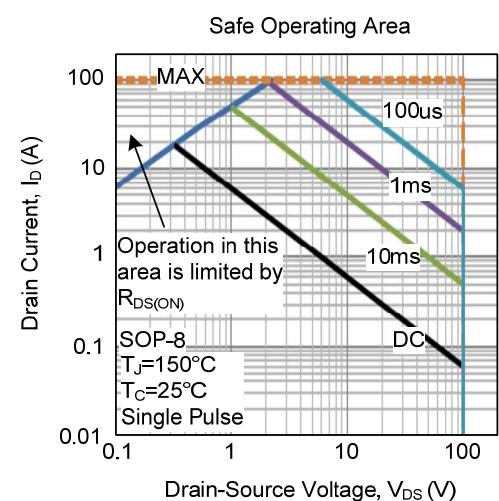
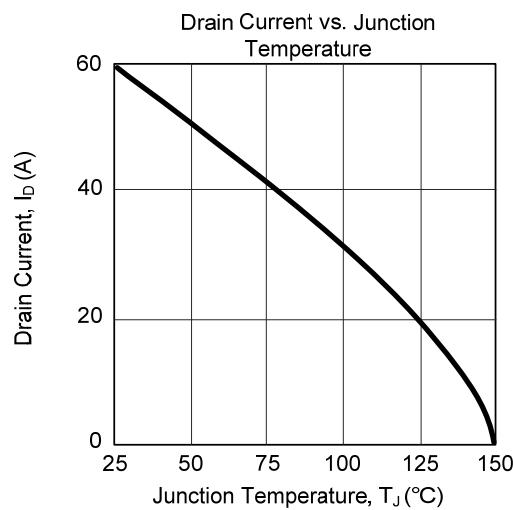
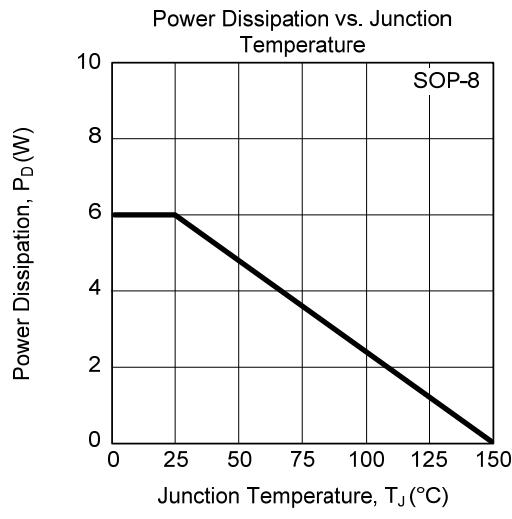
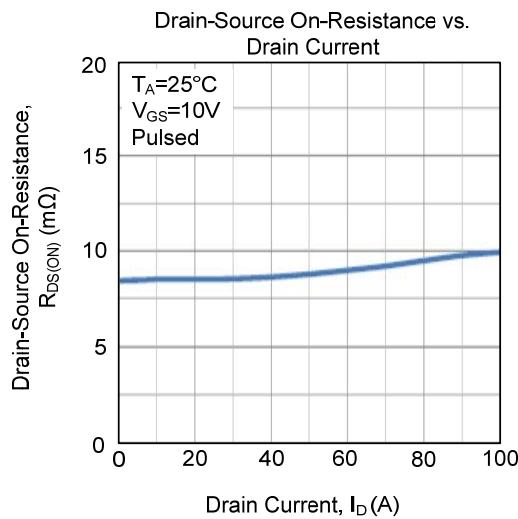
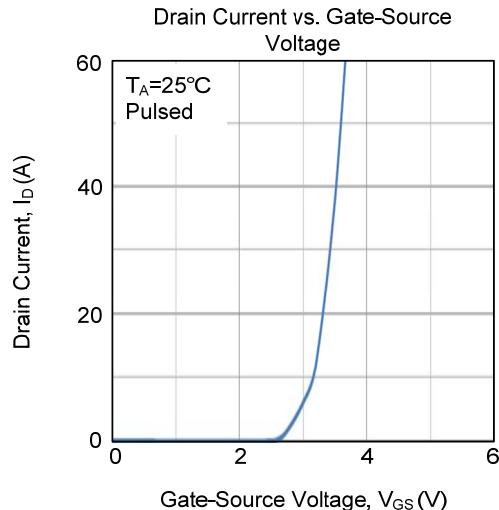
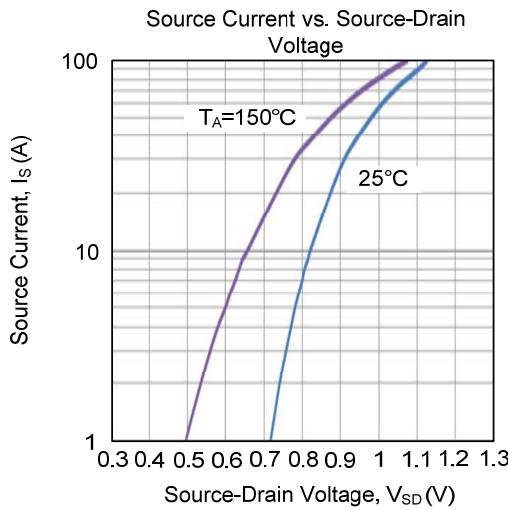
**Unclamped Inductive Switching Test Circuit**

**Unclamped Inductive Switching Waveforms**

■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



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